PHILIPS

Data handbook

Electronic
components
and materials

# Integrated circuits

Part 2 January 1983

## Bipolar ICs for video equipment

# INTEGRATED CIRCUITS

PART 2 — JANUARY 1983

## BIPOLAR ICs FOR VIDEO EQUIPMENT

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# DATA HANDBOOK SYSTEM

Our Data Handbook System is a comprehensive source of information on electronic components, subassemblies and materials; it is made up of four series of handbooks each comprising several parts.

| | |
|---|---|
| ELECTRON TUBES | BLUE |
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| COMPONENTS AND MATERIALS | GREEN |

The several parts contain all pertinent data available at the time of publication, and each is revised and reissued periodically.

Where ratings or specifications differ from those published in the preceding edition they are pointed out by arrows. Where application information is given it is advisory and does not form part of the product specification.

If you need confirmation that the published data about any of our products are the latest available, please contact our representative. He is at your service and will be glad to answer your inquiries.

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# ELECTRON TUBES (BLUE SERIES)

The blue series of data handbooks is comprised of the following parts:

| | |
|---|---|
| **T1** | **Tubes for r.f. heating** |
| **T2** | **Transmitting tubes for communications** |
| **T3** | **Klystrons, travelling-wave tubes, microwave diodes** |
| **ET3** | **Special Quality tubes, miscellaneous devices** (will not be reprinted) |
| **T4** | **Magnetrons** |
| **T5** | **Cathode-ray tubes**<br>Instrument tubes, monitor and display tubes, C.R. tubes for special applications |
| **T6** | **Geiger-Müller tubes** |
| **T7** | **Gas-filled tubes**<br>Segment indicator tubes, indicator tubes, dry reed contact units, thyratrons, industrial rectifying tubes, ignitrons, high-voltage rectifying tubes, associated accessories |
| **T8** | **Picture tubes and components**<br>Colour TV picture tubes, black and white TV picture tubes, colour monitor tubes for data graphic display, monochrome monitor tubes for data graphic display, components for colour television, components for black and white television and monochrome data graphic display |
| **T9** | **Photo and electron multipliers**<br>Photomultiplier tubes, phototubes, single channel electron multipliers, channel electron multiplier plates |
| **T10** | **Camera tubes and accessories, image intensifiers** |
| **T11** | **Microwave components and assemblies** |

# SEMICONDUCTORS (RED SERIES)

The red series of data handbooks is comprised of the following parts:

| | |
|---|---|
| **S1** | **Diodes**<br>Small-signal germanium diodes, small-signal silicon diodes, voltage regulator diodes(< 1,5 W), voltage reference diodes, tuner diodes, rectifier diodes |
| **S2** | **Power diodes, thyristors, triacs**<br>Rectifier diodes, voltage regulator diodes (> 1,5 W), rectifier stacks, thyristors, triacs |
| **S3** | **Small-signal transistors** |
| **S4** | **Low-frequency power transistors and hybrid IC modules** |
| **S5** | **Field-effect transistors** |
| **S6** | **R.F. power transistors and modules** |
| **S7** | **Microminiature semiconductors for hybrid circuits** |
| **S8** | **Devices for optoelectronics**<br>Photosensitive diodes and transistors, light-emitting diodes, displays, photocouplers, infrared sensitive devices, photoconductive devices. |
| **S9** | Taken into handbook T11 of the blue series |
| **S10** | **Wideband transistors and wideband hybrid IC modules** |

# INTEGRATED CIRCUITS (PURPLE SERIES)

The purple series of data handbooks is comprised of the following parts:

| | |
|---|---|
| **IC1** | **Bipolar ICs for radio and audio equipment** |
| **IC2** | **Bipolar ICs for video equipment** |
| **IC3** | **ICs for digital systems in radio, audio and video equipment** |
| **IC4** | **Digital integrated circuits**<br>LOCMOS HE4000B family |
| **IC5** | **Digital integrated circuits — ECL**<br>ECL10 000 (GX family), ECL100 000 (HX family), dedicated designs |
| **IC6*** | **Professional analogue integrated circuits** |
| **IC7** | **Signetics bipolar memories** |
| **IC8** | **Signetics analogue circuits** |
| **IC9** | **Signetics TTL logic** |

* This handbook will be available later this year.

# COMPONENTS AND MATERIALS (GREEN SERIES)

The green series of data handbooks is comprised of the following parts:

| | |
|---|---|
| **C1** | **Assemblies for industrial use**<br>PLC modules, PC20 modules, HNIL FZ/30 series, NORbits 60-, 61-, 90-series, input devices, hybrid ICs, peripheral devices |
| **C2** | **Television tuners, video modulators, surface acoustic wave filters** |
| **C3** | **Loudspeakers** |
| **C4** | **Ferroxcube potcores, square cores and cross cores** |
| **C5** | **Ferroxcube for power, audio/video and accelerators** |
| **C6** | **Electric motors and accessories**<br>Permanent magnet synchronous motors, stepping motors, direct current motors |
| **C7** | **Variable capacitors** |
| **C8** | **Variable mains transformers** |
| **C9** | **Piezoelectric quartz devices**<br>Quartz crystal units, temperature compensated crystal oscillators, compact integrated oscillators, quartz crystal cuts for temperature measurements |
| **C10** | **Connectors** |
| **C11** | **Non-linear resistors**<br>Voltage dependent resistors (VDR), light dependent resistors (LDR), negative temperature coefficient thermistors (NTC), positive temperature coefficient thermistors (PTC) |
| **C12** | **Variable resistors and test switches** |
| **C13** | **Fixed resistors** |
| **C14** | **Electrolytic and solid capacitors** |
| **C15** | **Film capacitors, ceramic capacitors** |
| **C16** | **Piezoelectric ceramics, permanent magnet materials** |

# FUNCTIONAL AND NUMERICAL INDEX
# MAINTENANCE TYPE LIST

# SELECTION GUIDE BY FUNCTION

| type number | description | package code | pins |
|---|---|---|---|
| **Vision i.f. circuits** | | | |
| *Economical circuits* | | | |
| TDA2540 | i.f. amplifier and demodulator; n-p-n tuners | SOT-38 | 16 |
| TDA2540Q | i.f. amplifier and demodulator; n-p-n tuners | SOT-58 | 16 |
| TDA2541 | i.f. amplifier and demodulator; p-n-p tuners | SOT-38 | 16 |
| TDA2541Q | i.f. amplifier and demodulator; p-n-p tuners | SOT-58 | 16 |
| TDA2542 | i.f. amplifier and demodulator; for E and L standards; p-n-p tuners | SOT-38 | 16 |
| TDA2542Q | i.f. amplifier and demodulator; for E and L standards; p-n-p tuners | SOT-58 | 16 |
| TDA2544 | i.f. amplifier and demodulator; MOS tuners | SOT-38 | 16 |
| TDA2544Q | i.f. amplifier and demodulator; MOS tuners | SOT-58 | 16 |
| TDA2548 | i.f. amplifier and demodulator; p-n-p tuners | SOT-38 | 16 |
| TDA2548Q | i.f. amplifier and demodulator; p-n-p tuners | SOT-58 | 16 |
| TDA2549 | i.f. amplifier and demodulator; for multistandard TV receivers | – | – |
| *High-performance circuits* | | | |
| TDA3540 | i.f. amplifier and demodulator; n-p-n tuners | SOT-38 | 16 |
| TDA3540Q | i.f. amplifier and demodulator; n-p-n tuners | SOT-58 | 16 |
| TDA3541 | i.f. amplifier and demodulator; p-n-p tuners | SOT-38 | 16 |
| TDA3541Q | i.f. amplifier and demodulator; p-n-p tuners | SOT-58 | 16 |
| **Colour decoding circuits** | | | |
| TBA540 | reference combination | SOT-38 | 16 |
| TBA540Q | reference combination | SOT-58 | 16 |
| TCA640 | chrominance amplifier for SECAM or PAL/SECAM decoders | SOT-38 | 16 |
| TCA650 | chrominance demodulator for SECAM or PAL/SECAM decoders | SOT-38 | 16 |
| TCA660B | contrast, saturation and brightness control circuit for colour difference and luminance signals | SOT-38 | 16 |
| TDA2510 | chrominance combination | SOT-38 | 16 |
| TDA2510Q | chrominance combination | SOT-58 | 16 |
| TDA2520 | colour demodulator combination | SOT-38 | 16 |
| TDA2520Q | colour demodulator combination | SOT-58 | 16 |
| TDA2522 | colour demodulator combination | SOT-38 | 16 |

## SELECTION GUIDE BY FUNCTION (continued)

| type number | description | package code | pins |
|---|---|---|---|
| **Colour decoding circuits** (continued) | | | |
| TDA2522Q | colour demodulator combination | SOT-58 | 16 |
| TDA2523 | colour demodulator combination | SOT-38 | 16 |
| TDA2523Q | colour demodulator combination | SOT-58 | 16 |
| TDA2524 | colour demodulator combination | SOT-38 | 16 |
| TDA2525 | colour demodulator combination | SOT-38 | 16 |
| TDA2530 | RGB matrix preamplifier | SOT-38 | 16 |
| TDA2530Q | RGB matrix preamplifier | SOT-58 | 16 |
| TDA2532 | RGB matrix preamplifier | SOT-38 | 16 |
| TDA2532Q | RGB matrix preamplifier | SOT-58 | 16 |
| TDA2560 | luminance and chrominance control combination | SOT-38 | 16 |
| TDA2560Q | luminance and chrominance control combination | SOT-58 | 16 |
| TDA3500 | video control combination | SOT-117 | 28 |
| TDA3501 | video control combination | SOT-117 | 28 |
| TDA3505 | video control combination with automatic cut-off control | SOT-117 | 28 |
| TDA3510 | PAL decoder | SOT-101A | 24 |
| TDA3520 | SECAM decoder | SOT-117 | 28 |
| TDA3560 | PAL decoder | SOT-117 | 28 |
| TDA3561A | PAL decoder | SOT-117 | 28 |
| TDA3562A | PAL/NTSC decoder | SOT-117 | 28 |
| TDA3563 | NTSC decoder | SOT-117 | 28 |
| TDA3570 | NTSC decoder | — | 28 |
| TDA3590 | SECAM processor circuit | SOT-101B | 24 |
| TDA3590A | SECAM processor circuit (improved TDA3590) | SOT-101B | 24 |
| TDA3591 | SECAM processor circuit | SOT-101B | 24 |
| **Vertical deflection circuits** | | | |
| TDA2652 | vertical deflection circuit; 20AX; 30AX | SOT-69C | 16 |
| TDA2653 | vertical deflection circuit; PIL-S4; 30AX | SOT-69C | 16 |
| TDA2653A | vertical deflection circuit; PIL-S4; 30AX | SOT-141B | 13 |
| TDA2654 | vertical deflection circuit; monochrome, 110°; tiny-vision colour, 90° | SOT-110B | 9 |
| TDA2655A | vertical deflection circuit; colour, 90° | SOT-150 | 12 |
| TDA2655B | vertical deflection circuit; colour and monochrome, 90° | SOT-150 | 12 |
| TDA3650 | vertical deflection circuit | SOT-141B | 13 |
| TDA3651 | vertical deflection circuit | SOT-110B | 9 |
| TDA3651A | vertical deflection circuit | SOT-131B | 9 |
| TDA3651AQ | vertical deflection circuit | SOT-157B | 9 |
| TDA3652 | vertical deflection circuit | SOT-131B | 9 |
| TDA3652Q | vertical deflection circuit | SOT-157B | 9 |

TBA 950 ( Ha:TBA 920)

| type number | description | package code | pins |
|---|---|---|---|
| **Sync processors; horizontal; vertical** | | | |
| TBA720A | horizontal oscillator circuit | SOT-38 | 16 |
| TBA720AQ | horizontal oscillator circuit | SOT-58 | 16 |
| TBA890 | signal processing circuit | SOT-38 | 16 |
| TBA890Q | signal processing circuit | SOT-58 | 16 |
| TBA920 | horizontal combination | SOT-38 | 16 |
| TBA920Q | horizontal combination | SOT-58 | 16 |
| * TBA920S | horizontal combination | SOT-38 | 16 |
| TDA2571A | horizontal synchronization and vertical 625 divider system | SOT-38 | 16 |
| TDA2571AQ | horizontal synchronization and vertical 625 divider system | SOT-58 | 16 |
| TDA2575A | horizontal synchronization and vertical 625 divider system | SOT-38 | 16 |
| TDA2575AQ | horizontal synchronization and vertical 625 divider system | SOT-58 | 16 |
| TDA2576A | horizontal oscillator combination with vertical 625 divider system | SOT-38 | 16 |
| TDA2577A | synchronization circuit with vertical oscillator and driver stages | SOT-102HE | 18 |
| TDA2578A | synchronization circuit with vertical oscillator and driver stages | SOT-102HE | 18 |
| TDA2593 | horizontal combination | SOT-38 | 16 |
| TDA2594 | horizontal combination with transmitter identification | SOT-102DS | 18 |
| TDA2595 | horizontal combination with transmitter identification and protection circuits | SOT-102CS | 18 |
| TDA3571B | sync combination with transmitter identification and vertical 625 divider system | SOT-102A | 18 |
| TDA3576B | sync combination with transmitter identification and vertical 625 divider system | SOT-102HE4 | 18 |
| **Sound circuits** | | | |
| TBA120U | sound i.f. amplifier/demodulator for TV | VO-36 | 14 |
| TBA750C | limiter/amplifier | SOT-38 | 16 |
| TBA750CQ | limiter/amplifier | SOT-58 | 16 |
| TDA1028 | signal sources switch (2 x four channels) | SOT-38 | 16 |
| TDA1029 | signal sources switch (4 x two channels) | SOT-38 | 16 |
| TDA1512 | 12 to 20 W hi-fi audio power amplifier | SOT-131B | 9 |
| TDA1512Q | 12 to 20 W hi-fi audio power amplifier | SOT-157B | 9 |
| TDA1520 | 20 W hi-fi audio power amplifier | SOT-131A | 9 |
| TDA1524 | stereo-tone volume control circuit | SOT-102CS | 18 |
| TDA2543 | AM sound i.f. circuit for French standard | SOT-102CS | 18 |
| TDA2545 | quasi-split-sound circuit | SOT-38 | 16 |
| TDA2546 | quasi-split-sound circuit with 5,5 MHz demodulation | SOT-102CS | 18 |
| TDA2611A | 5 W audio power amplifier | SOT-110B | 9 |
| TDA2791 | TV sound combination; volume, treble, bass | SOT-38 | 16 |
| TDA2795 | TV stereo/dual sound identification decoder | SOT-102DS | 18 |
| TDA3800 | stereo/dual TV sound processing circuit | SOT-117 | 28 |

## SELECTION GUIDE BY FUNCTION (continued)

| type number | description | package code | pins |
|---|---|---|---|
| **Video recorder circuits** | | | |
| TDA2721 | colour sub-carrier oscillator and mixer (video recorders) | SOT-38 | 16 |
| TDA2730 | FM limiter/demodulator (video recorders) | SOT-38 | 16 |
| TDA2740 | amplifier and drop-out identification circuit (video recorders) | SOT-38 | 16 |
| TDA3700A | PAL synchronization processor (video recorders) | SOT-117 | 28 |
| TDA3710 | chrominance signal/mixer (video recorders) | SOT-117 | 28 |
| TDA3771 | video processor (video recorders) | SOT-102CS | 18 |
| TDA3780 | frequency modulator (video recorders) | SOT-102CS | 18 |
| **Miscellaneous** | | | |
| SAA5030 | videotex/video processor | SOT-101A | 24 |
| TDA0820T | double balanced modulator/demodulator | SOT-108A (SO-14) | 14 |
| TDA2581 | control circuit for SMPS | SOT-38 | 16 |
| TDA2581Q | control circuit for SMPS | SOT-58 | 16 |
| TDA2582 | control circuit for PPS | SOT-38 | 16 |
| TDA2582Q | control circuit for PPS | SOT-58 | 16 |
| TDA2640 | SMPS drive circuit | SOT-38 | 16 |
| TDA2640Q | SMPS drive circuit | SOT-58 | 16 |
| TDA3047 | infrared receiver | – | – |
| TDA3048 | infrared receiver | – | – |
| TDA4500 | small signal combination IC for monochrome TV | SOT-117 | 28 |
| TEA1002 | PAL colour encoder and video summer | SOT-102CS | 18 |

# NUMERICAL INDEX

| type number | description | package code | pins |
|---|---|---|---|
| SAA5030 | videotex/video processor | SOT-101A | 24 |
| TBA120U | sound i.f. amplifier/demodulator for TV | VO-36 | 14 |
| TBA540 | reference combination | SOT-38 | 16 |
| TBA540Q | reference combination | SOT-58 | 16 |
| TBA720A | horizontal oscillator circuit | SOT-38 | 16 |
| TBA720AQ | horizontal oscillator circuit | SOT-58 | 16 |
| TBA750C | limiter/amplifier | SOT-38 | 16 |
| TBA750CQ | limiter/amplifier | SOT-58 | 16 |
| TBA890 | signal processing circuit | SOT-38 | 16 |
| TBA890Q | signal processing circuit | SOT-58 | 16 |
| TBA920 | horizontal combination | SOT-38 | 16 |
| TBA920Q | horizontal combination | SOT-58 | 16 |
| TBA920S | horizontal combination | SOT-38 | 16 |
| TCA640 | chrominance amplifier for SECAM or PAL/SECAM decoders | SOT-38 | 16 |
| TCA650 | chrominance demodulator for SECAM or PAL/SECAM decoders | SOT-38 | 16 |
| TCA660B | contrast, saturation and brightness control circuit for colour difference and luminance signals | SOT-38 | 16 |
| TDA0820T | double balanced modulator/demodulator | SOT-108A (SO-14) | 14 |
| TDA1028 | signal sources switch (2 x four channels) | SOT-38 | 16 |
| TDA1029 | signal sources switch (4 x two channels) | SOT-38 | 16 |
| TDA1512 | 12 to 20 W hi-fi audio power amplifier | SOT-131B | 9 |
| TDA1512Q | 12 to 20 W hi-fi audio power amplifier | SOT-157B | 9 |
| TDA1520 | 20 W hi-fi audio power amplifier | SOT-131A | 9 |
| TDA1524 | stereo-tone volume control circuit | SOT-102CS | 18 |
| TDA2510 | chrominance combination | SOT-38 | 16 |
| TDA2510Q | chrominance combination | SOT-58 | 16 |
| TDA2520 | colour demodulator combination | SOT-38 | 16 |
| TDA2520Q | colour demodulator combination | SOT-58 | 16 |
| TDA2522 | colour demodulator combination | SOT-38 | 16 |
| TDA2522Q | colour demodulator combination | SOT-58 | 16 |
| TDA2523 | colour demodulator combination | SOT-38 | 16 |
| TDA2523Q | colour demodulator combination | SOT-58 | 16 |
| TDA2524 | colour demodulator combination | SOT-38 | 16 |
| TDA2525 | colour demodulator combination | SOT-38 | 16 |
| TDA2530 | RGB matrix preamplifier | SOT-38 | 16 |
| TDA2530Q | RGB matrix preamplifier | SOT-58 | 16 |

## NUMERICAL INDEX (continued)

| type number | description | package code | pins |
|---|---|---|---|
| TDA2532 | RGB matrix preamplifier | SOT-38 | 16 |
| TDA2532Q | RGB matrix preamplifier | SOT-58 | 16 |
| TDA2540 | i.f. amplifier and demodulator; n-p-n tuners | SOT-38 | 16 |
| TDA2540Q | i.f. amplifier and demodulator; n-p-n tuners | SOT-58 | 16 |
| TDA2541 | i.f. amplifier and demodulator; p-n-p tuners | SOT-38 | 16 |
| TDA2541Q | i.f. amplifier and demodulator; p-n-p tuners | SOT-58 | 16 |
| TDA2542 | i.f. amplifier and demodulator; for E and L standards; p-n-p tuners | SOT-38 | 16 |
| TDA2542Q | i.f. amplifier and demodulator; for E and L standards; p-n-p tuners | SOT-58 | 16 |
| TDA2543 | AM sound i.f. circuit for French standard | SOT-102CS | 18 |
| TDA2544 | i.f. amplifier and demodulator; MOS tuners | SOT-38 | 16 |
| TDA2544Q | i.f. amplifier and demodulator; MOS tuners | SOT-58 | 16 |
| TDA2545 | quasi-split-sound circuit | SOT-38 | 16 |
| TDA2546 | quasi-split-sound circuit with 5,5 MHz demodulation | SOT-102CS | 18 |
| TDA2548 | i.f. amplifier and demodulator; p-n-p tuners | SOT-38 | 16 |
| TDA2548Q | i.f. amplifier and demodulator; p-n-p tuners | SOT-58 | 16 |
| TDA2549 | i.f. amplifier and demodulator; for multistandard TV receivers | – | – |
| TDA2560 | luminance and chrominance control combination | SOT-38 | 16 |
| TDA2560Q | luminance and chrominance control combination | SOT-58 | 16 |
| TDA2571A | horizontal synchronization and vertical 625 divider system | SOT-38 | 16 |
| TDA2571AQ | horizontal synchronization and vertical 625 divider system | SOT-58 | 16 |
| TDA2575A | horizontal synchronization and vertical 625 divider system | SOT-38 | 16 |
| TDA2575AQ | horizontal synchronization and vertical 625 divider system | SOT-58 | 16 |
| TDA2576A | horizontal oscillator combination with vertical 625 divider system | SOT-38 | 16 |
| TDA2577A | synchronization circuit with vertical oscillator and driver stages | SOT-102HE | 18 |
| TDA2578A | synchronization circuit with vertical oscillator and driver stages | SOT-102HE | 18 |
| TDA2581 | control circuit for SMPS | SOT-38 | 16 |
| TDA2581Q | control circuit for SMPS | SOT-58 | 16 |
| TDA2582 | control circuit for PPS | SOT-38 | 16 |
| TDA2582Q | control circuit for PPS | SOT-58 | 16 |
| TDA2593 | horizontal combination | SOT-38 | 16 |
| TDA2594 | horizontal combination with transmitter identification | SOT-102DS | 18 |
| TDA2595 | horizontal combination with transmitter identification and protection circuits | SOT-102CS | 18 |
| TDA2611A | 5 W audio power amplifier | SOT-110B | 9 |
| TDA2640 | SMPS drive circuit | SOT-38 | 16 |
| TDA2640Q | SMPS drive circuit | SOT-58 | 16 |

| type number | description | package code | pins |
|---|---|---|---|
| TDA2652 | vertical deflection circuit; 20AX; 30AX | SOT-69C | 16 |
| TDA2653 | vertical deflection circuit; PIL-S4; 30AX | SOT-69C | 16 |
| TDA2653A | vertical deflection circuit; PIL-S4; 30AX | SOT-141B | 13 |
| TDA2654 | vertical deflection circuit; monochrome, 110°; tiny-vision colour, 90° | SOT-110B | 9 |
| TDA2655A | vertical deflection circuit; colour, 90° | SOT-150 | 12 |
| TDA2655B | vertical deflection circuit; colour and monochrome, 90° | SOT-150 | 12 |
| TDA2721 | colour sub-carrier oscillator and mixer (video recorders) | SOT-38 | 16 |
| TDA2730 | FM limiter/demodulator (video recorders) | SOT-38 | 16 |
| TDA2740 | amplifier and drop-out identification circuit (video recorders) | SOT-38 | 16 |
| TDA2791 | TV sound combination; volume, treble, bass | SOT-38 | 16 |
| TDA2795 | TV stereo/dual sound identification decoder | SOT-102DS | 18 |
| TDA3047 | infrared receiver | – | – |
| TDA3048 | infrared receiver | – | – |
| TDA3500 | video control combination | SOT-117 | 28 |
| TDA3501 | video control combination | SOT-117 | 28 |
| TDA3505 | video control combination with automatic cut-off control | SOT-117 | 28 |
| TDA3510 | PAL decoder | SOT-101A | 24 |
| TDA3520 | SECAM decoder | SOT-117 | 28 |
| TDA3540 | i.f. amplifier and demodulator; n-p-n tuners | SOT-38 | 16 |
| TDA3540Q | i.f. amplifier and demodulator; n-p-n tuners | SOT-58 | 16 |
| TDA3541 | i.f. amplifier and demodulator; p-n-p tuners | SOT-38 | 16 |
| TDA3541Q | i.f. amplifier and demodulator; p-n-p tuners | SOT-58 | 16 |
| TDA3560 | PAL decoder | SOT-117 | 28 |
| TDA3561A | PAL decoder | SOT-117 | 28 |
| TDA3562A | PAL/NTSC decoder | SOT-117 | 28 |
| TDA3563 | NTSC decoder | SOT-117 | 28 |
| TDA3570 | NTSC decoder | – | 28 |
| TDA3571B | sync combination with transmitter identification and vertical 625 divider system | SOT-102A | 18 |
| TDA3576B | sync combination with transmitter identification and vertical 625 divider system | SOT-102HE4 | 18 |
| TDA3590 | SECAM processor circuit | SOT-101B | 24 |
| TDA3590A | SECAM processor circuit (improved TDA3590) | SOT-101B | 24 |
| TDA3591 | SECAM processor circuit | SOT-101B | 24 |
| TDA3650 | vertical deflection circuit | SOT-141B | 13 |
| TDA3651 | vertical deflection circuit | SOT-110B | 9 |
| TDA3651A | vertical deflection circuit | SOT-131B | 9 |
| TDA3651AQ | vertical deflection circuit | SOT-157B | 9 |
| TDA3652 | vertical deflection circuit | SOT-131B | 9 |
| TDA3652Q | vertical deflection circuit | SOT-157B | 9 |
| TDA3700A | PAL synchronization processor (video recorders) | SOT-117 | 28 |
| TDA3710 | chrominance signal/mixer (video recorders) | SOT-117 | 28 |

**NUMERICAL INDEX** (continued)

| type number | description | package code | pins |
|---|---|---|---|
| TDA3771 | video processor (video recorders) | SOT-102CS | 18 |
| TDA3780 | frequency modulator (video recorders) | SOT-102CS | 18 |
| TDA3800 | stereo/dual TV sound processing circuit | SOT-117 | 28 |
| TDA4500 | small signal combination IC for monochrome TV | SOT-117 | 28 |
| TEA1002 | PAL colour encoder and video summer | SOT-102CS | 18 |

# MAINTENANCE TYPE LIST

| | |
|---|---|
| TAA550 | |
| TBA530; Q | |
| TBA560C; CQ | |
| TCA270S; SQ | |
| TCA420A | |
| TCA530 | |
| TCA750 | |
| TDA2573A | |
| TDA2576 | successor type: TDA2576A |
| TDA2610; A | |
| TDA2612 | |
| TDA2700 | |
| TDA2710 | |
| TDA2720 | successor type: TDA2721 |
| TDA2790 | |

# GENERAL

**Type designation**
**Rating systems**

# PRO ELECTRON TYPE DESIGNATION CODE FOR INTEGRATED CIRCUITS

This type nomenclature applies to semiconductor monolithic, semiconductor multi-chip, thin-film, thick-film and hybrid integrated circuits.

A basic number consists of:

*THREE LETTERS FOLLOWED BY A SERIAL NUMBER*

## FIRST AND SECOND LETTER

1. DIGITAL FAMILY CIRCUITS

   The FIRST TWO LETTERS identify the FAMILY (see note 1).

2. SOLITARY CIRCUITS

   The FIRST LETTER divides the solitary circuits into:

   S : Solitary digital circuits
   T : Analogue circuits
   U : Mixed analogue/digital circuits

   The SECOND LETTER is a serial letter without any further significance except 'H' which stands for hybrid circuits.

3. MICROPROCESSORS

   The FIRST TWO LETTERS identify microprocessors and correlated circuits as follows:

   MA : Microcomputer / Central processing unit
   MB : Slice processor (see note 2)
   MD : Correlated memories
   ME : Other correlated circuits (interface, clock, peripheral controller, etc.)

4. CHARGE-TRANSFER DEVICES AND SWITCHED CAPACITORS

   The FIRST TWO LETTERS identify the following:

   NH : Hybrid circuits
   NL : Logic circuits
   NM : Memories
   NS : Analogue signal processing, using switched capacitors
   NT : Analogue signal processing, using CTDs
   NX : Imaging devices
   NY : Other correlated circuits

**Notes**

1. A logic family is an assembly of digital circuits designed to be interconnected and defined by its basic electrical characteristics (such as: supply voltage, power consumption, propagation delay, noise immunity).
2. By 'slice processor' is meant: a functional slice of microprocessor.

## THIRD LETTER

It indicates the operating ambient temperature range.
The letters A to G give information about the temperature:

A : temperature range not specified
B : 0 to + 70 °C
C : –55 to + 125 °C
D : –25 to + 70 °C
E : –25 to + 85 °C
F : –40 to + 85 °C
G : –55 to + 85 °C

If a circuit is published for another temperature range, the letter indicating a narrower temperature range may be used or the letter 'A'.

Example: the range 0 to + 75 °C can be indicated by 'B' or 'A'.

## SERIAL NUMBER

This may be either a 4-digit number assigned by Pro Electron, or the serial number (which may be a combination of figures and letters) of an existing company type designation of the manufacturer.

To the basic type number may be added:

*A VERSION LETTER*

Indicates a minor variant of the basic type or the package. Except for 'Z', which means customized wiring, the letter has no fixed meaning. The following letters are recommended for package variants:

C : for cylindrical
D : for ceramic DIL
F : for flat pack
L : for chip on tape
P : for plastic DIL
Q : for QIL
T : for miniature plastic (mini-pack)
U : for uncased chip

Alternatively a TWO LETTER SUFFIX may be used instead of a single package version letter, if the manufacturer (sponsor) wishes to give more information.

*FIRST LETTER*: General shape

C : Cylindrical
D : Dual-in-line (DIL)
E : Power DIL (with external heatsink)
F : Flat (leads on 2 sides)
G : Flat (leads on 4 sides)
K : Diamond (TO-3 family)
M : Multiple-in-line (except Dual-, Triple-, Quadruple-in-line)
Q : Quadruple-in-line (QIL)
R : Power QIL (with external heatsink)
S : Single-in-line
T : Triple-in-line

*SECOND LETTER*: Material

C : Metal-ceramic
G : Glass-ceramic (cerdip)
M : Metal
P : Plastic

A hyphen precedes the suffix to avoid confusion with a version letter.

# RATING SYSTEMS

The rating systems described are those recommended by the International Electrotechnical Commission (IEC) in its Publication 134.

## DEFINITIONS OF TERMS USED

*Electronic device.* An electronic tube or valve, transistor or other semiconductor device.

Note
This definition excludes inductors, capacitors, resistors and similar components.

*Characteristic.* A characteristic is an inherent and measurable property of a device. Such a property may be electrical, mechanical, thermal, hydraulic, electro-magnetic, or nuclear, and can be expressed as a value for stated or recognized conditions. A characteristic may also be a set of related values, usually shown in graphical form.

*Bogey electronic device.* An electronic device whose characteristics have the published nominal values for the type. A bogey electronic device for any particular application can be obtained by considering only those characteristics which are directly related to the application.

*Rating.* A value which establishes either a limiting capability or a limiting condition for an electronic device. It is determined for specified values of environment and operation, and may be stated in any suitable terms.

Note
Limiting conditions may be either maxima or minima.

*Rating system.* The set of principles upon which ratings are established and which determine their interpretation.

Note
The rating system indicates the division of responsibility between the device manufacturer and the circuit designer, with the object of ensuring that the working conditions do not exceed the ratings.

## ABSOLUTE MAXIMUM RATING SYSTEM

Absolute maximum ratings are limiting values of operating and environmental conditions applicable to any electronic device of a specified type as defined by its published data, which should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking no responsibility for equipment variations, environmental variations, and the effects of changes in operating conditions due to variations in the characteristics of the device under consideration and of all other electronic devices in the equipment.

The equipment manufacturer should design so that, initially and throughout life, no absolute maximum value for the intended service is exceeded with any device under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, equipment control adjustment, load variations, signal variation, environmental conditions, and variations in characteristics of the device under consideration and of all other electronic devices in the equipment.

## DESIGN MAXIMUM RATING SYSTEM

Design maximum ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking responsibility for the effects of changes in operating conditions due to variations in the characteristics of the electronic device under consideration.

The equipment manufacturer should design so that, initially and throughout life, no design maximum value for the intended service is exceeded with a bogey device under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, variation in characteristics of all other devices in the equipment, equipment control adjustment, load variation, signal variation and environmental conditions.

## DESIGN CENTRE RATING SYSTEM

Design centre ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under normal conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device in average applications, taking responsibility for normal changes in operating conditions due to rated supply voltage variation, equipment component variation, equipment control adjustment, load variation, signal variation, environmental conditions, and variations in the characteristics of all electronic devices.

The equipment manufacturer should design so that, initially, no design centre value for the intended service is exceeded with a bogey electronic device in equipment operating at the stated normal supply voltage.

# PACKAGE OUTLINES

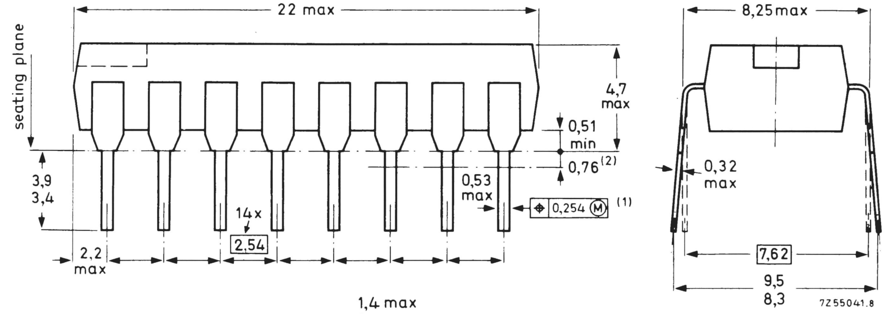
In this chapter the package outlines are given for the following types, except for those marked with an asterisk which are included in the device data sheet.

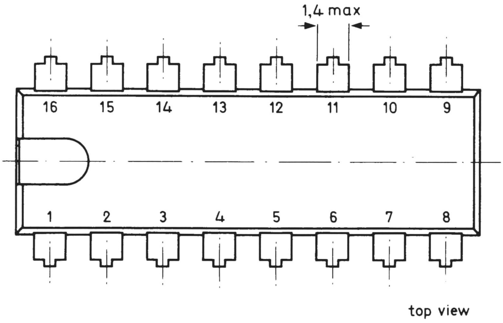
| type number | package code | description |
|---|---|---|
| SAA5030 | SOT-101A | 24-lead dual in-line; plastic with internal heat spreader (SOT-101A) |
| TBA120U | VO-36 | 14-lead dual in-line; plastic (VO-36) |
| TBA540 | SOT-38 | 16-lead dual in-line; plastic (SOT-38) |
| TBA540Q | SOT-58 | 16-lead quadruple in-line; plastic (SOT-58) |
| TBA720A | SOT-38 | 16-lead dual in-line; plastic (SOT-38) |
| TBA720AQ | SOT-58 | 16-lead quadruple in-line; plastic (SOT-58) |
| TBA750C | SOT-38 | 16-lead dual in-line; plastic (SOT-38) |
| TBA750CQ | SOT-58 | 16-lead quadruple in-line; plastic (SOT-58) |
| TBA890 | SOT-38 | 16-lead dual in-line; plastic (SOT-38) |
| TBA890Q | SOT-58 | 16-lead quadruple in-line; plastic (SOT-58) |
| TBA920 | SOT-38 | 16-lead dual in-line; plastic (SOT-38) |
| TBA920Q | SOT-58 | 16-lead quadruple in-line; plastic (SOT-58) |
| TBA920S | SOT-38 | 16-lead dual in-line; plastic (SOT-38) |
| TCA640 | SOT-38 | 16-lead dual in-line; plastic (SOT-38) |
| TCA650 | SOT-38 | 16-lead dual in-line; plastic (SOT-38) |
| TCA660B | SOT-38 | 16-lead dual in-line; plastic (SOT-38) |
| TDA0820T | SOT-108A | 14-lead mini-pack; plastic (SO-14; SOT-108A) |
| TDA1028 | SOT-38 | 16-lead dual in-line; plastic (SOT-38) |
| TDA1029 | SOT-38 | 16-lead dual in-line; plastic (SOT-38) |
| TDA1512 | SOT-131B | 9-lead single in-line; plastic power (SOT-131A, B) |
| TDA1512Q | SOT-157B | 9-lead single in-line; plastic power (SOT-157B) |
| TDA1520 | SOT-131A | 9-lead single in-line; plastic power (SOT-131A, B) |
| TDA1524 | SOT-102CS | 18-lead dual in-line; plastic (SOT-102CS) |
| TDA2510 | SOT-38 | 16-lead dual in-line; plastic (SOT-38) |
| TDA2510Q | SOT-58 | 16-lead quadruple in-line; plastic (SOT-58) |
| TDA2520 | SOT-38 | 16-lead dual in-line; plastic (SOT-38) |
| TDA2520Q | SOT-58 | 16-lead quadruple in-line; plastic (SOT-58) |
| TDA2522 | SOT-38 | 16-lead dual in-line; plastic (SOT-38) |
| TDA2522Q | SOT-58 | 16-lead quadruple in-line; plastic (SOT-58) |
| TDA2523 | SOT-38 | 16-lead dual in-line; plastic (SOT-38) |
| TDA2523Q | SOT-58 | 16-lead quadruple in-line; plastic (SOT-58) |
| TDA2524 | SOT-38 | 16-lead dual in-line; plastic (SOT-38) |
| TDA2525 | SOT-38 | 16-lead dual in-line; plastic (SOT-38) |
| TDA2530 | SOT-38 | 16-lead dual in-line; plastic (SOT-38) |
| TDA2530Q | SOT-58 | 16-lead quadruple in-line; plastic (SOT-58) |
| TDA2532 | SOT-38 | 16-lead dual in-line; plastic (SOT-38) |
| TDA2532Q | SOT-58 | 16-lead quadruple in-line; plastic (SOT-58) |
| TDA2540 | SOT-38 | 16-lead dual in-line; plastic (SOT-38) |
| TDA2540Q | SOT-58 | 16-lead quadruple in-line; plastic (SOT-58) |
| TDA2541 | SOT-38 | 16-lead dual in-line; plastic (SOT-38) |

| type number | package code | description |
|---|---|---|
| TDA2541Q | SOT-58 | 16-lead quadruple in-line; plastic (SOT-58) |
| TDA2542 | SOT-38 | 16-lead dual in-line; plastic (SOT-38) |
| TDA2542Q | SOT-58 | 16-lead quadruple in-line; plastic (SOT-58) |
| TDA2543 | SOT-102CS | 18-lead dual in-line; plastic (SOT-102CS) |
| TDA2544 | SOT-38 | 16-lead dual in-line; plastic (SOT-38) |
| TDA2544Q | SOT-58 | 16-lead quadruple in-line; plastic (SOT-58) |
| TDA2545 | SOT-38 | 16-lead dual in-line; plastic (SOT-38) |
| TDA2546 | SOT-102CS | 18-lead dual in-line; plastic (SOT-102CS) |
| TDA2548 | SOT-38 | 16-lead dual in-line; plastic (SOT-38) |
| TDA2548Q | SOT-58 | 16-lead quadruple in-line; plastic (SOT-58) |
| TDA2549 | – | not yet determined |
| TDA2560 | SOT-38 | 16-lead dual in-line; plastic (SOT-38) |
| TDA2560Q | SOT-58 | 16-lead quadruple in-line; plastic (SOT-58) |
| TDA2571A | SOT-38 | 16-lead dual in-line; plastic (SOT-38) |
| TDA2571AQ | SOT-58 | 16-lead quadruple in-line; plastic (SOT-58) |
| TDA2575A | SOT-38 | 16-lead dual in-line; plastic (SOT-38) |
| TDA2575AQ | SOT-58 | 16-lead quadruple in-line; plastic (SOT-58) |
| TDA2576A | SOT-38 | 16-lead dual in-line; plastic (SOT-38) |
| TDA2577A | SOT-102HE | 18-lead dual in-line; plastic (SOT-102HE) |
| TDA2578A | SOT-102HE | 18-lead dual in-line; plastic (SOT-102HE) |
| TDA2581 | SOT-38 | 16-lead dual in-line; plastic (SOT-38) |
| TDA2581Q | SOT-58 | 16-lead quadruple in-line; plastic (SOT-58) |
| TDA2582 | SOT-38 | 16-lead dual in-line; plastic (SOT-38) |
| TDA2582Q | SOT-58 | 16-lead quadruple in-line; plastic (SOT-58) |
| TDA2593 | SOT-38 | 16-lead dual in-line; plastic (SOT-38) |
| TDA2594 | SOT-102DS | 18-lead dual in-line; plastic (SOT-102DS) |
| TDA2595 | SOT-102CS | 18-lead dual in-line; plastic (SOT-102CS) |
| TDA2611A | SOT-110B | 9-lead single in-line; plastic (SOT-110B) |
| TDA2640 | SOT-38 | 16-lead dual in-line; plastic (SOT-38) |
| TDA2640Q | SOT-58 | 16-lead quadruple in-line; plastic (SOT-58) |
| TDA2652 | SOT-69C | 16-lead dual in-line; plastic power (SOT-69C) |
| TDA2653 | SOT-69C | 16-lead dual in-line; plastic power (SOT-69C) |
| TDA2653A | SOT-141B | 13-lead SIL-bent-to-DIL; plastic power (SOT-141B) |
| TDA2654 | SOT-110B | 9-lead single in-line; plastic (SOT-110B) |
| TDA2655A | SOT-150 | 12-lead dual in-line; plastic with metal cooling fin (SOT-150) |
| TDA2655B | SOT-150 | 12-lead dual in-line; plastic with metal cooling fin (SOT-150) |
| TDA2721 | SOT-38 | 16-lead dual in-line; plastic (SOT-38) |
| TDA2730 | SOT-38 | 16-lead dual in-line; plastic (SOT-38) |
| TDA2740 | SOT-38 | 16-lead dual in-line; plastic (SOT-38) |
| TDA2791 | SOT-38 | 16-lead dual in-line; plastic (SOT-38) |
| TDA2795 | SOT-102DS | 18-lead dual in-line; plastic (SOT-102DS) |
| TDA3047 | – | not yet determined |
| TDA3048 | – | not yet determined |
| TDA3500 | SOT-117 | 28-lead dual in-line; plastic (SOT-117) |
| TDA3501 | SOT-117 | 28-lead dual in-line; plastic (SOT-117) |

| type number | package code | description |
|---|---|---|
| TDA3505 | SOT-117 | 28-lead dual in-line; plastic (SOT-117) |
| TDA3510 | SOT-101A | 24-lead dual in-line; plastic (SOT-101A) |
| TDA3520 | SOT-117 | 28-lead dual in-line; plastic (SOT-117) |
| TDA3540 | SOT-38 | 16-lead dual in-line; plastic (SOT-38) |
| TDA3540Q | SOT-58 | 16-lead quadruple in-line; plastic (SOT-58) |
| TDA3541 | SOT-38 | 16-lead dual in-line; plastic (SOT-38) |
| TDA3541Q | SOT-58 | 16-lead quadruple in-line; plastic (SOT-58) |
| TDA3560 | SOT-117 | 28-lead dual in-line; plastic (SOT-117) |
| TDA3561A | SOT-117 | 28-lead dual in-line; plastic (SOT-117) |
| TDA3562A | SOT-117 | 28-lead dual in-line; plastic (SOT-117) |
| TDA3563 | SOT-117 | 28-lead dual in-line; plastic (SOT-117) |
| TDA3570* | | |
| TDA3571B | SOT-102A | 18-lead dual in-line; plastic (SOT-102A) |
| TDA3576B | SOT-102HE | 18-lead dual in-line; plastic (SOT-102HE4) |
| TDA3590 | SOT-101B | 24-lead dual in-line; plastic with internal heat spreader (SOT-101B) |
| TDA3590A | SOT-101B | 24-lead dual in-line; plastic with internal heat spreader (SOT-101B) |
| TDA3591 | SOT-101B | 24-lead dual in-line; plastic with internal heat spreader (SOT-101B) |
| TDA3650 | SOT-141B | 13-lead SIL-bent-to-DIL; plastic power (SOT-141B) |
| TDA3651 | SOT-110B | 9-lead single in-line; plastic (SOT-110B) |
| TDA3651A | SOT-131B | 9-lead single in-line; plastic power (SOT-131A, B) |
| TDA3651AQ | SOT-157B | 9-lead single in-line; plastic power (SOT-157B) |
| TDA3652 | SOT-131B | 9-lead single in-line; plastic power (SOT-131A, B) |
| TDA3652Q | SOT-157B | 9-lead single in-line; plastic power (SOT-157B) |
| TDA3700A | SOT-117 | 28-lead dual in-line; plastic (SOT-117) |
| TDA3710 | SOT-117 | 28-lead dual in-line; plastic (SOT-117) |
| TDA3771 | SOT-102CS | 18-lead dual in-line; plastic (SOT-102CS) |
| TDA3780 | SOT-102CS | 18-lead dual in-line; plastic (SOT-102CS) |
| TDA3800 | SOT-117 | 28-lead dual in-line; plastic (SOT-117) |
| TDA4500 | SOT-117 | 28-lead dual in-line; plastic with internal heat spreader (SOT-117) |
| TEA1002 | SOT-102CS | 18-lead dual in-line; plastic (SOT-102CS) |

# 16-LEAD DUAL IN-LINE; PLASTIC (SOT-38)


22 max
seating plane
4,7
max
0,51
min
0,76(2)
3,9
3,4
14x
2,54
0,53
max
0,254 Ⓜ (1)
2,2
max
8,25max
0,32
max
7,62
9,5
8,3
7Z55041.8


1,4 max
16
15
14
13
12
11
10
9
1
2
3
4
5
6
7
8
top view

⌖ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

**Dimensions in mm**

## SOLDERING

### 1. By hand

Apply the soldering iron below the seating plane (or not more than 2 mm above it).
If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

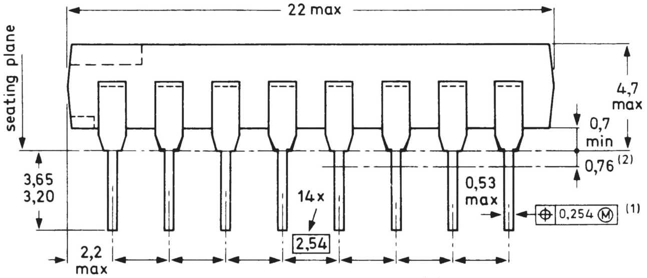
### 2. By dip or wave

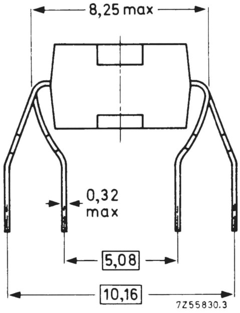
The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.
The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

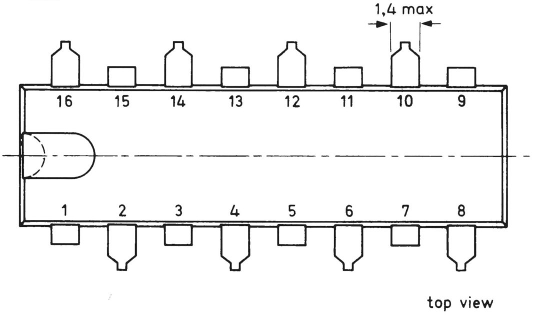
### 3. Repairing soldered joints

The same precautions and limits apply as in (1) above.

# 16-LEAD QUADRUPLE IN-LINE; PLASTIC (SOT-58)


22 max
seating plane
4,7
max
0,7
min
0,76 (2)
3,65
3,20
14x
2,54
0,53
max
0,254 Ⓜ (1)
2,2
max


8,25 max
0,32
max
5,08
10,16
7Z55830.3


1,4 max
16
15
14
13
12
11
10
9
1
2
3
4
5
6
7
8
top view

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

**Dimensions in mm**

## SOLDERING

### 1. By hand

Apply the soldering iron below the seating plane (or not more than 2 mm above it).
If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

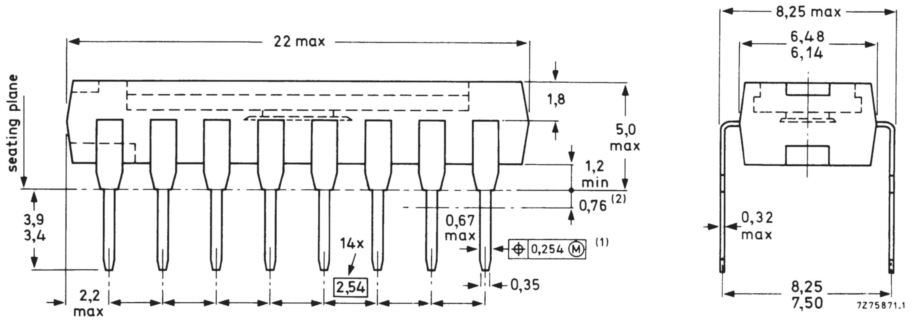
### 2. By dip or wave

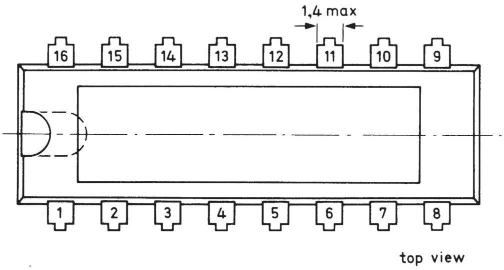
The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.
The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

### 3. Repairing soldered joints

The same precautions and limits apply as in (1) above.

# 16-LEAD DUAL IN-LINE; PLASTIC POWER (SOT-69C)


22 max
seating plane
1,8
5,0
max
1,2
min
0,76 (2)
0,67
max
14x
2,54
0,254 M (1)
0,35
3,9
3,4
2,2
max
8,25 max
6,48
6,14
0,32
max
8,25
7,50
7Z75871.1


1,4 max
16
15
14
13
12
11
10
9
1
2
3
4
5
6
7
8
top view

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

**Dimensions in mm**

## SOLDERING

### 1. By hand

Apply the soldering iron below the seating plane (or not more than 2 mm above it).
If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

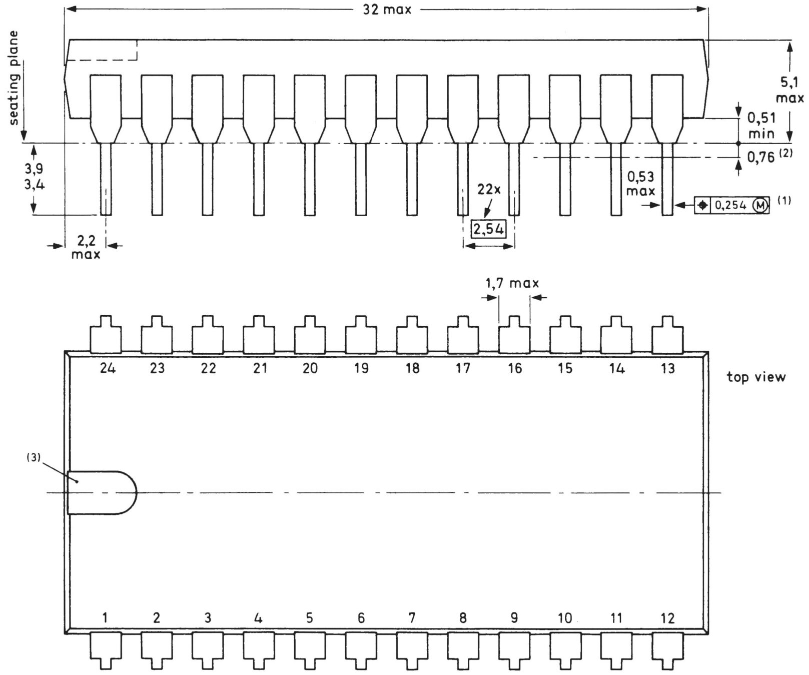
### 2. By dip or wave

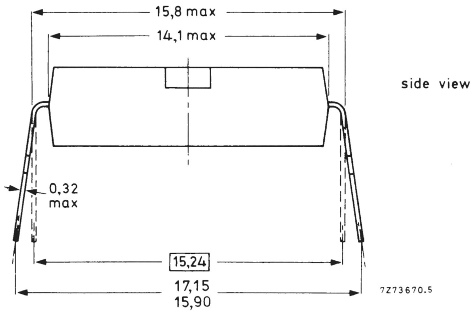
The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.
The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

### 3. Repairing soldered joints

The same precautions and limits apply as in (1) above.

# 24-LEAD DUAL IN-LINE; PLASTIC (WITH INTERNAL HEAT SPREADER) (SOT-101A, B)


32 max
seating plane
5,1 max
0,51 min
0,76 (2)
3,9
3,4
0,53 max
22x
2,54
0,254 M (1)
2,2 max
1,7 max
24 23 22 21 20 19 18 17 16 15 14 13
top view
(3)
1 2 3 4 5 6 7 8 9 10 11 12


15,8 max
14,1 max
side view
0,32 max
15,24
17,15
15,90
7Z73670.5

⌖ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

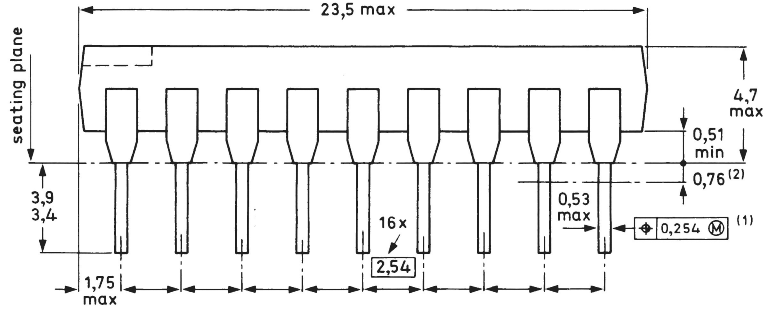
(3) Index may be horizontal as shown, or vertical.

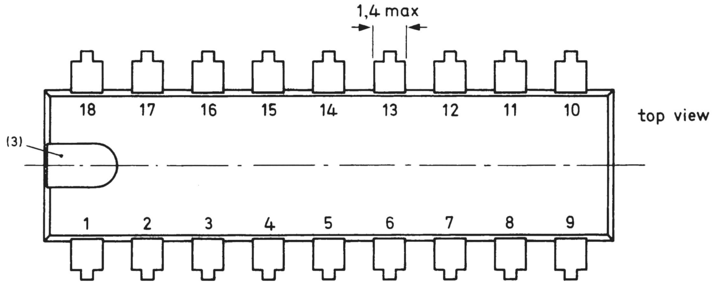
**Dimensions in mm**

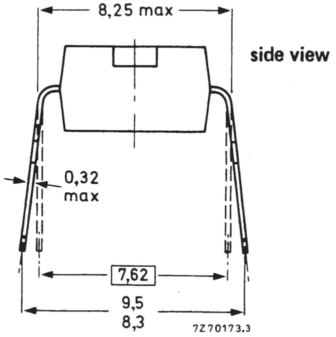
## SOLDERING

See page 5 of this chapter (SOT-38).

# 18-LEAD DUAL IN-LINE; PLASTIC (SOT-102A)


23,5 max
seating plane
4,7
max
0,51
min
0,76 (2)
3,9
3,4
0,53
max
16 x
2,54
0,254 Ⓜ
(1)
1,75
max


1,4 max
18
17
16
15
14
13
12
11
10
top view
(3)
1
2
3
4
5
6
7
8
9


8,25 max
side view
0,32
max
7,62
9,5
8,3
7Z70173.3

⌖ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

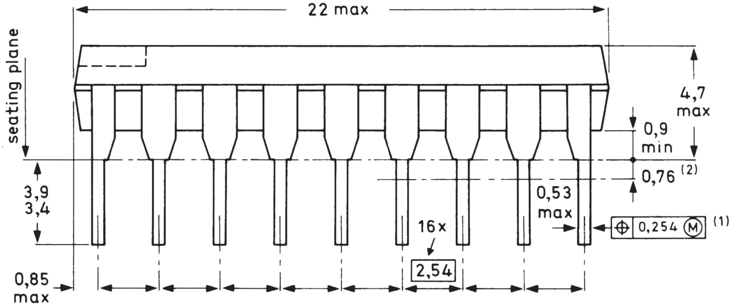
(3) Index may be horizontal as shown, or vertical.

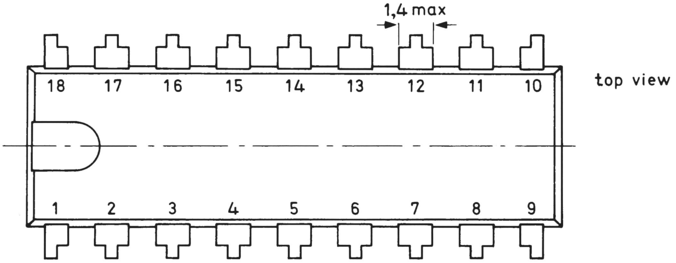
**Dimensions in mm**

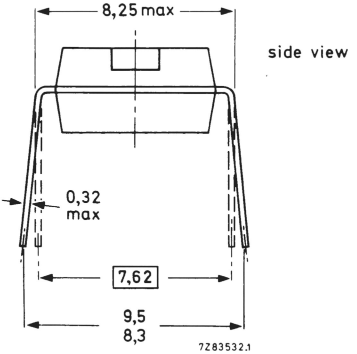
## SOLDERING

See page 5 of this chapter (SOT-38).

# 18-LEAD DUAL IN-LINE; PLASTIC (SOT-102CS)


22 max
seating plane
4,7
max
0,9
min
0,76 (2)
3,9
3,4
0,53
max
16x
2,54
⊕ 0,254 Ⓜ (1)
0,85
max


1,4 max
18
17
16
15
14
13
12
11
10
top view
1
2
3
4
5
6
7
8
9


8,25 max
side view
0,32
max
7,62
9,5
8,3
7Z83532.1

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

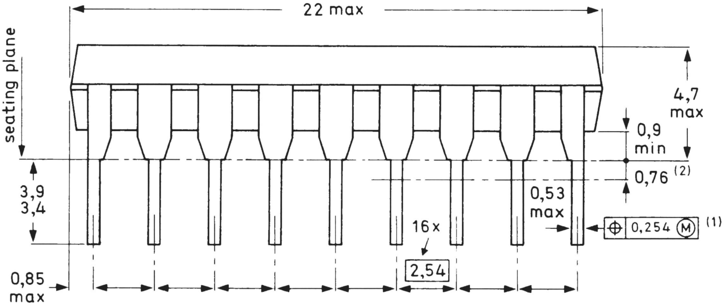
(2) Lead spacing tolerances apply from seating plane to the line indicated.

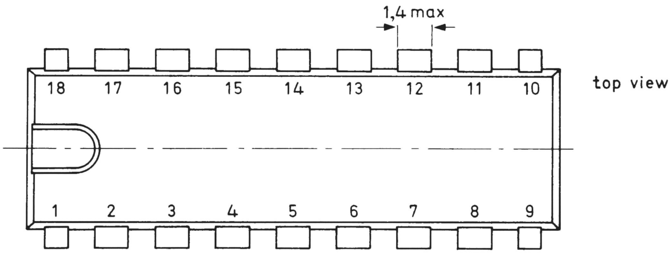
**Dimensions in mm**

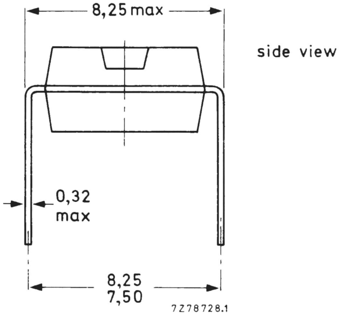
**SOLDERING**

See page 5 of this chapter (SOT-38).

# 18-LEAD DUAL IN-LINE; PLASTIC (SOT-102DS)


22 max
seating plane
4,7
max
0,9
min
0,76 (2)
3,9
3,4
0,53
max
16x
2,54
0,254 Ⓜ (1)
0,85
max


1,4 max
18
17
16
15
14
13
12
11
10
top view
1
2
3
4
5
6
7
8
9


8,25 max
side view
0,32
max
8,25
7,50
7Z78728.1

⌖ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

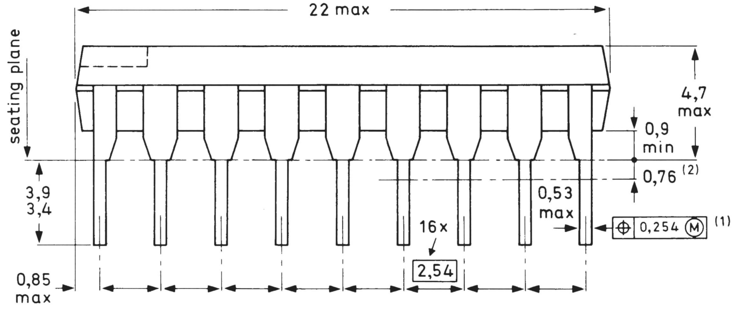
(2) Lead spacing tolerances apply from seating plane to the line indicated.

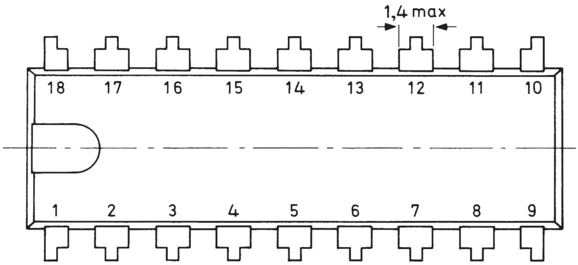
**Dimensions in mm**

## SOLDERING

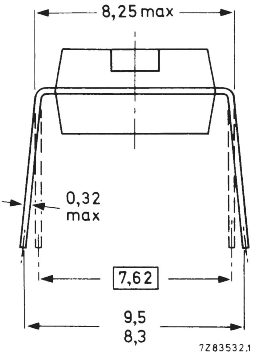
See page 5 of this chapter (SOT-38).

# 18-LEAD DUAL IN-LINE; PLASTIC (SOT-102HE)


22 max
seating plane
4,7
max
0,9
min
0,76 (2)
3,9
3,4
0,53
max
⊕ 0,254 Ⓜ (1)
16x
2,54
0,85
max


1,4 max
18
17
16
15
14
13
12
11
10
1
2
3
4
5
6
7
8
9

top view


8,25 max
0,32
max
7,62
9,5
8,3
7Z83532.1

side view

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

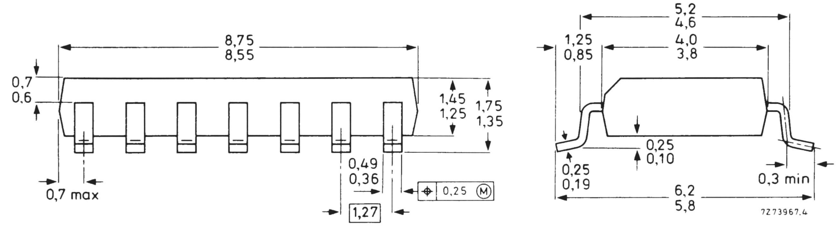
(2) Lead spacing tolerances apply from seating plane to the line indicated.

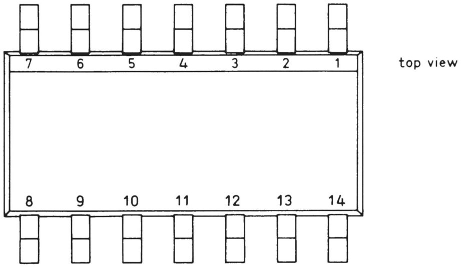
**Dimensions in mm**

## SOLDERING

See page 5 of this chapter (SOT-38).

# 14-LEAD MINI-PACK; PLASTIC (SO-14; SOT-108A)





**Dimensions in mm**

⌖ Positional accuracy.

Ⓜ Maximum Material Condition.

## SOLDERING

### The reflow solder technique

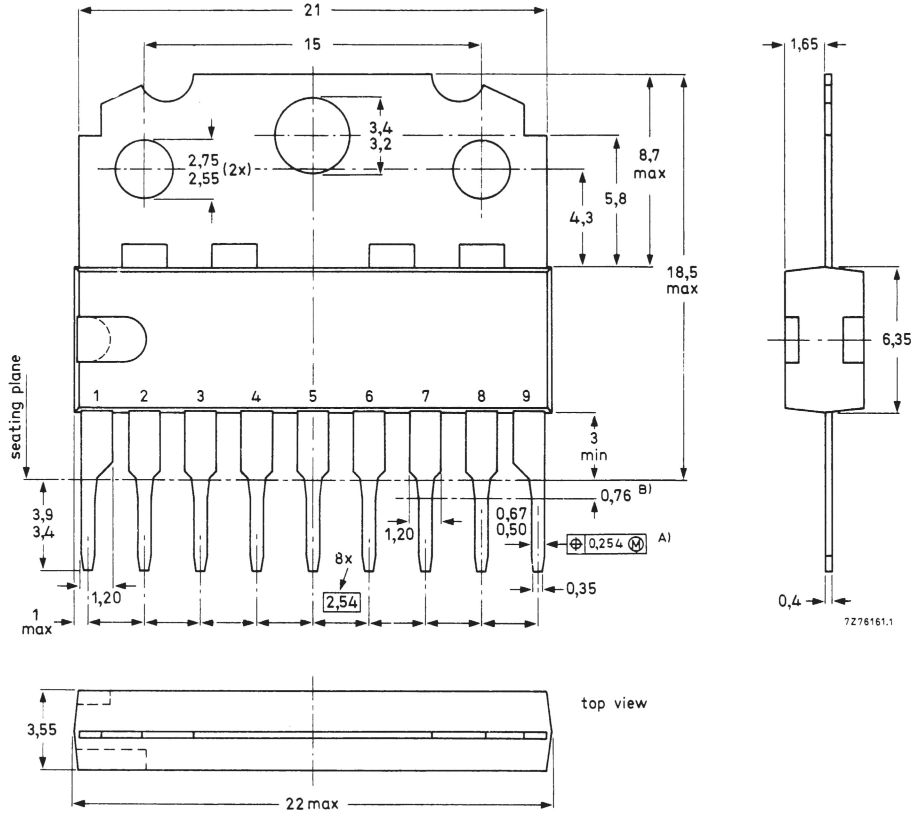
The preferred technique for mounting miniature components on hybrid thick or thin-film circuits is reflow soldering. Solder is applied to the required areas on the substrate by dipping in a solder bath or, more usually, by screen printing a solder paste. Components are put in place and the solder is reflowed by heating.

Solder pastes consist of very finely powdered solder and flux suspended in an organic liquid binder. They are available in various forms depending on the specification of the solder and the type of binder used. For hybrid circuit use, a tin-lead solder with 2 to 4% silver is recommended. The working temperature of this paste is about 220 to 230 °C when a mild flux is used.

For printing the paste onto the substrate a stainless steel screen with a mesh of 80 to 105 $\mu$m is used for which the emulsion thickness should be about 50 $\mu$m. To ensure that sufficient solder paste is applied to the substrate, the screen aperture should be slightly larger than the corresponding contact area.

The contact pins are positioned on the substrate, the slight adhesive force of the solder paste being sufficient to keep them in place. The substrate is heated to the solder working temperature preferably by means of a controlled hot plate. The soldering process should be kept as short as possible: 10 to 15 seconds is sufficient to ensure good solder joints and evaporation of the binder fluid.
After soldering, the substrate must be cleaned of any remaining flux.

# 9-LEAD SINGLE IN-LINE; PLASTIC (SOT-110B)


21
15
1,65
3,4
3,2
2,75
2,55
(2x)
8,7
max
5,8
4,3
18,5
max
6,35
seating plane
1
2
3
4
5
6
7
8
9
3
min
0,76 B)
3,9
3,4
0,67
0,50
1,20
8x
2,54
0,254 Ⓜ
A)
0,35
1,20
1
max
0,4
7Z76161.1
3,55
top view
22 max

**Dimensions in mm**

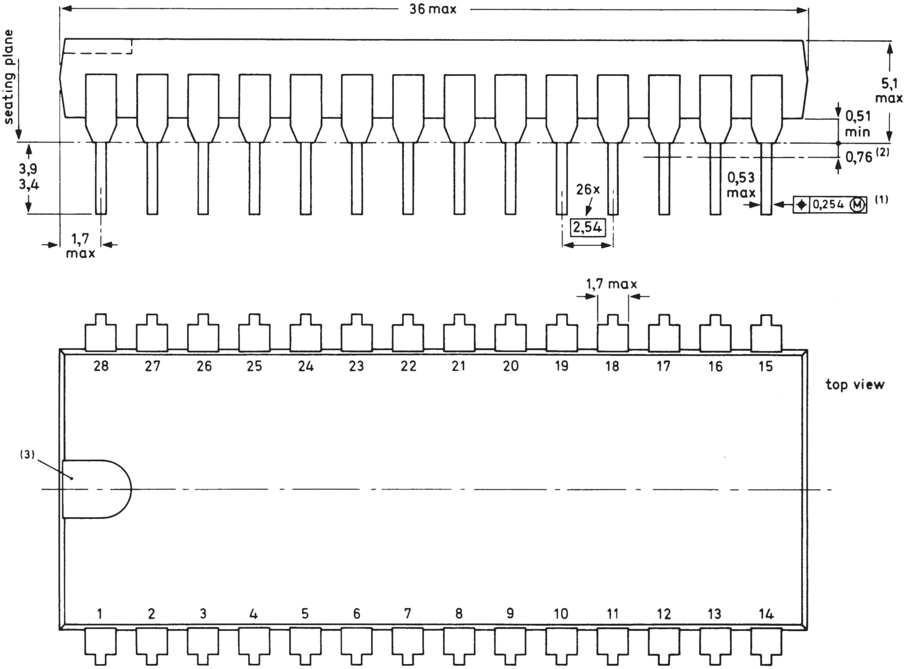
⊕ Positional accuracy.

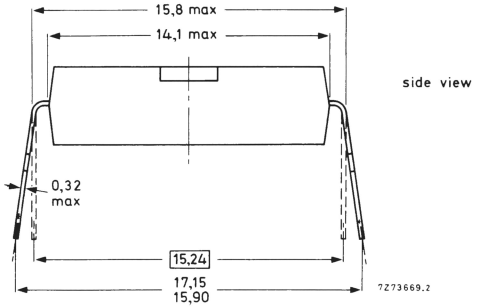
Ⓜ Maximum Material Condition.

A Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

B Lead spacing tolerances apply from seating plane to the line indicated.

# 28-LEAD DUAL IN-LINE; PLASTIC (WITH INTERNAL HEAT SPREADER) (SOT-117)


36 max
seating plane
5,1
max
0,51
min
0,76 (2)
3,9
3,4
0,53
max
26x
2,54
0,254 Ⓜ (1)
1,7
max
1,7 max
28
27
26
25
24
23
22
21
20
19
18
17
16
15
top view
(3)
1
2
3
4
5
6
7
8
9
10
11
12
13
14


15,8 max
14,1 max
side view
0,32
max
15,24
17,15
15,90
7Z73669.2

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

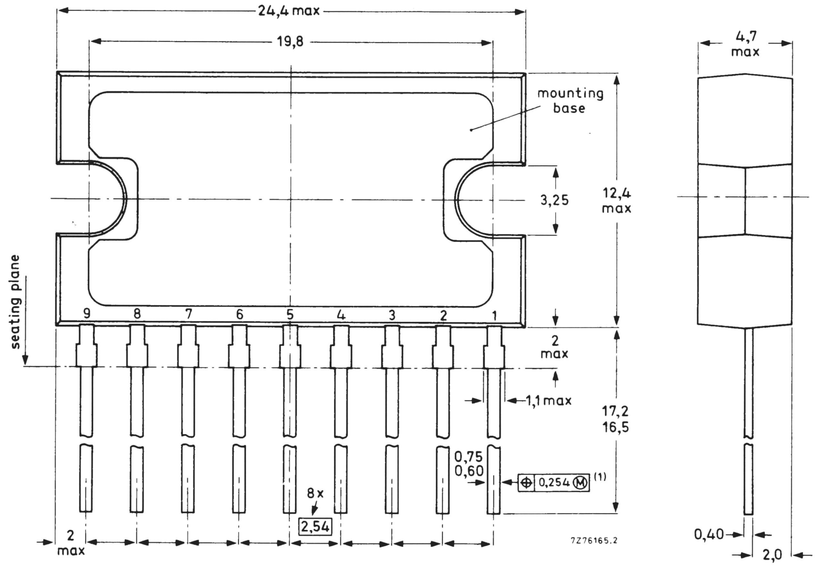
(3) Index may be horizontal as shown, or vertical.

**Dimensions in mm**

## SOLDERING

See page 5 of this chapter (SOT-38).

# 9-LEAD SINGLE IN-LINE; PLASTIC POWER (SOT-131A, B)


24,4 max
19,8
mounting base
3,25
12,4 max
seating plane
9
8
7
6
5
4
3
2
1
2 max
1,1 max
17,2
16,5
0,75
0,60
0,254 Ⓜ
(1)
8x
2,54
2 max
7Z76165.2
4,7 max
0,40
2,0

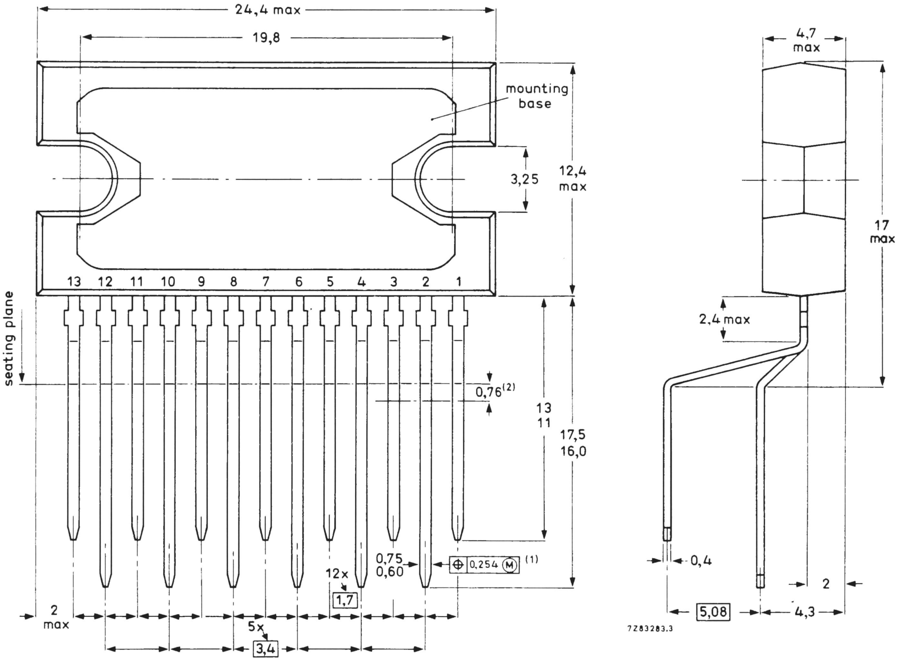
**Dimensions in mm**

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

# 13-LEAD SIL-BENT-TO-DIL; PLASTIC POWER (SOT-141B)


24,4 max
19,8
mounting base
3,25
12,4 max
13 12 11 10 9 8 7 6 5 4 3 2 1
seating plane
0,76(2)
13
11
17,5
16,0
0,75
0,60
12x
1,7
0,254 M (1)
2 max
5x
3,4
4,7 max
17 max
2,4 max
0,4
2
5,08
4,3
7Z83283.3

**Dimensions in mm**

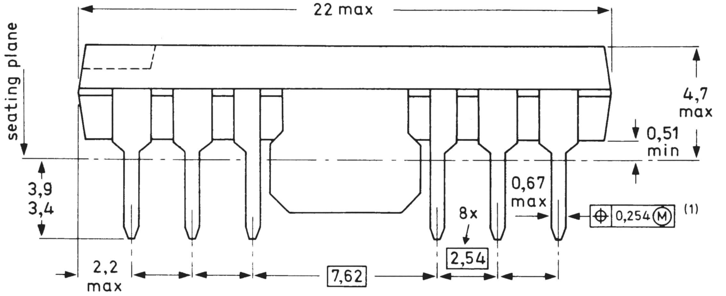
⊕ Positional accuracy.

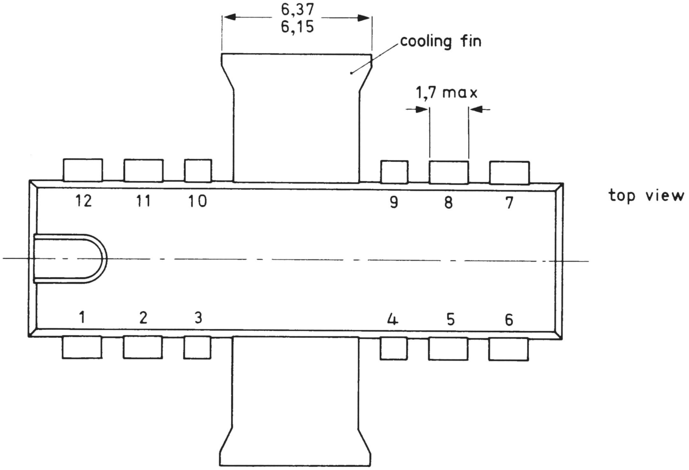
Ⓜ Maximum Material Condition.

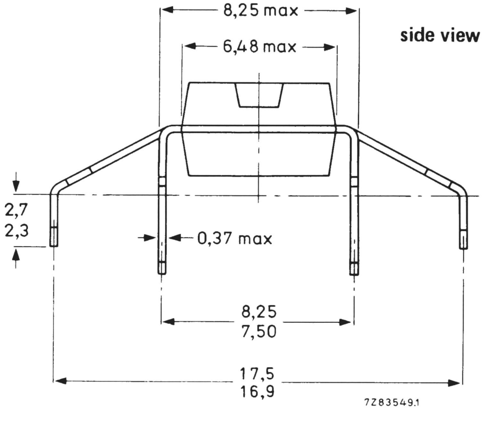
(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

# 12-LEAD DUAL IN-LINE; PLASTIC WITH METAL COOLING FIN (SOT-150)


22 max
seating plane
4,7
max
0,51
min
3,9
3,4
0,67
max
8x
0,254 M
(1)
2,2
max
7,62
2,54


6,37
6,15
cooling fin
1,7 max
12
11
10
9
8
7
top view
1
2
3
4
5
6


8,25 max
6,48 max
side view
2,7
2,3
0,37 max
8,25
7,50
17,5
16,9
7Z83549.1

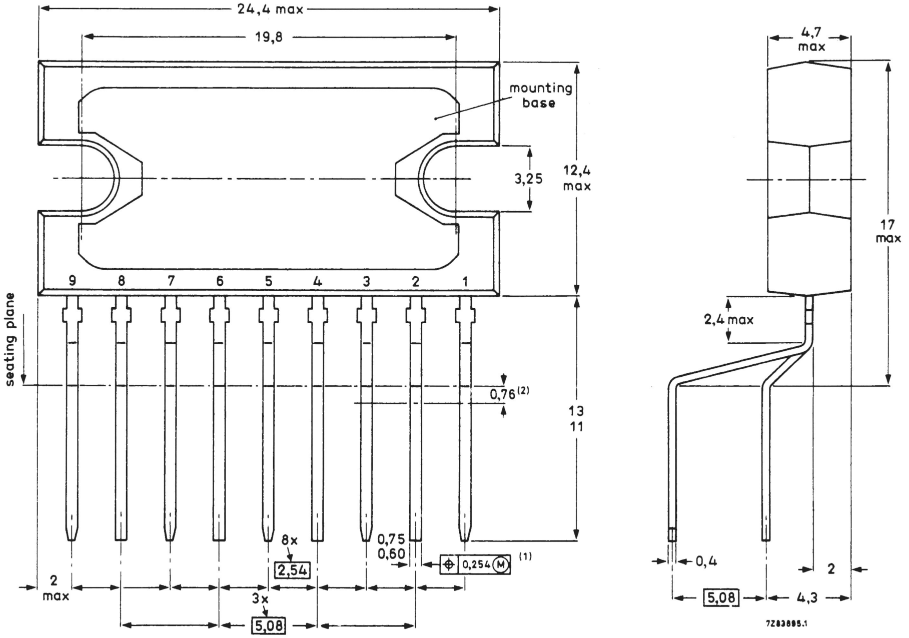
**Dimensions in mm**

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

# 9-LEAD SIL-BENT-TO-DIL; PLASTIC POWER (SOT-157B)


24,4 max
19,8
mounting
base
3,25
12,4
max
9
8
7
6
5
4
3
2
1
seating plane
0,76 (2)
13
11
8x
2,54
0,75
0,60
0,254 M
(1)
2
max
3x
5,08
4,7
max
17
max
2,4 max
0,4
2
5,08
4,3
7Z83895.1

**Dimensions in mm**

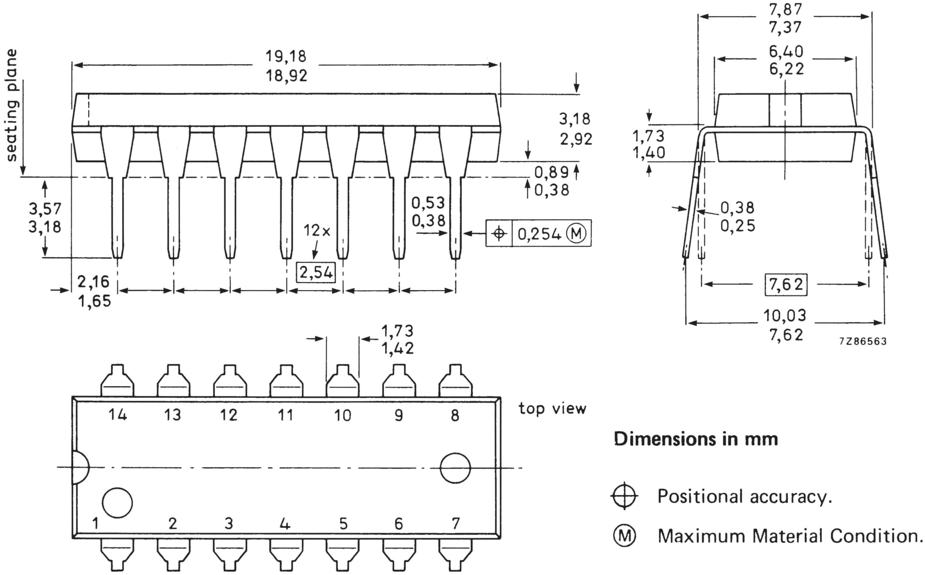
⌖ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

# 14-LEAD DUAL IN-LINE; PLASTIC (VO-36)


seating plane
19,18
18,92
3,18
2,92
0,89
0,38
3,57
3,18
0,53
0,38
12×
2,54
0,254 Ⓜ
2,16
1,65
1,73
1,42
7,87
7,37
6,40
6,22
1,73
1,40
0,38
0,25
7,62
10,03
7,62
7Z86563
14
13
12
11
10
9
8
1
2
3
4
5
6
7
top view

**Dimensions in mm**

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

## SOLDERING

### 1. By hand

Apply the soldering iron below the seating plane (or not more than 2 mm above it).
If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

### 2. By dip or wave

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.
The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

### 3. Repairing soldered joints

The same precautions and limits apply as in (1) above.

# DEVICE DATA

# TELETEXT VIDEO PROCESSOR

The SAA5030 is a monolithic bipolar integrated circuit used for teletext video processing. It is one of a package of four circuits to be used in teletext tv data systems. The SAA5030 extracts data and data clock information from the television composite video signal and feeds this to the Acquisition and Control circuit SAA5040. A 6 MHz crystal controlled phase locked oscillator is incorporated which drives the Timing Chain circuit SAA5020. An adaptive sync separator is also provided which derives line and field sync pulses from the input video in order to synchronise the timing chain.

## QUICK REFERENCE DATA

| | | | | |
|---|---|---|---|---|
| Supply voltage | $V_{CC}$ | nom. | 12 | V |
| Supply current ($V_{CC}$ = 12 V) | $I_{CC}$ | typ. | 110 | mA |
| Video input amplitude (sync-white) | $V_{16video(p-p)}$ | nom. | 2.4 | V |
| Teletext data input amplitude | $V_{16teletext(p-p)}$ | nom. | 1.1 | V |
| Sync amplitude | $V_{16sync(p-p)}$ | nom. | 0.7 | V |
| Operating ambient temperature range | $T_{amb}$ | | −20 to +70 | °C |

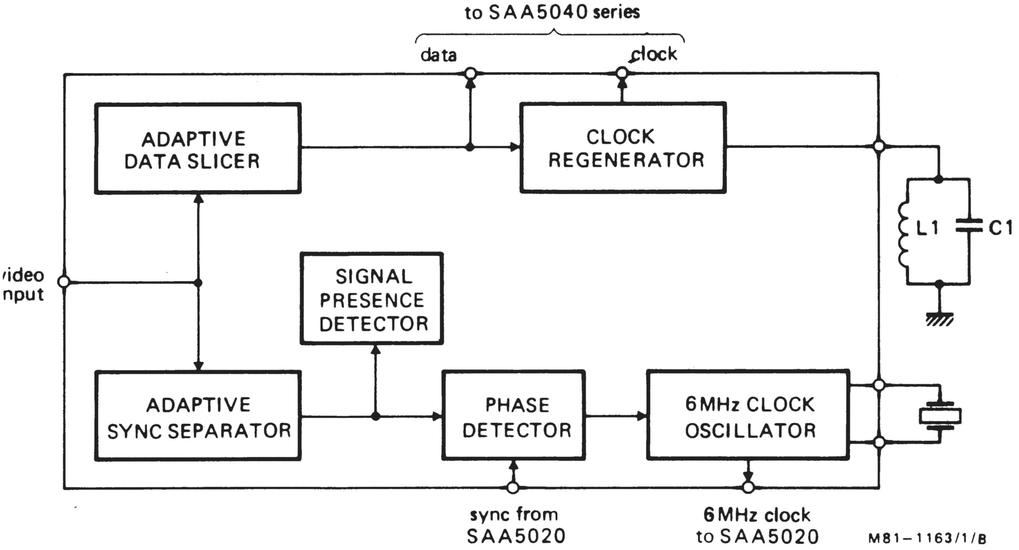

to SAA5040 series
data
clock
ADAPTIVE DATA SLICER
CLOCK REGENERATOR
L1
C1
ideo
nput
SIGNAL PRESENCE DETECTOR
ADAPTIVE SYNC SEPARATOR
PHASE DETECTOR
6 MHz CLOCK OSCILLATOR
sync from SAA5020
6 MHz clock to SAA5020
M81-1163/1/B

Fig.1 Block diagram

## PACKAGE OUTLINE

24-lead DIL; plastic (SOT–101A with internal heat spreader).

## PINNING

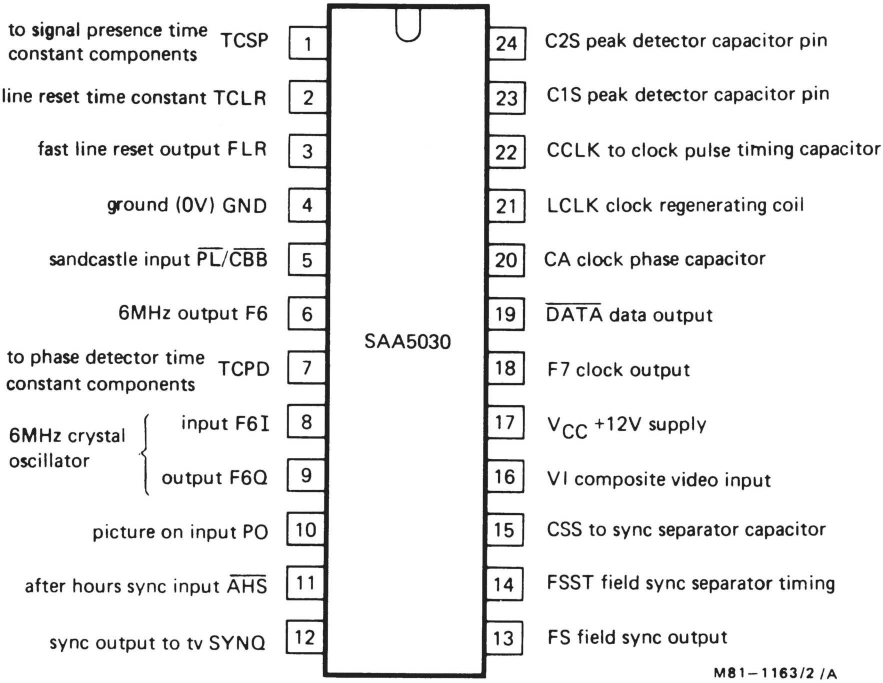

to signal presence time constant components TCSP 1
line reset time constant TCLR 2
fast line reset output FLR 3
ground (0V) GND 4
sandcastle input $\overline{PL}/\overline{CBB}$ 5
6MHz output F6 6
to phase detector time constant components TCPD 7
6MHz crystal oscillator
input F6I 8
output F6Q 9
picture on input PO 10
after hours sync input $\overline{AHS}$ 11
sync output to tv SYNQ 12
SAA5030
24 C2S peak detector capacitor pin
23 C1S peak detector capacitor pin
22 CCLK to clock pulse timing capacitor
21 LCLK clock regenerating coil
20 CA clock phase capacitor
19 $\overline{DATA}$ data output
18 F7 clock output
17 $V_{CC}$ +12V supply
16 VI composite video input
15 CSS to sync separator capacitor
14 FSST field sync separator timing
13 FS field sync output
M81–1163/2 /A

Fig.2 Pinning diagram

**RATINGS** Limiting values in accordance with the Absolute Maximum System. (IEC134)

**Voltages**

| | | | | | |
|---|---|---|---|---|---|
| Supply voltage | $V_{17\text{-}4}$ | $V_{CC}$ | max. | 13.2 | V |
| Input voltages | $V_{5\text{-}4}$ | $V_I$ | max. | 9.0 | V |
| | $V_{10\text{-}4}$ | $V_I$ | max. | $V_{CC}$ | V |
| | $V_{11\text{-}4}$ | $V_I$ | max. | 7.5 | V |

**Temperatures**

| | | | |
|---|---|---|---|
| Storage temperature range | $T_{stg}$ | −20 to +125 | °C |
| Operating ambient temperature range | $T_{amb}$ | −20 to +70 | °C |

**CHARACTERISTICS** (At $T_{amb}$ = 25 °C, $V_{CC}$ = 12 V and with external components as shown in Fig.3 unless otherwise stated).

| | | min. | typ. | max. | |
|---|---|---|---|---|---|
| Supply voltage | $V_{CC}$ | 10.8 | 12.0 | 13.2 | V |
| Supply current ($V_{CC}$ = 12.0 V) | $I_{CC}$ | – | 110 | – | mA |
| **Video input and sync separator** | | | | | |
| Video input amplitude (sync to white) Fig.4 | $V_{16video(p\text{-}p)}$ | 2.0 | 1.4 | 3.0 | V |
| Source impedance, f = 100 kHz | $\|Z_s\|$ | – | – | 250 | Ω |
| Sync amplitude | $V_{16sync(p\text{-}p)}$ | 0.07 | 0.7 | 1.0 | V |
| Delay through sync separator | $t_d$ | – | 0.5 | – | µs |
| Delay between field sync datum at pin 12 and the leading edge of separated field sync at pin 13 (Note 1, Fig.4) | $t_d$ | 32 | 48 | 62 | µs |
| Field sync output | | | | | |
| $V_O$ (LOW) ($I_{13}$ = 20 µA) | $V_{OL}$ | – | – | 0.5 | V |
| $V_O$ (HIGH) ($-I_{13}$ = 100 µA) | $V_{OH}$ | 2.4 | – | – | V |

**Crystal controlled phase-locked oscillator**

Measured using a crystal with the following specification e.g. catalogue number 4322 143 03241

$C_1$ = 27.5 fF (typ.)
$C_0$ = 6.8 pF (typ.)
$C_L$ = 20 pF

| | | |
|---|---|---|
| Trimability ($C_L$ increased to 30 pF) | > | 750 Hz |
| Fundamental ESR | < | 50 Ω |

| | | min. | typ. | max. | |
|---|---|---|---|---|---|
| Frequency | $f_{F6}$ | – | 6.0 | – | MHz |
| Holding range | | 1.5 | 3.0 | – | kHz |
| Catching range | | 1.5 | 3.0 | – | kHz |
| Control sensitivity of phase detector measured as voltage at pin 7 with respect to phase difference between separated syncs and phase lock pulse $\overline{PL}$ | | – | 0.3 | – | mV/ns |
| Control sensitivity of oscillator measured as change in 6 MHz phase shift from pin 8 to pin 9 with respect to voltage at pin 7 | | – | 2 | – | deg/mV |
| Gain of sustaining amplifier, $V_{9\text{-}8}$ measured with input voltage of 100 $mV_{p\text{-}p}$ and phase detector immobilised | | 2.5 | – | – | V/V |
| Output voltage of 6 MHz signal at pin 6, measured into 20 pF load capacitance; peak-to-peak value | | – | 5.5 | – | V |
| Output rise and fall times at pin 6 into 20 pF load | $t_r$; $t_f$ | – | – | 30 | ns |
| **Data slicer and clock regenerator** | | | | | |
| Teletext data input amplitude, pin 16 (Note 2, Fig.4); peak-to-peak value | | – | 1.1 | – | V |
| Data input amplitude at pin 16 required to enable amplitude gate flip-flop; peak-to-peak value | | – | 0.46 | – | V |
| Attack rate, measured at pins 23 and 24 with a step to pin 16 (positive) | | – | 15 | – | V/μs |
| (negative) | | – | 9 | – | V/μs |

| **Data slicer and clock regenerator** (continued) | | min. | typ. | max. | |
|---|---|---|---|---|---|
| Decay rate, measured at pins 23 and 24 with a step input to pin 16 | | 48 | 100 | 144 | mV/μs |
| Width of clock coil drive pulses from pin 21 when clock amplitude is not being controlled (Note 3) | | – | 40 | – | ns |
| Clock hangover measured at pin 18 as the time the clock coil continues ringing after the end of data (Note 4) | | 20 | – | – | Clock Periods |
| Clock and data output voltages at pins 18 and 19 measured with 20 pF load capacitance; peak-to-peak value | | – | 5.5 | – | V |
| Output rise and fall times at pins 18 and 19 into 20 pF loads | $t_r$; $t_f$ | – | – | 30 | ns |
| **Sandcastle input** | | | | | |
| Sandcastle detector thresholds, pin 5 | | | | | |
| Phase lock pulse (PL) on | | 2 | – | – | V |
| Phase lock pulse off | | – | – | 3 | V |
| Blanking pulse ($\overline{CBB}$) on | | 4.5 | – | – | V |
| Blanking pulse off | | – | – | 5.5 | V |
| **Dual polarity sync buffer** | | | | | |
| After hours sync ($\overline{AHS}$) pulse input pin 11 | | | | | |
| Threshold for $\overline{AHS}$ active | | 1.0 | – | – | V |
| Threshold for $\overline{AHS}$ off | | – | – | 2.0 | V |
| Picture On (PO) input, pin 10 | | | | | |
| Threshold for PO active | | – | – | 2.0 | V |
| Threshold for PO off | | 1.0 | – | – | V |
| Sync output, pin 12 | | | | | |
| $\overline{AHS}$ output with pin 10 $<$ 1 V (Note 5) peak-to-peak value | | – | 0.7 | – | V |
| Composite sync output with pin 10 $>$ 2 V (Notes 5 and 6); peak-to-peak value | | – | 0.7 | 1.0 | V |
| Output current | | – | – | 3 | mA |
| **Line reset and signal presence detectors** | | | | | |
| Schmitt trigger threshold on pin 2 to inhibit line reset output at pin 3 (syncs coincident) | | – | 6.2 | – | V |
| Schmitt trigger threshold on pin 2 to permit line reset output at pin 3 (syncs non-coincident) | | – | 7.8 | – | V |
| Line reset output $V_{OL}$ ($I_3$ = 20 μA) | | – | – | 0.5 | V |
| Line reset output $V_{OH}$ ($-I_3$ = 100 μA) | | 2.4 | – | – | V |
| Signal presence Schmitt trigger threshold on pin 2 below which the circuit accepts the input signal | | – | 6.0 | – | V |
| Signal presence Schmitt trigger threshold on pin 2 above which the input signal is rejected. | | – | 6.3 | – | V |

Notes

1. This is measured with the dual polarity buffer external resistor connected to give negative-going syncs. The measurement is made after adjustment of the potential divider at pin 14 for optimum delay.
2. The teletext data input contains binary elements as a two level NRZ signal shaped by a raised cosine filter. The bit rate is 6.9375 M bit/s. The use of odd parity for the 8-bit bytes ensures that there are never more than 14-bit periods between each data transition.
3. This is measured by replacing the clock coil with a small value resistor.
4. This must be measured with the clock coil tuned and using a clock-cracker signal into pin 16. The clock-cracker is a teletext waveform consisting of only one data transition in each byte.
5. With the external resistor connected to the ground rail, syncs are positive-going centred on +2.3 V. With the resistor connected to the supply rail, syncs are negative-going centred on +9.7 V.
6. When the composite sync is being delivered, the level is substantially the same as that at the video input.

## APPLICATION DATA

**The function is quoted against the corresponding pin number**

Pin No.

1. **Signal presence time constant**

   A capacitor and a resistor connected in parallel between this pin and supply determine the delay in operation of the signal presence detector.

2. **Line reset time constant**

   A capacitor between this pin and supply integrates current pulses from the coincidence detector; the resultant level is used to determine whether to allow FLR pulses (see pin 3).

3. **Fast line reset output (FLR)**

   Positive-going sync pulses are produced at this output if the coincidence detector shows no coincidence between the syncs separated from the incoming video and the $\overline{\text{CBB}}$ waveform from the timing chain circuit SAA5020. These pulses are sent to the timing chain circuit and are used to reset its counters, so as to effect rapid lock-up of the phase locked loop.

4. **Ground** (0 V)

5. **Sandcastle input ($\overline{\text{PL}}$ and $\overline{\text{CBB}}$)**

   This input accepts a sandcastle waveform which is formed from $\overline{\text{PL}}$ and $\overline{\text{CBB}}$ from the timing chain SAA5020. $\overline{\text{PL}}$ is obtained by slicing the waveform at 2.5 V, and this, together with separated sync, are inputs to the phase detector which forms part of the phase locked loop. When the loop has locked up, the edges of $\overline{\text{PL}}$ are nominally 2 μs before and 2 μs after the leading edge of separated line syncs.
   CBB is obtained by slicing the waveform at 5 V, and is used to prevent the data slicer being offset by the colour burst.

6. **6 MHz output (F6)**

   This is the output of the crystal oscillator (see pins 8 and 9), and is taken to the timing chain circuit SAA5020 via a series capacitor.

7. **Phase detector time constant**

   The integrating components for the phase detector of the phase locked loop are connected between this pin and supply.

APPLICATION DATA (continued)

8, 9. **6 MHz crystal**

A 6 MHz crystal in series with a trimmer capacitor is connected between these pins. It forms part of an oscillator whose frequency is controlled by the voltage on pin 7, which forms part of the phase locked loop.

10. **Picture On input (PO)**

The PO signal from the acquisition and control circuits SAA5040 Series is fed to this input and is used to determine whether the input video (pin 16) or the $\overline{\text{AHS}}$ waveform (pin 11) appears at pin 12.

11. **After hours sync ($\overline{\text{AHS}}$)**

A composite sync waveform $\overline{\text{AHS}}$ is generated in the timing chain circuit SAA5020 and is used to synchronise the tv (see pin 10).

12. **Sync output to tv**

Either the input video of $\overline{\text{AHS}}$ is available at this output dependent on whether the PO signal is HIGH or LOW. In addition either signal may be positive-going or negative-going, dependent on whether the load resistor at this output is connected to ground or supply.

13. **Field sync output (FS)**

A pulse, derived from the input video by the field sync separator, which is used to reset the line counter in the timing chain circuit SAA5020.

14. **Field sync separator timing**

A capacitor and adjusting network is connected to this pin and forms the integrator of the field sync separator.

15. **Sync separator capacitor**

A capacitor connected to this pin forms part of the adaptive sync separator.

16. **Composite video input (VI)**

The composite video is fed to this input via a coupling capacitor.

17. **Supply voltage (+12 V)**

18. **Clock output**

The regenerated clock, after extraction from the teletext data, is fed out to the acquisition and control circuits SAA5040 Series via a series capacitor.

19. **Data output**

The teletext data is sliced off the video waveform, squared up and latched within the SAA5030. The latched output is fed to the acquisition and control circuits SAA5040 Series via a series capacitor.

20. **Clock decoupling**

A 1 nF capacitor between pin 20 and ground is required for clock decoupling.

21. **Clock regenerator coil**

A high-Q parallel tuned circuit is connected between this pin and an external potential divider. The coil is part of the clock regeneration circuit (see pin 22).

APPLICATION DATA (continued)

22. **Clock pulse timing capacitor**

Short pulses are derived from both edges of data with the aid of a capacitor connected to this pin. The resulting pulses are fed, as a current, into the clock coil connected to pin 21. Resulting oscillations are limited and taken to the acquisition and control circuits SAA5040 Series via pin 18.

23, 24 **Peak detector capacitors**

The teletext data is sliced with an automatic data slicer whose slicing level is the mid-point of two peak detectors working on the video signal. Storage capacitors are connected to these pins for the negative and positive peak detectors.

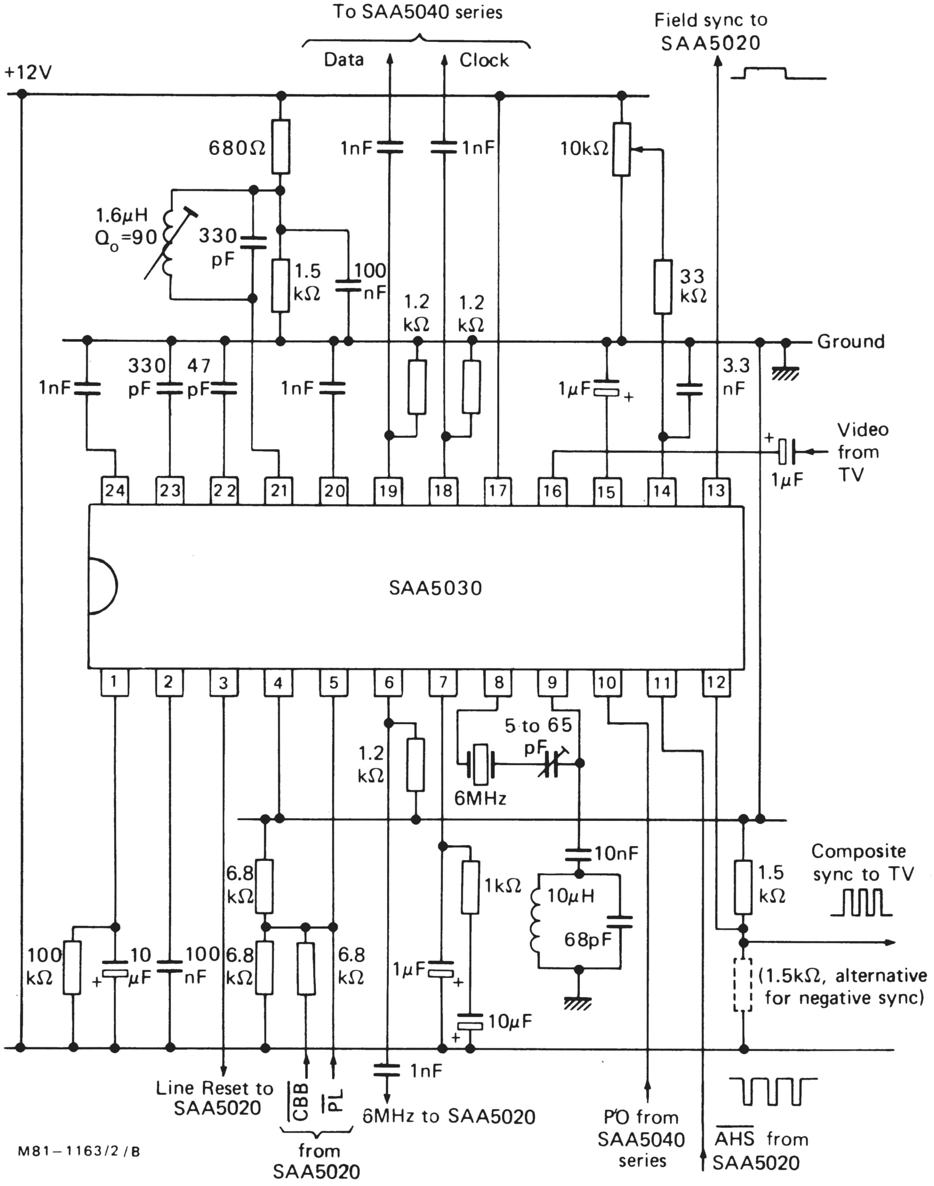

To SAA5040 series
Data
Clock
Field sync to SAA5020
+12V
680Ω
1nF
1nF
10kΩ
1.6μH
Q₀=90
330 pF
1.5 kΩ
100 nF
1.2 kΩ
1.2 kΩ
33 kΩ
Ground
1nF
330 pF
47 pF
1nF
1μF
3.3 nF
Video from TV
1μF
24
23
22
21
20
19
18
17
16
15
14
13
SAA5030
1
2
3
4
5
6
7
8
9
10
11
12
5 to 65 pF
1.2 kΩ
6MHz
10nF
1kΩ
10μH
68pF
6.8 kΩ
6.8 kΩ
6.8 kΩ
100 kΩ
10 μF
100 nF
1μF
10μF
1.5 kΩ
Composite sync to TV
(1.5kΩ, alternative for negative sync)
1nF
Line Reset to SAA5020
CBB
PL
from SAA5020
6MHz to SAA5020
PO from SAA5040 series
AHS from SAA5020
M81–1163/2/B

Fig.3 Peripheral circuit

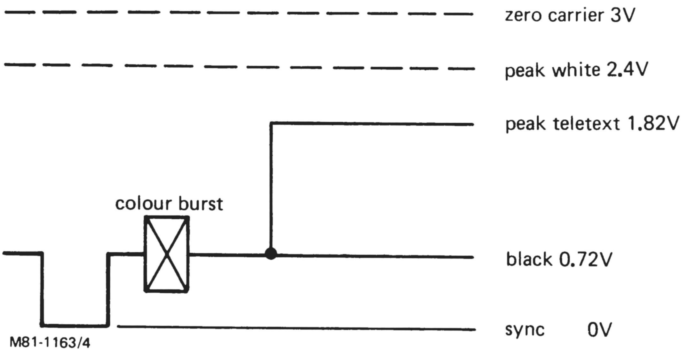

zero carrier 3V
peak white 2.4V
peak teletext 1.82V
colour burst
black 0.72V
sync 0V
M81-1163/4

Fig.4 Part of teletext line, with burst showing nominal levels.

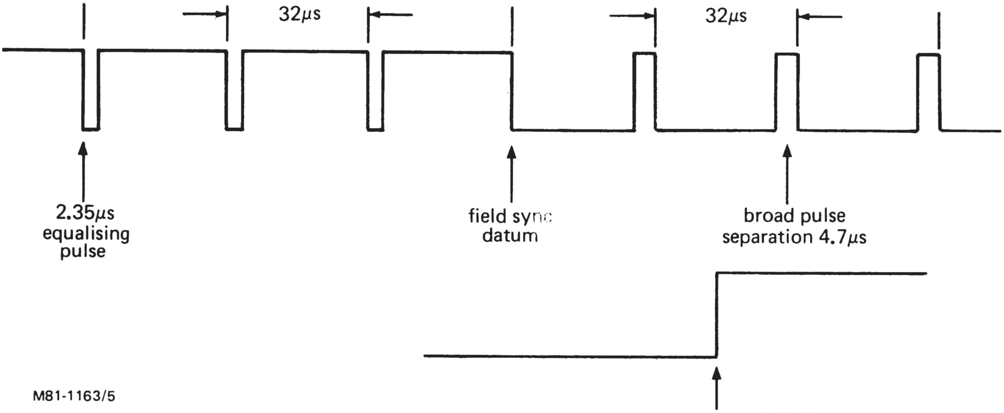

32$\mu$s
32$\mu$s
2.35$\mu$s equalising pulse
field sync datum
broad pulse separation 4.7$\mu$s
leading edge of field sync pulse
M81-1163/5

Fig.5 Detail of idealised composite sync waveform.

# SOUND I.F. AMPLIFIER/DEMODULATOR FOR TV

The TBA120U is an i.f. amplifier with a symmetrical FM demodulator and an a.f. amplifier with adjustable output voltage. The a.f. amplifier is also provided with an output for volume control and an input for VCR operation.

The input and output of the TBA120U are especially designed for LC-circuits, but the input can also be used with a ceramic filter.

## QUICK REFERENCE DATA

| | | | | |
|---|---|---|---|---|
| Supply voltage (pin 11) | $V_P$ | typ. | 12 | V |
| Supply current | $I_P$ | typ. | 13,5 | mA |
| I.F. voltage gain at f = 5,5 MHz | $G_{v\ if}$ | typ. | 68 | dB |
| Input voltage starting limiting | $V_i$ | typ. | 30 | $\mu$V |
| AM suppression at $\Delta f = \pm 50$ kHz | $\alpha$ | typ. | 60 | dB |
| A.F. output voltage adjustment range (pin 8) | $\Delta V_{o\ af}$ | typ. | 85 | dB |
| A.F. output voltage at $\Delta f = \pm 50$ kHz (r.m.s. value) | | | | |
| at pin 8 | $V_{o\ af(rms)}$ | typ. | 1,2 | V |
| at pin 12 | $V_{o\ af(rms)}$ | typ. | 1,0 | V |

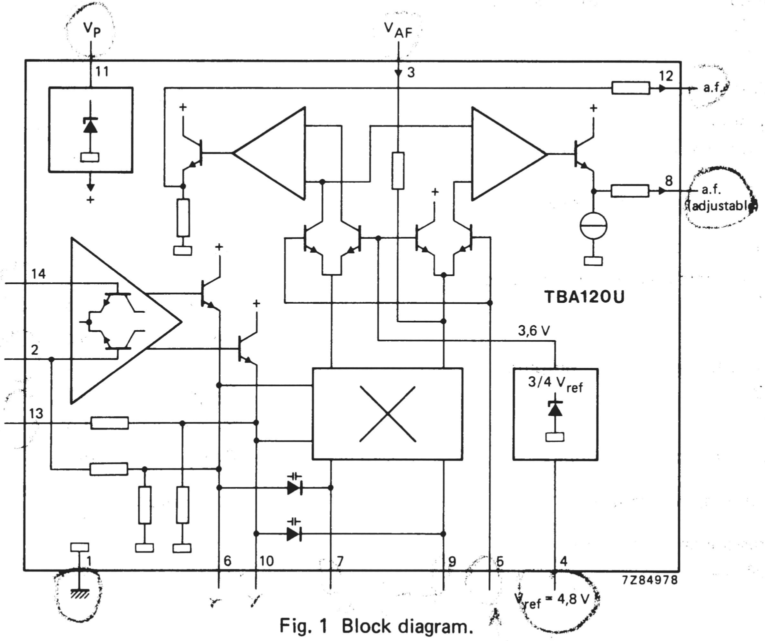


Fig. 1 Block diagram.

## PACKAGE OUTLINE

14-lead DIL; plastic (VO-36).

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | | |
|---|---|---|---|---|
| Supply voltage (pin 11) | $V_P = V_{11\text{-}1}$ | max. | 18 | V* |
| Adjustment voltage (pin 5) | $V_{5\text{-}1}$ | max. | 6 | V |
| Total power dissipation | $P_{tot}$ | max. | 400 | mW |
| By-pass resistance | $R_{13\text{-}14}$ | max. | 1 | kΩ |
| Storage temperature range | $T_{stg}$ | | −40 to + 125 | °C |
| Operating ambient temperature range | $T_{amb}$ | | −15 to + 70 | °C |

## CHARACTERISTICS

$V_P = 12$ V; $T_{amb} = 25$ °C; f = 5,5 MHz

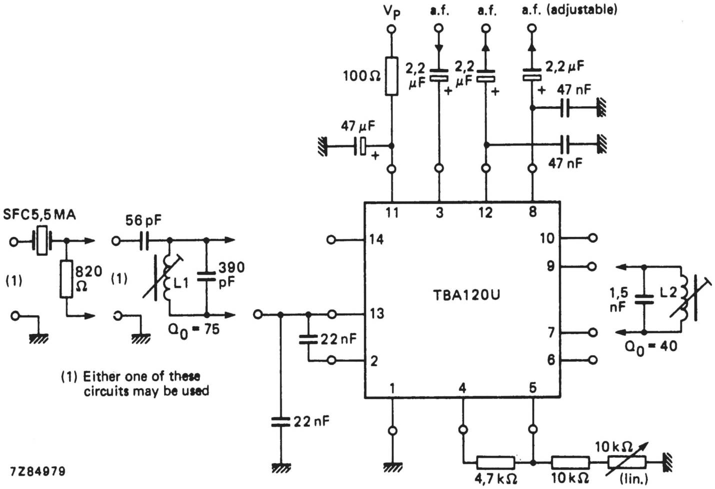
| | | | | |
|---|---|---|---|---|
| I.F. voltage gain | $G_{v\,if\,6\text{-}14}$ | typ. | 68 | dB |
| Input voltage starting limiting at Δf = ± 50 kHz; $f_m = 1$ kHz | $V_i$ | typ.<br>< | 30<br>60 | μV<br>μV |
| I.F. output voltage at limiting (peak-to-peak value) | $V_{o\,if\,(p\text{-}p)}$ | typ. | 250 | mV |
| AM suppression at Δf = ± 50 kHz; $V_i = 500$ μV; $f_m = 1$ kHz; m = 30% | α | ><br>typ. | 50<br>60 | dB<br>dB |
| I.F. residual voltage without de-emphasis | | | | |
| at pin 12 | $V_{if\,12}$ | typ. | 30 | mV |
| at pin 8 | $V_{if\,8}$ | typ. | 20 | mV |
| A.F. voltage gain | $G_{v\,af\,8\text{-}3}$ | typ. | 7,5 | |
| A.F. adjustment at $R_{4\text{-}5} = 5$ kΩ; $R_{5\text{-}1} = 13$ kΩ | $\Delta V_{o\,af}$ | <br>typ. | 20 to 36<br>28 | dB<br>dB |
| A.F. output voltage control range | $\Delta V_{o\,af}$ | ><br>typ. | 70<br>85 | dB<br>dB |
| Adjustment resistor** | $R_{4\text{-}5}$ | | 1 to 10 | kΩ |
| D.C. voltage portion at the a.f. outputs | | | | |
| pin 12 | $V_{12\text{-}1}$ | typ. | 5,6 | V |
| pin 8 | $V_{8\text{-}1}$ | typ. | 4,0 | V |
| Output resistance of the a.f. outputs | | | | |
| pin 12 | $R_{o\,12\text{-}1}$ | typ. | 1,1 | kΩ |
| pin 8 | $R_{o\,8\text{-}1}$ | typ. | 1,1 | kΩ |
| Input resistance of the a.f. input | $R_{i\,3\text{-}1}$ | typ. | 2 | kΩ |
| Stabilized reference voltage | $V_{4\text{-}1} = V_{ref}$ | <br>typ. | 4,2 to 5,3<br>4,8 | V<br>V |
| Source resistance of reference voltage source | $R_{4\text{-}1}$ | typ. | 12 | Ω |

---

* Supply voltage operating range is 10 to 18 V.

** Pin 5 must be connected to pin 4, when volume control adjustment is not applicable.

| | | | | |
|---|---|---|---|---|
| Hum suppression | | | | |
| at pin 12 | $V_{12}/V_{11}$ | typ. | 30 | dB |
| at pin 8 | $V_8/V_{11}$ | typ. | 35 | dB |
| Supply current (pin 11) | $I_P = I_{11}$ | | 9,5 to 17,5 | mA |
| | | typ. | 13,5 | mA |
| I.F. input impedance | $\|Z_i\|$ | typ. | 40 kΩ/4,5 | pF |
| | | > | 15 kΩ/< 6 | pF |
| A.F. output voltage at $\Delta f = \pm 50$ kHz; $f_m = 1$ kHz; $V_i = 10$ mV; $Q_o = 45$; r.m.s. value | | | | |
| at pin 12 | $V_{o\ af\ (rms)}$ | typ. | 1,0 | V |
| at pin 8 | $V_{o\ af\ (rms)}$ | typ. | 1,2 | V |
| Distortion at $\Delta f = \pm 50$ kHz; $f_m = 1$ kHz; $V_i = 10$ mV; $Q_o = 20$ | $d_{tot}$ | typ. | 1 | % |



V_P
a.f.
a.f.
a.f. (adjustable)
100 Ω
2,2 µF
2,2 µF
2,2 µF
47 nF
47 µF
47 nF
11
3
12
8
14
10
9
13
7
2
6
1
4
5
TBA120U
SFC5,5MA
56 pF
820 Ω
(1)
(1)
L1
390 pF
Q0 = 75
22 nF
22 nF
1,5 nF
L2
Q0 = 40
10 kΩ
4,7 kΩ
10 kΩ
(lin.)
(1) Either one of these circuits may be used
7Z84979

Fig. 2 Application example using TBA120U.

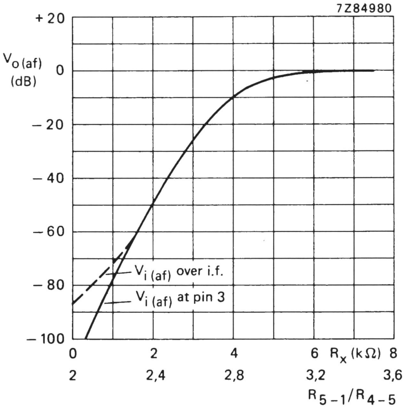


Fig. 3 The a.f. output voltage at pin 8 as a function of the resistance values as shown in Fig. 4.

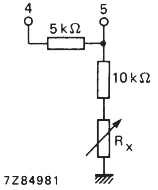
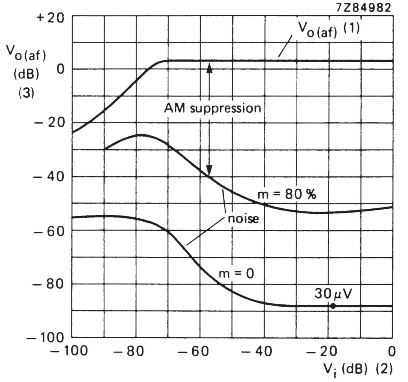


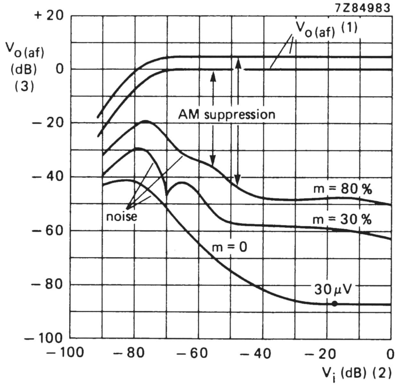
Fig. 4 Resistor conditions for curves in Fig. 3.



(1) $V_{o\ af}$ with de-emphasis at $\Delta f = \pm 50$ kHz; $f_m = 1$ kHz; $d_{tot} = 1{,}5\%$; 0 dB ≙ 770 mV.

(2) $V_i$: 0 dB ≙ 200 mV at 60 Ω.

Fig. 5 The a.f. output voltage at pin 8 as a function of the input voltage with SFC 5,5 MA at the input (see Fig. 2).



(1) $V_{o\ af}$ with de-emphasis at $f_m = 1$ kHz;
0 dB ≙ 770 mV;
curve a: $\Delta f = \pm 50$ kHz; $d_{tot} = 3\%$;
curve b: $\Delta f = \pm 25$ kHz; $d_{tot} = 1\%$.

(2) $V_i$: 0 dB ≙ 200 mV at pin 14.

Fig. 6 The a.f. output voltage at pin 8 as a function of the input voltage with broadband input (60 Ω).

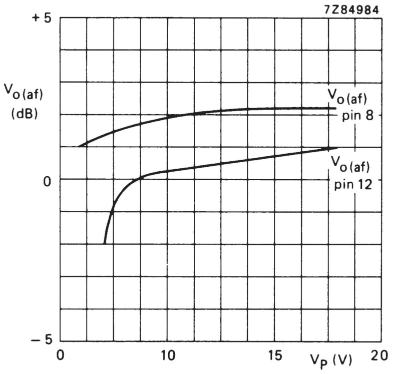


Fig. 7 The a.f. output voltages at pins 8 and 1 as a function of the supply voltage; 0 dB ≙ 770 mV.

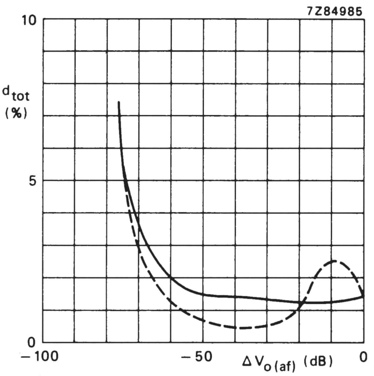


Fig. 8 Total distortion as a function of the a.f. output voltage change.
———— 0 dB ≙ 900 mV over i.f. (pin 8)
– – – – 0 dB ≙ 1,15 V (pin 8)

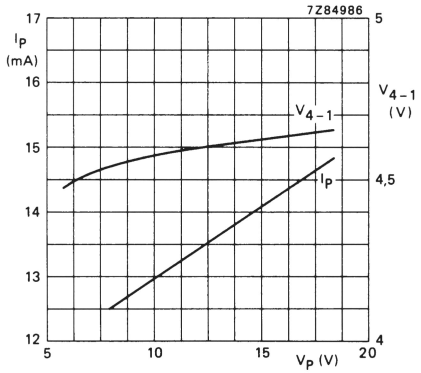


Fig. 9 Supply current and the reference voltage at pin 4 as a function of supply voltage.

# REFERENCE COMBINATION

The TBA540 is an integrated reference oscillator circuit for colour television receivers incorporating an automatic phase and amplitude controlled oscillator employing a quartz crystal, together with a half-line frequency synchronous demodulator circuit. The latter compares the phases and amplitude of the swinging burst ripple and the PAL flip-flop waveform, and generates appropriate a.c.c., colour killer and identification signals. The use of synchronous demodulation for these functions permits a high standard of noise immunity.

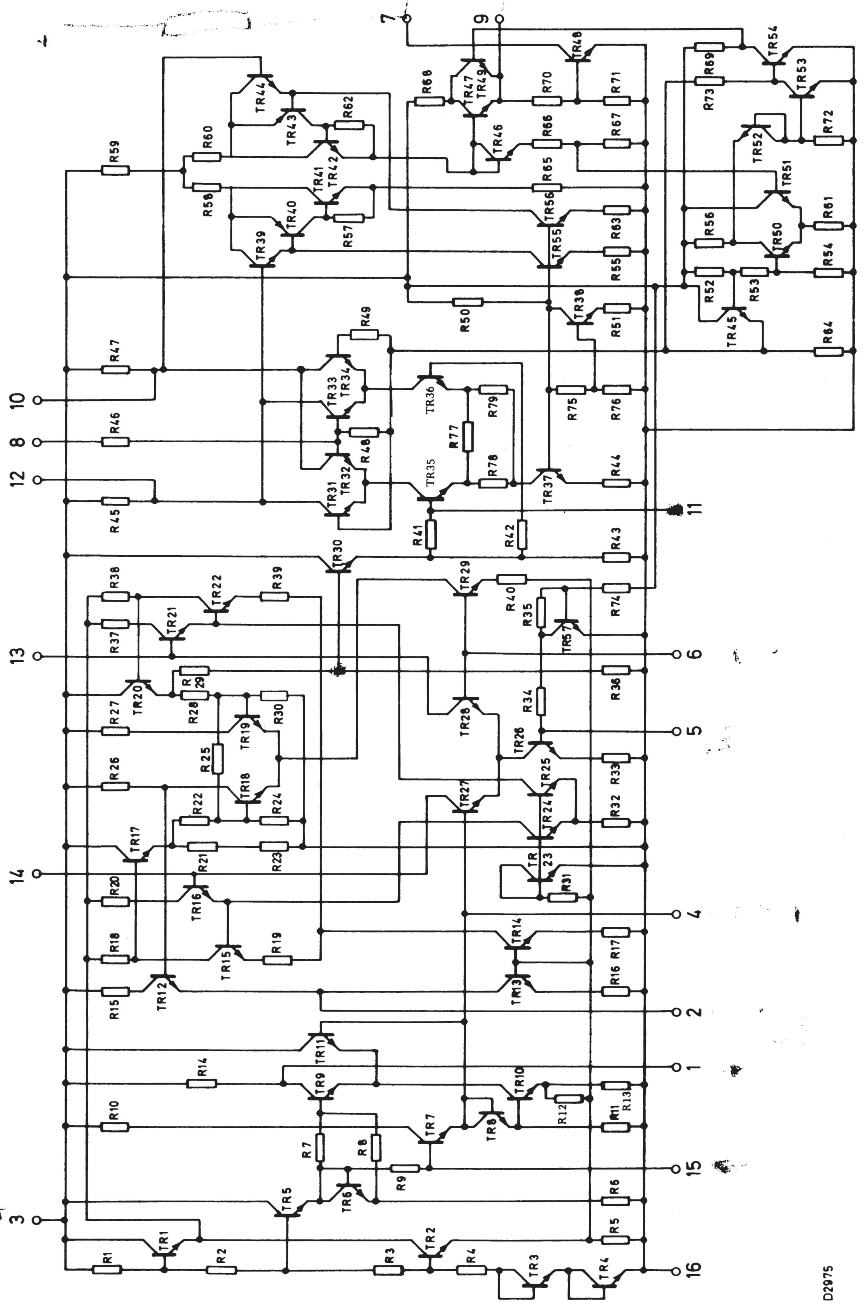
**QUICK REFERENCE DATA**

| | | | | |
|---|---|---|---|---|
| Supply voltage | $V_{3-16}$ | nom. | 12 | V |
| Total current drain | $I_3$ | typ. | 33 | mA |
| R-Y reference signal output<br>peak-to-peak value | $V_{4-16(p-p)}$ | typ. | 1,5 | V |
| Colour killer output: colour on | $V_{7-16}$ | typ. | 12 | V |
| colour off | $V_{7-16}$ | < | 250 | mV |
| A.C.C. output voltage range<br>at correct phase of PAL switch | $V_{9-16}$ | | +4 to +0,2 | V |
| at incorrect phase of PAL switch | $V_{9-16}$ | | +4 to +11 | V |

**PACKAGE OUTLINES**

TBA540 : 16-lead DIL; plastic (SOT-38).
TBA540Q: 16-lead QIL; plastic (SOT-58).

# CIRCUIT DIAGRAM


7
9
10
8
12
13
14
3
+
16
15
1
2
4
5
6
11
D2975

**RATINGS** Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | | |
|---|---|---|---|---|
| Voltage | | | | |
| Supply voltage | $V_{3-16}$ | max. | 13.2 | V |
| Power dissipation | | | | |
| Total power dissipation at $T_{amb}$ = 50 °C | $P_{tot}$ | max. | 680 | mW |
| Temperatures | | | | |
| Storage temperature | $T_{stg}$ | | −55 to +125 | °C |
| Operating ambient temperature | $T_{amb}$ | | −20 to +60 | °C |

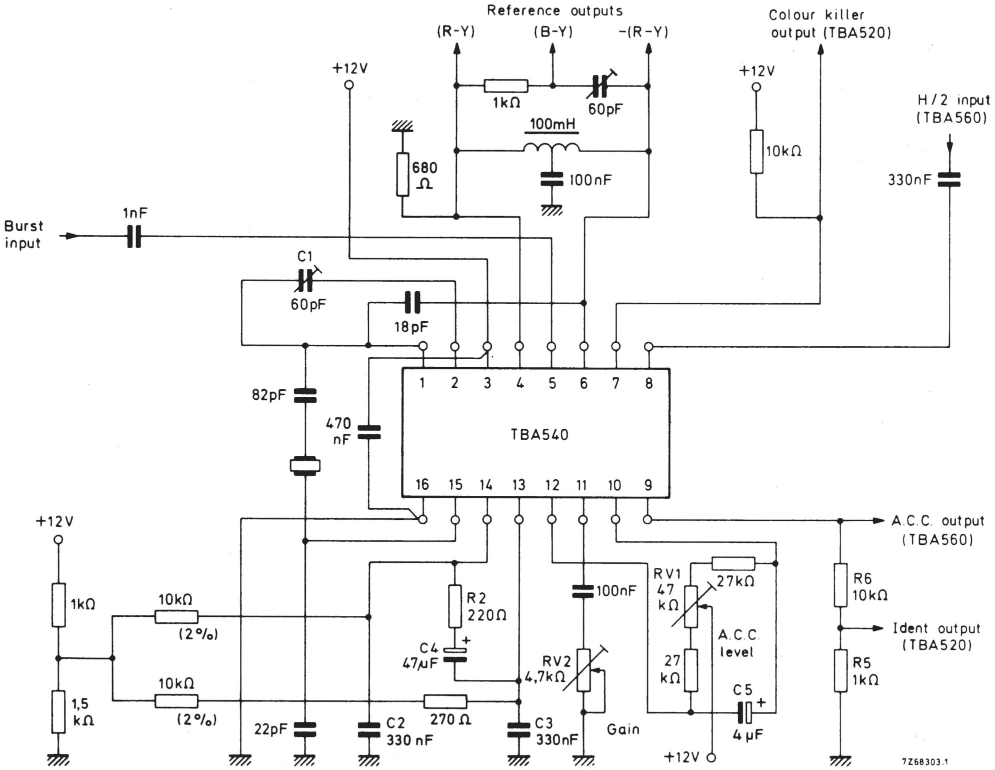
**CHARACTERISTICS** at $V_{3-16}$ = 12 V; $T_{amb}$ = 25 °C; $V_{5-16\,M}$ = 0.7 V (burst signal input); $V_{8-16(p-p)}$ = 2.5 V (P.A.L. square wave input) Measured in circuit shown on page 4.

| | | | | |
|---|---|---|---|---|
| Output signals | | | | |
| R-Y reference signal output peak-to-peak value | $V_{4-16(p-p)}$ | typ. | 1.5 | V |
| Colour killer output: colour on | $V_{7-16}$ | typ. | 12 | V |
| colour off | $V_{7-16}$ | < | 250 | mV |
| A.C.C. output signal range | | | | |
| at correct phase of P.A.L. switch | $V_{9-16}$ | | +4 to +0.2 | V |
| at incorrect phase of P.A.L. switch | $V_{9-16}$ | | +4 to +11 | V |
| Oscillator section (amplifier) | | | | |
| Input resistance | $R_{15-16}$ | typ. | 3.5 | kΩ |
| Input capacitance | $C_{15-16}$ | typ. | 5 | pF |
| Voltage gain | $G_{15-1}$ | typ. | 4.7 | |
| Reactance control section | | | | |
| Voltage gain with pins 13 and 14 interconnected | $G_{15-2}$ | typ. | 1.3 | |
| Rate of change of gain $G_{15-2}$ with phase difference between burst and reference signal | $\frac{\Delta G_{15-2}}{\Delta\varphi_{5-4}}$ | typ. | 5 | $\frac{1}{\text{rad}}$ |
| Supply current consumption | $I_3$ | typ. | 33 | mA |

## PINNING

1. Oscillator feedback output
2. Reactance control stage feedback
3. Supply voltage (12 V)
4. Reference waveform output
5. Burst waveform input
6. Reference waveform input
7. Colour killer output
8. P.A.L. flip-flop square wave input
9. A.C.C. output
10. A.C.C. level setting (see also pin 12)
11. A.C.C. gain setting
12. A.C.C. level setting (see also pin 10)
13. } D.C. control points for
14. } oscillator phase control loop
15. Oscillator feedback input
16. Earth (negative supply)

## APPLICATION INFORMATION


Reference outputs
(R-Y)
(B-Y)
-(R-Y)
Colour killer output (TBA520)
+12V
1kΩ
60pF
100mH
680 Ω
100nF
10kΩ
H/2 input (TBA560)
330nF
Burst input
1nF
C1
60pF
18pF
82pF
470 nF
TBA540
1 2 3 4 5 6 7 8
16 15 14 13 12 11 10 9
A.C.C. output (TBA560)
R6 10kΩ
Ident output (TBA520)
R5 1kΩ
1kΩ
1,5 kΩ
10kΩ (2%)
10kΩ (2%)
R2 220Ω
C4 47µF
RV1 47 kΩ
27kΩ
A.C.C. level
27 kΩ
C5 4µF
RV2 4,7kΩ
Gain
22pF
C2 330 nF
270 Ω
C3 330nF
100nF
+12V
7Z68303.1

**APPLICATION INFORMATION** (continued)

The function is quoted against the corresponding pin number

1. Oscillator feedback output
   The crystal receives its energy from this pin. The input impedance is approximately 2 kΩ in parallel with 5 pF.

2. Reactance control stage feedback
   This pin is fed internally with a sinewave derived from the reference input (pin 6) and controlled in amplitude by the internal reactance control circuit. The phase of the feedback from pin 2 to the crystal via C1 is such that the value of C1 is effectively increased. Pin 2 is held internally at a very low impedance therefore the tuning of the crystal is controlled automatically by the amplitude of the feedback waveform and its influence on the effective value of C1.

3. Positive 12 V supply
   The maximum voltage must not exceed 13.2 V.

4. Reference waveform output
   This pin is driven internally by the regenerated subcarrier waveform in R-Y phase. An output amplitude of nominally 1.5 V peak-to-peak is produced at low impedance. No d.c. load to earth is required. A d.c. connection between pins 4 and 6 is, however, necessary via the bifilar coupling inductor. The function of this inductor is to produce, on pin 6, a signal of equal amplitude and opposite phase (-(R-Y)) to that on pin 4. A centre tap on the inductor, connected to earth via a d.c. blocking capacitor, is therefore necessary.

5. Burst waveform input
   A burst waveform amplitude of 1 V peak-to-peak is required to be a.c.-coupled to this pin. The amplitude of the burst will normally be controlled by the adjustment and operation of the a.c.c. circuit. The input impedance at this pin is approximately 1 kΩ and a threshold level of 0.7 V must be exceeded before the burst signal becomes effective. A d.c. bias of 400 mV is internally derived for pin 5 The absolute level of the tip of the burst at pin 5 will normally reach 1.25 V (1.5 V peak-to-peak burst amplitude). Under abnormal conditions the burst amplitude should not be allowed to exceed 3 V peak-to-peak and a limiting condition will be reached in the i.c. which inhibits the performance of the phase lock loop.

**APPLICATION INFORMATION** (continued)

6. Reference waveform input
   This pin requires a reference waveform in the -(R-Y) phase, derived from pin 4 via a bifilar transformer (see pin 4), to drive the internal balanced reactance control stage. A d.c. connection between pins 4 and 6 must be made via the transformer.

7. Colour killer output
   This pin is driven from the collector of an internal switching transistor and requires an external load resistor (typical 10 kΩ) connected to +12 V. The unkilled and killed voltages on this pin are then +12 V and < 250 mV respectively. (The voltage on pin 9 at which switching of the colour killer output on pin 7 occurs is nominally +2.5 V

8. P.A.L. flip-flop square wave input
   A 2.5 V peak-to-peak square wave derived from the P.A.L. flip-flop (in the TBA520 demodulator i.c.) is required at this pin, a.c.-coupled via a capacitor. The input impedance is about 3.3 kΩ.

9. A.C.C. output
   An emitter follower provides a low impedance output potential which is negative-going with a rising burst input amplitude. With zero input signal the d.c. potential produced at pin 9 is set to be +4 V (RV1) The appearance of a burst signal on pin 5 will cause the potential on pin 9 to go in a negative direction in the event that the P.A.L. flip-flop is identified to be in the correct phase. The range of potential over which full a.c.c. control is excercised at pin 9 is determined by the control characteristics of the a.c.c. amplifier i.e. for the TBA560 from 1 V to 0.2 V. The potential at pin 9 will fall to a value within this range as the burst input signal is stabilised at 1.5 V peak-to-peak. The latter condition is achieved by correct adjustment of RV2. If, however, the P.A.L. flip-flop phase is wrong the potential on pin 9 will move positively. The potential divider R5, R6 will then operate a P.A.L. switch cut-off function in the TBA520 demodulator i.c. The switching of the colour killer output at pin 7 is designed to occur as the potential on pin 9 moves past +2.5 V.

10. A.C.C. level setting
    The network connected between pins 10 and 12 balances the a.c.c. circuit and RV1 is adjusted to give +4 V on pin 9 with no burst input signal to pin 5. C5 provides filtering.

11. A.C.C. gain control
    RV2 is adjusted to give the correct amplitude of burst signal on pin 5 (1.5 V peak-to-peak) under a.c.c. control;

12. See pin 10.

13. See pin 14.

## APPLICATION INFORMATION (continued)

14. D.C. control points in reference control loop
Pins 13 and 14 are connected to opposite sides of a differential amplifier circuit and are brought out for the purposes d. c. balancing of the reactance stage and the connection of the bandwidth-determining filter network. The conventional double time constant filter networks are R2, C2, R3, C3 and $R_4$, $C_4$. The d. c. potentials on these pins are nominally +7, 2 V.

15. Oscillator feedback input
The input impedance at this pin is nominally 3. 5 kΩ in parallel with 5 pF. No d. c. connection is required on this pin. The voltage in the i. c. between pin 15 and pin 1 is nominally 4. 7 times.

16. Negative supply (earth)

### PERFORMANCE AND COMMENTS

### Initial adjustment

(a) Remove burst signal.

(b) Short-circuit pins 13- 14. Adjust oscillator to correct frequency by C1. Remove short circuit.

(c) Set the a. c. c. level adjustment RV1, to give +4 V on pin 9.

(d) Apply burst signal.

(e) Adjust a. c. c. gain, RV 2, to give a burst amplitude of 1. 5 V peak-to-peak on pin 5.

### Phase lock loop performance (with crystal type 4322 152 0110)

(a) Phase difference between reference and burst signals for ±400 Hz deviation of crystal frequency, $\pm 10^{0}$.

(b) Typical holding range, ± 600 Hz.

(c) Typical pull-in range, ± 300 Hz.

(d) Temperature coefficient of oscillator frequency, i. c. only, 2 $Hz/^{0}C$.

# LINE OSCILLATOR CIRCUIT

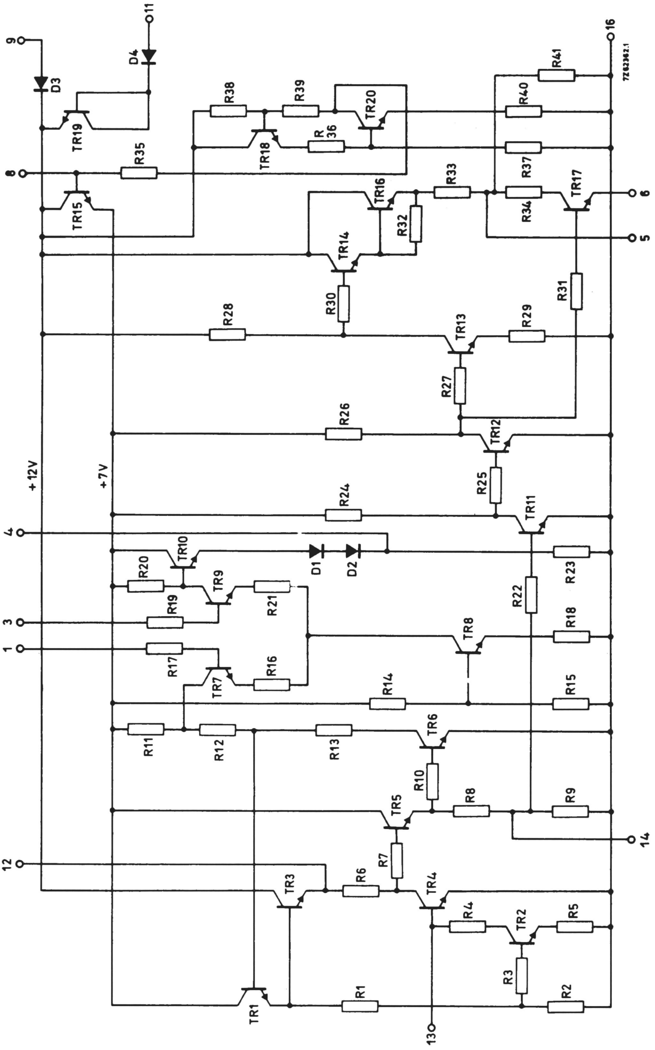
This circuit has been designed for use as line-oscillator and reactance stage in colour and monochrome t.v. receivers.
The circuit consists of a Miller-integrator-oscillator followed by a pulse shaping circuit, which delivers a positive pulse of 8 V and adjustable width. The available output current is in excess of 60 mA. Finally a supply voltage take-over switch for starting purposes is built in. The TBA720A can co-operate with the TBA890.

| QUICK REFERENCE DATA | | | | |
|---|---|---|---|---|
| Supply voltage | $V_{11-16}$ | typ. | 12 | V |
| Starting voltage | $V_{9-16}$ | | 8 to 12 | V |
| Required input signals | | | | |
| D.C. control voltage at pin 1 | $V_{1-16}$ | | 2,4 to 5,3 | V |
| at pin 3 | $V_{3-16}$ | | 2,4 to 5,3 | V |
| Delivered output signals | | | | |
| Output voltage at pin 5<br>no load; peak-to-peak value | $V_{5-16(p-p)}$ | typ. | 8 | V |
| Output current at pin 5 | $I_5$ | < | 60 | mA |

**PACKAGE OUTLINES**

TBA720A : 16-lead DIL; plastic (SOT-38).
TBA720AQ: 16-lead QIL; plastic (SOT-58).

## CIRCUIT DIAGRAM


9
11
16
8
4
3
1
12
13
14
5
6
+12V
+7V
D1
D2
D3
D4
TR1
TR2
TR3
TR4
TR5
TR6
TR7
TR8
TR9
TR10
TR11
TR12
TR13
TR14
TR15
TR16
TR17
TR18
TR19
TR20
R1
R2
R3
R4
R5
R6
R7
R8
R9
R10
R11
R12
R13
R14
R15
R16
R17
R18
R19
R20
R21
R22
R23
R24
R25
R26
R27
R28
R29
R30
R31
R32
R33
R34
R35
R 36
R37
R38
R39
R40
R41
7Z62382.1

**RATINGS** Limiting values in accordance with the Absolute Maximum System (IEC134).

| | | | |
|---|---|---|---|
| Voltages | | | |
| Supply voltage | $V_{11-16}$ | max. | 16 V |
| Starting voltage | $V_{9-16}$ | max. | 15 V |
| Currents | | | |
| Output current | $I_5$ | max. | 60 mA |
| Power dissipation | | | |
| Total power dissipation when mounted on a printed-wiring board | $P_{tot}$ | max. | 280 mW |
| Temperatures | | | |
| Storage temperature | $T_{stg}$ | | −55 to +125 °C |
| Operating ambient temperature | $T_{amb}$ | | 0 to +60 °C |

**CHARACTERISTICS** Measured in the test set-up on page 4

| | | | |
|---|---|---|---|
| Supply voltage | $V_{11-16}$ | typ. | 12 V<br>10 to 13 V |
| Starting voltage | $V_{9-16}$ | > | 8 V [1] |

**CHARACTERISTICS** at $T_{amb} = 25\ ^{o}C$; $V_{11-16} = 12$ V

| | | | |
|---|---|---|---|
| Supply current [2] | $I_{11}$ | typ. | 10,5 mA<br>7,5 to 13,5 mA |
| Required input signals | | | |
| D.C. control voltage for nominal frequency at pin No. 1 and pin No. 3 | $V_{1-16} = V_{3-16}$ | | 2,4 to 5,3 V |
| Sensitivity of reactance stage | $V_{1-3}$ | typ. | 2 kHz/V |
| Duty cycle regulation at pin No. 14 | $I_{14}$ | typ. | 0 μA<br>+400 to −400 μA |
| Delivered output signals | | | |
| Output voltage at pin No. 5 no load; peak-to-peak value | $V_{5-16(p-p)}$ | typ. | 8 V |
| Output current | $I_5$ | < | 60 mA |
| Duty cycle; without regulation | $\delta$ | typ. | 40 %<br>35 to 45 % |
| with regulation | $\delta$ | | 20 to 60 % |
| Rise time at pin No. 5 leading edge of output pulse | $t_r$ | typ. | 200 ns |

---

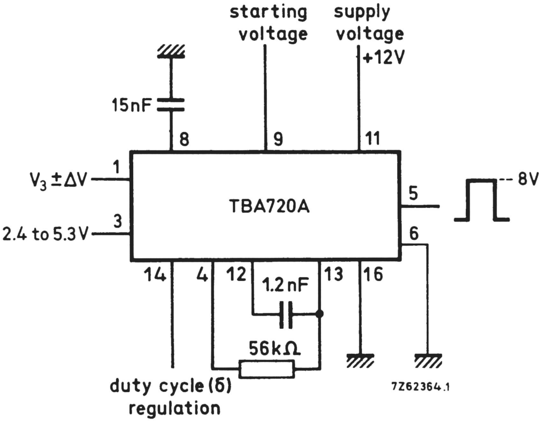
[1] Maximum starting voltage should not exceed the value of the supply voltage minus 1 volt.

[2] No load connected to the output. When the output is loaded, the extra current is: $\delta \times I$, in which $\delta$ = duty cycle of output pulse and I = current flowing during output pulse.

## CHARACTERISTICS (continued)

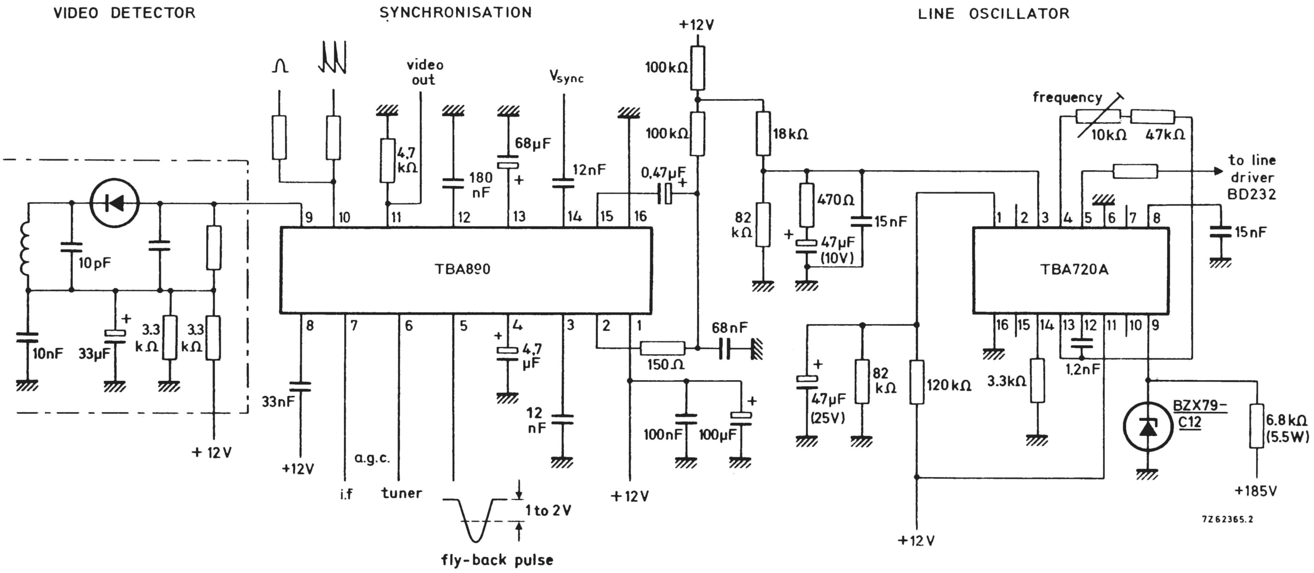
| | | | |
|---|---|---|---|
| Relative frequency deviation for $\Delta V_{11}$ = 1 V | | | 2 ‰ |
| Relative frequency deviation for change of ambient temperature 25 to 55 °C | | | 3 ‰ |
| Allowable hum-ripple on supply line (peak-to-peak value) | $\Delta V_{11-16(p-p)}$ | typ. | 100 mV |

### Test set-up


starting voltage
supply voltage
+12V
15nF
8
9
11
1
$V_3 \pm \Delta V$
3
2.4 to 5.3V
TBA720A
5
8V
6
14
4
12
1.2nF
13
16
56kΩ
duty cycle (δ) regulation
7Z62364.1

## APPLICATION INFORMATION

The TBA720A with the TBA890 or TBA900 in a receiver with transistorized line deflection.


VIDEO DETECTOR
SYNCHRONISATION
LINE OSCILLATOR
10pF
10nF
33μF
3.3 kΩ
3.3 kΩ
+ 12V
33nF
+12V
video out
4.7 kΩ
180 nF
68μF
Vsync
12nF
TBA890
i.f
a.g.c.
tuner
4.7 μF
12 nF
1 to 2V
fly-back pulse
+12V
100kΩ
100kΩ
0,47μF
68nF
150Ω
100nF
100μF
+12V
18kΩ
82 kΩ
470Ω
47μF (10V)
15nF
47μF (25V)
82 kΩ
120kΩ
3.3kΩ
+12V
frequency
10kΩ
47kΩ
to line driver BD232
TBA720A
15nF
1.2nF
BZX79-C12
6.8kΩ (5.5W)
+185V
7Z62365.2

## APPLICATION INFORMATION (continued)

Notes

1. The TBA720A is intended to drive a line deflection circuit equipped with transistors.
2. The duty cycle δ can be adjusted by connecting a resistor between pin 14 and ground or the supply.
3. The oscillation frequency can be set between 10 kHz and 25 kHz by connecting a resistor between pins 4 and 13, and a capacitor between pins 12 and 13.
4. At a nominal oscillation frequency of 15,625 kHz, the frequency deviation is limited to ±1,3 kHz to safeguard the line timebase output circuits.
5. Besides the oscillator, the TBA720A incorporates a reactance stage and a supply voltage take-over switch for starting purposes (pin 9). The latter can be used to advantage if the 12 V supply is derived from the line flyback pulse.
6. Pins 2, 7, 10 and 15 should not be connected.

# LIMITER/AMPLIFIER

The TBA750C is a limiter/amplifier with f.m. detector, d.c. volume control and a.f. preamplifier. It is intended for 4,5 MHz, 5,5 MHz or 10,7 MHz. The limiter/amplifier is a four-stage differential amplifier that gives very good noise and interference suppression. The detector is of the balanced type. The d.c. volume control stage has excellent control characteristics with a control range of more than 80 dB. The a.f. preamplifier can drive a triode-pentode output stage or a class-A push-pull transistor output stage.

## QUICK REFERENCE DATA

| | | | | |
|---|---|---|---|---|
| Supply voltage | $V_{2-5}$ | typ | 12 | V |
| Total current drain | $I_{tot}$ | typ | 34 | mA |
| Frequency | $f_o$ | | 5,5 | MHz |
| Input voltage at start of limiting | $V_{i\,lim}$ | typ | 130 | $\mu$V |
| A.M. rejection at $V_i$ = 1 mV | $\alpha$ | typ | 45 | dB |
| A.F. output voltage at $\Delta f = \pm$ 15 kHz at pin 16 | $V_{o(rms)}$ | typ | 2,7 | V |
| D.C. volume control range | | > | 80 | dB |

**PACKAGES OUTLINES**

TBA750C: 16-lead DIL; plastic (SOT-38).
TBA750CQ: 16-lead QIL; plastic (SOT-58).

## CIRCUIT DIAGRAM

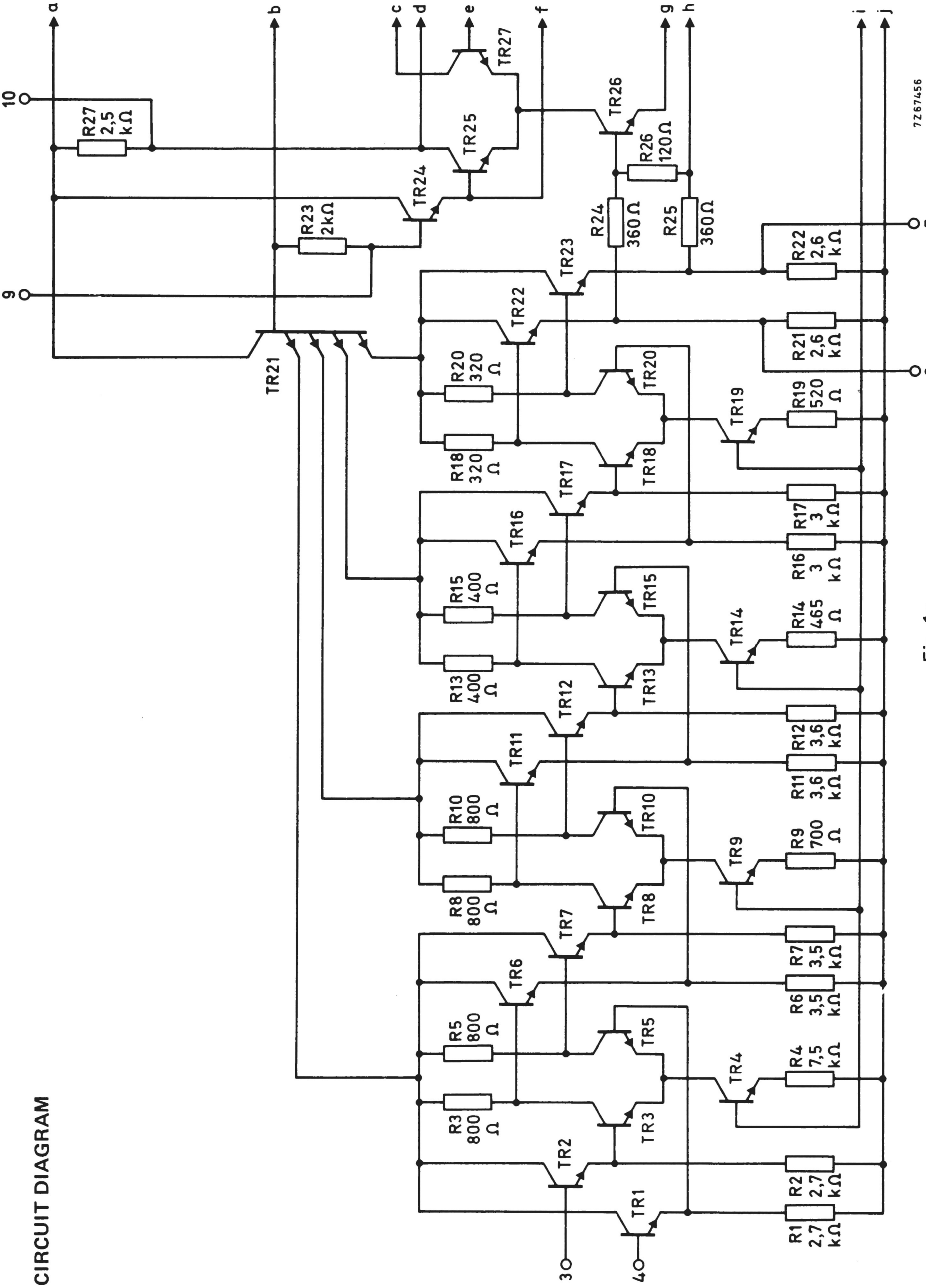

a
b
c
d
e
f
g
h
i
j
10
9
3
4
7
6
R27 2,5 kΩ
R23 2kΩ
R26 120Ω
R24 360Ω
R25 360Ω
R22 2,6 kΩ
R21 2,6 kΩ
R20 320 Ω
R18 320 Ω
R19 520 Ω
R17 3 kΩ
R16 3 kΩ
R15 400 Ω
R13 400 Ω
R14 465 Ω
R12 3,6 kΩ
R11 3,6 kΩ
R10 800 Ω
R8 800 Ω
R9 700 Ω
R7 3,5 kΩ
R6 3,5 kΩ
R5 800 Ω
R3 800 Ω
R4 7,5 kΩ
R2 2,7 kΩ
R1 2,7 kΩ
TR1
TR2
TR3
TR4
TR5
TR6
TR7
TR8
TR9
TR10
TR11
TR12
TR13
TR14
TR15
TR16
TR17
TR18
TR19
TR20
TR21
TR22
TR23
TR24
TR25
TR26
TR27
7Z67456

Fig. 1a.

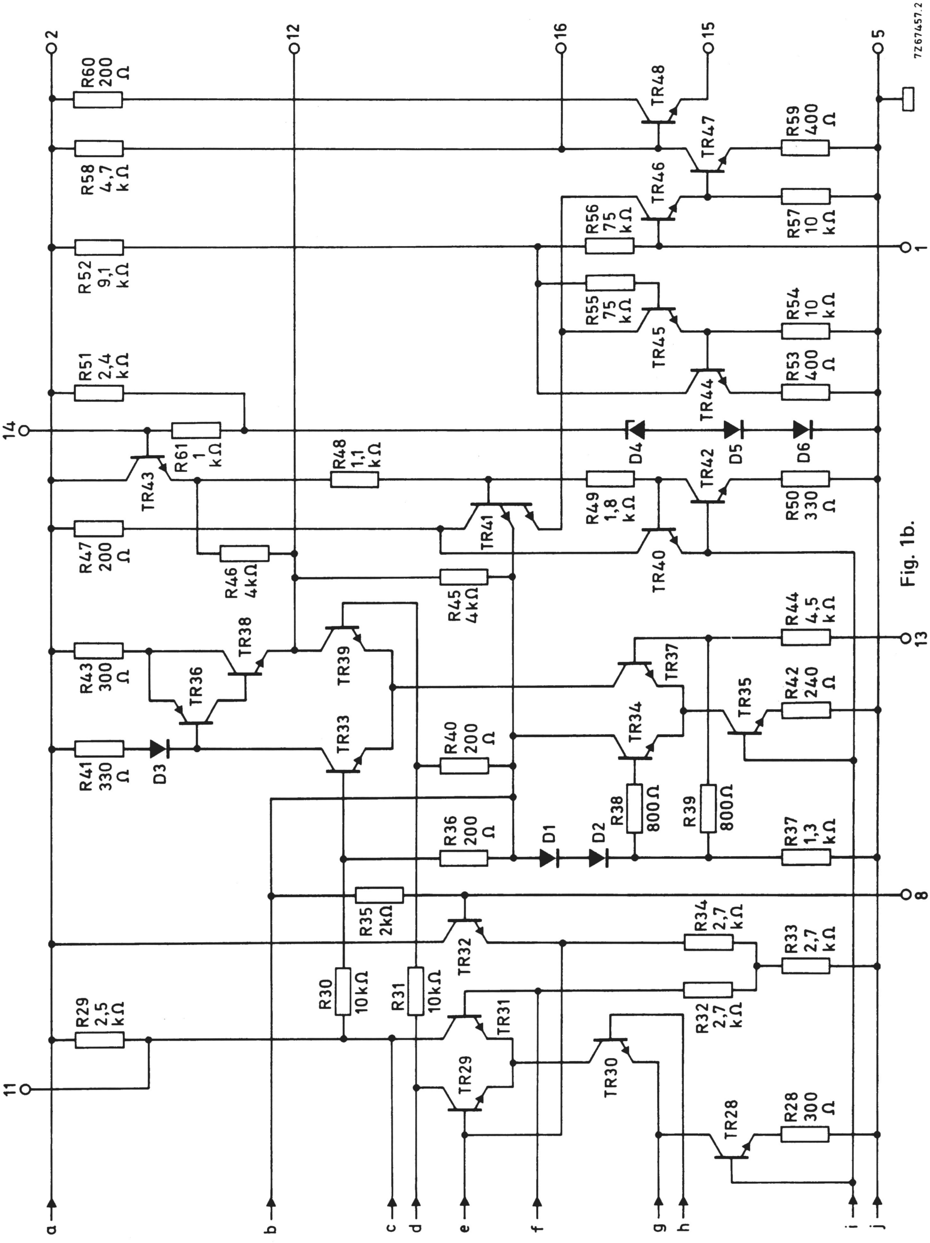

7Z67457.2
2
12
16
15
5
14
1
13
8
11
a
b
c
d
e
f
g
h
i
j
R60 200 Ω
R58 4,7 kΩ
R52 9,1 kΩ
R51 2,4 kΩ
R61 1 kΩ
R48 1,1 kΩ
R47 200 Ω
R46 4kΩ
R45 4kΩ
R43 300 Ω
R41 330 Ω
R40 200 Ω
R36 200 Ω
R35 2kΩ
R30 10kΩ
R31 10kΩ
R29 2,5 kΩ
R59 400 Ω
R57 10 kΩ
R56 75 kΩ
R55 75 kΩ
R54 10 kΩ
R53 400 Ω
R49 1,8 kΩ
R50 330 Ω
R44 4,5 kΩ
R42 240 Ω
R38 800Ω
R39 800Ω
R37 1,3 kΩ
R34 2,7 kΩ
R33 2,7 kΩ
R32 2,7 kΩ
R28 300 Ω
TR28
TR29
TR30
TR31
TR32
TR33
TR34
TR35
TR36
TR37
TR38
TR39
TR40
TR41
TR42
TR43
TR44
TR45
TR46
TR47
TR48
D1
D2
D3
D4
D5
D6

Fig. 1b.

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | |
|---|---|---|---|
| Supply voltage | $V_{2-5}$ | max | 16 V * |
| Storage temperature | $T_{stg}$ | | −55 to + 125 °C |
| Operating ambient temperature | $T_{amb}$ | | −25 to + 55 °C |
| Power dissipation | | | |

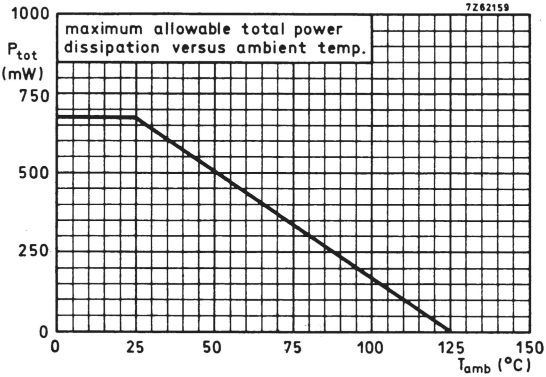


Fig. 2.

## CHARACTERISTICS

Measured in test circuit Fig. 3.

| | | | |
|---|---|---|---|
| Supply voltage range<br>see also Fig. 4 | $V_{2-5}$ | | 10 to 25 V |
| Total current drain; pin 15 not connected | $I_2$ | | 25 to 45 mA |
| Input limiting voltage at $V_o$ = −3 dB (r.m.s. value) | $V_{i\,lim(rms)}$ | typ | 130 μV |
| I.F. output voltage at pins 6 and 7<br>(peak-to-peak value) | $V_{6-5(p\text{-}p)}$<br>$V_{7-5(p\text{-}p)}$ | typ | 380 mV |
| A.M. rejection | | | |
| $V_i$ = 1 mV | $\alpha$ | typ | 45 dB |
| $V_i$ = 10 mV | $\alpha$ | typ | 50 dB |
| $V_i$ = 100 mV | $\alpha$ | typ | 55 dB |
| D.C. volume control range; see also Fig. 5 | | > | 80 dB |
| A.F. preamplifier voltage gain<br>pin 1 to pin 16 | $G_v$ | typ | 10 |
| Input resistance at pin 1 | $R_i$ | ≥ | 35 kΩ |

---

* Allowable only if the dissipation in the IC is limited by means of a series resistor in the supply (see also Fig. 4).

## CHARACTERISTICS (continued)

| | | | | |
|---|---|---|---|---|
| A.F. output voltages (r.m.s. values) | | | | |
| $\Delta f = \pm 15$ kHz; $f_m = 1$ kHz | $V_{10-5(rms)}$<br>$V_{11-5(rms)}$ | typ | 65 | mV |
| | $V_{12-5(rms)}$ | typ | 250 | mV |
| | $V_{16-5(rms)}$ | typ | 2,7 | V |
| Total harmonic distortion | | | | |
| at pin 12; $\Delta f = 15$ kHz | $d_{tot}$ | typ | 3 | % |
| at pin 1 with respect to pin 16; $V_{o(rms)} = 3$ V | $d_{tot}$ | typ | 2,6 | % |

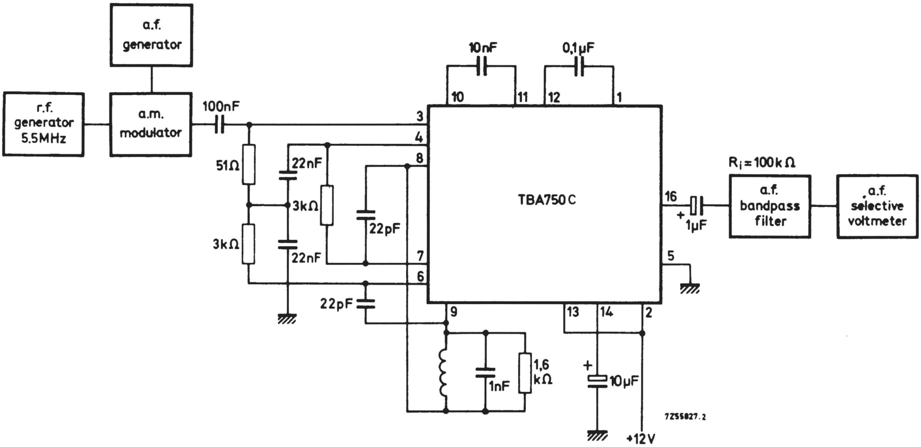

a.f. generator
r.f. generator 5.5MHz
a.m. modulator
100nF
51Ω
3kΩ
22nF
3kΩ
22nF
22pF
22pF
10nF
0,1μF
10
11
12
1
3
4
8
7
6
9
13
14
2
16
5
TBA750C
1nF
1,6 kΩ
10μF
+12V
1μF
$R_i = 100k\Omega$
a.f. bandpass filter
a.f. selective voltmeter
7Z55827.2

Fig.3 Test circuit; for f.m.: $f_o = 5{,}5$ MHz; $\Delta f = \pm 15$ kHz; $f_m = 70$ Hz.
For a.m.: $m = 0{,}3$; $f_m = 1$ kHz.

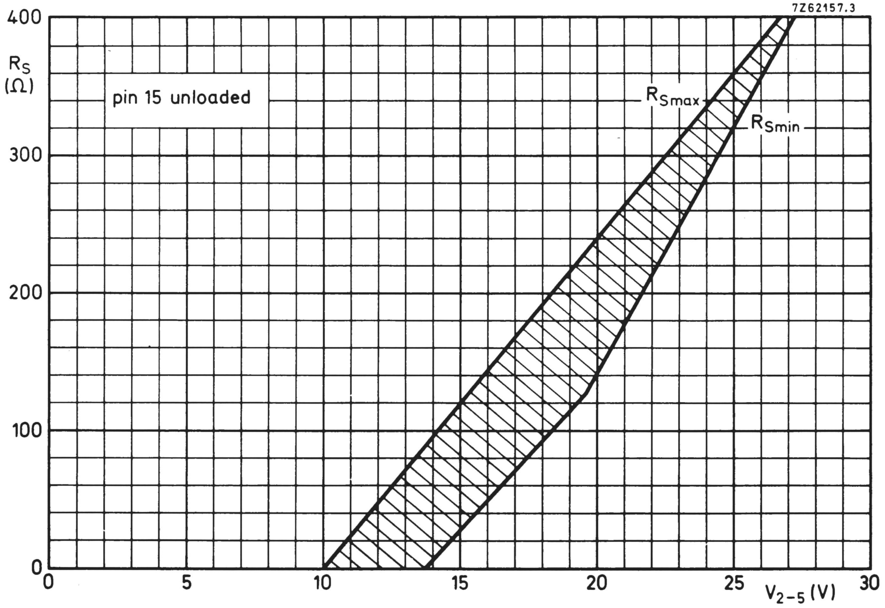


Fig. 4 Maximum and minimum values for the power supply series resistance ($R_S$).

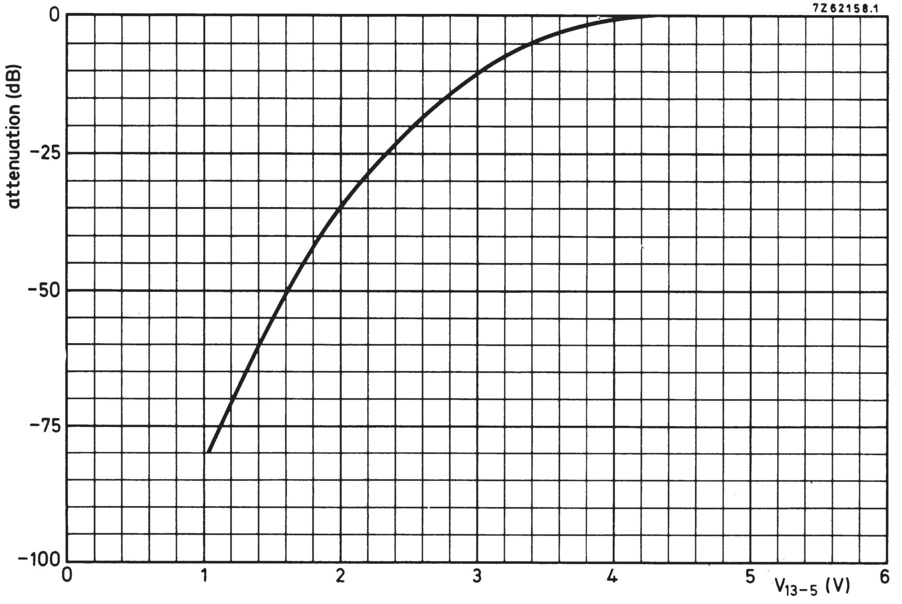


Fig. 5 Remote control characteristic.

**APPLICATION INFORMATION** at f = 5,5 MHz

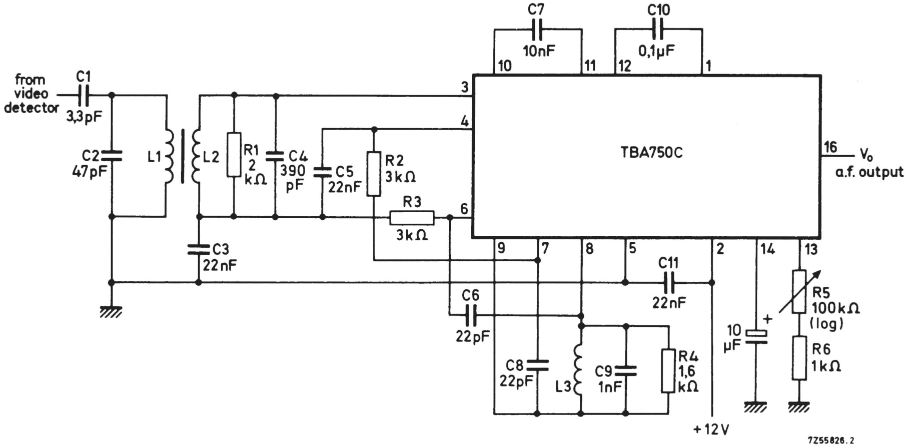

from video detector
C1
3,3pF
C2
47pF
L1
L2
R1
2 kΩ
C4
390 pF
C5
22nF
R2
3kΩ
R3
3kΩ
C3
22nF
C7
10nF
C10
0,1μF
10
11
12
1
3
4
6
TBA750C
16
$V_o$
a.f. output
9
7
8
5
2
14
13
C11
22nF
C6
22pF
C8
22pF
L3
C9
1nF
R4
1,6 kΩ
10 μF
+
R5
100kΩ
(log)
R6
1kΩ
+12V
7Z55826.2

Fig. 6.

L1 = 18 μH; $Q_{L1}$ = 36
L2 = 2,2 μH; $Q_{L2}$ = 21
L3 = 0,84 μH; $Q_{L3}$ = 22

**Note**

$Q_{L1}$, $Q_{L2}$ and $Q_{L3}$ are the loaded Q-factors.

The transfer ratio of the input bandpass filter: $\frac{V_2}{V_1}$ = 0,54.

The peak-to-peak bandwidth of the detector S-curve is 300 kHz.

# TELEVISION SIGNAL PROCESSING CIRCUIT

The TBA890 is a silicon monolithic integrated signal processing circuit for monochrome and colour television receivers.

It combines the following functions:

- video pre-amplifier with emitter-follower output and short circuit protection.
- blanking facility for the video amplifier.
- gated a.g.c. detector supplying the a.g.c. voltages for the vision i.f. amplifier and tuner.
- noise cancelling circuit in the a.g.c. and sync separator circuits.
- sync separator.
- automatic horizontal phase detector
- vertical sync pulse separator.

The circuit is designed for receivers equipped with tubes or transistors in the deflection and video output stages.

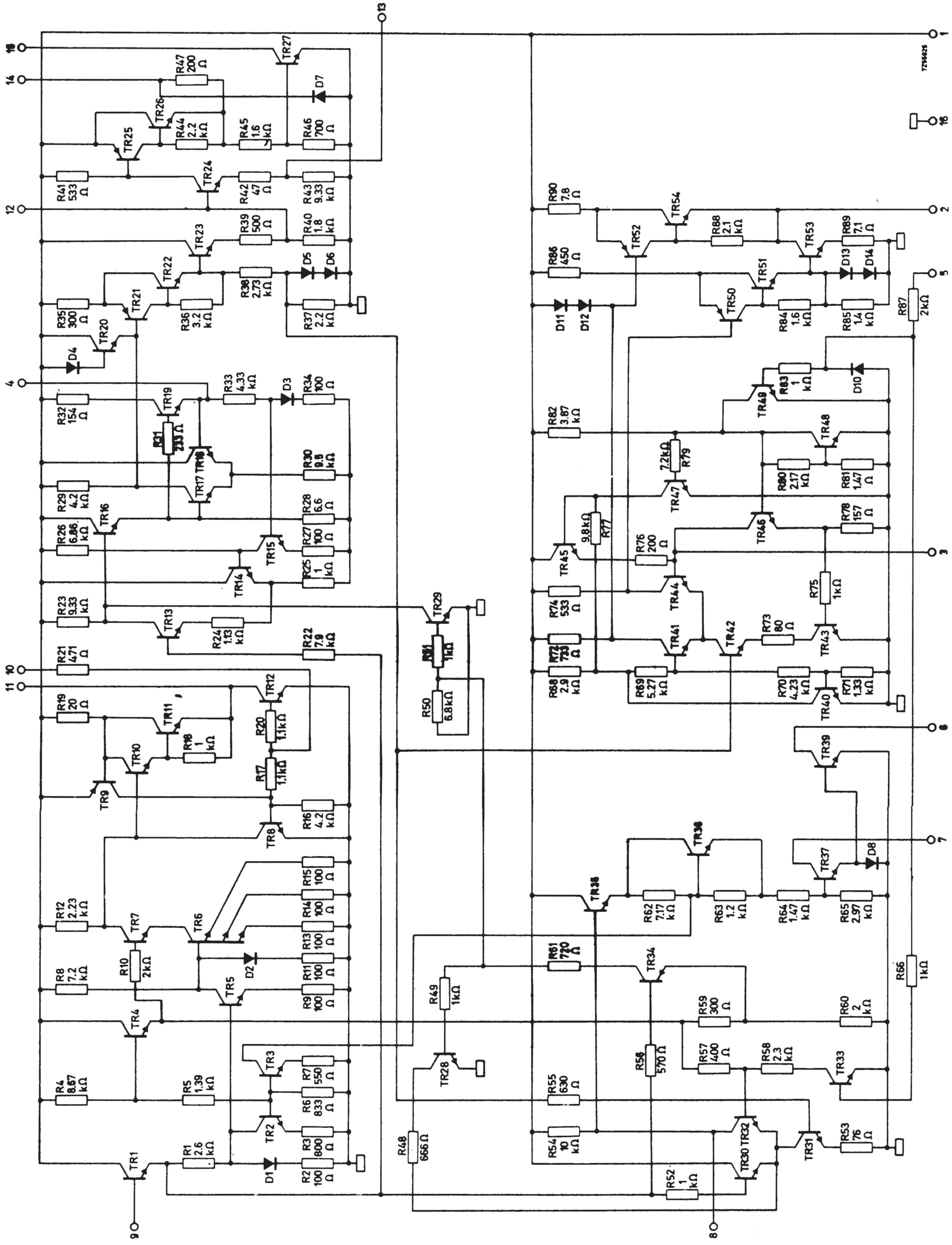
The control stages in the i.f. amplifier and the tuner have to be equipped with n-p-n transistors. The circuit is developed for signals with negative modulation.

## QUICK REFERENCE DATA

| | | | | |
|---|---|---|---|---|
| Supply voltage | $V_P$ | typ. | 12 | V |
| Ambient temperature | $T_{amb}$ | typ. | 25 | $^oC$ |
| Video input voltage (peak-to-peak value) | $V_{9-16(p-p)}$ | typ. | 2,7 | V |
| Voltage gain of the video amplifier | $G_V$ | typ. | 7 | dB |
| A.G.C. voltage for i.f. part | $V_{7-16}$ | 1,0 to | 12 | V |
| A.G.C. voltage for tuner | $V_{6-16}$ | 0,3 to | 12 | V |
| Output voltage range horizontal phase detector | $V_{2-16}$ | 2 to | 10 | V |
| Vertical sync output voltage (positive going pulse; peak-to-peak value) | $V_{14-16(p-p)}$ | typ. | 11 | V |

**PACKAGE OUTLINES**

TBA890 : 16-lead DIL; plastic (SOT-38).
TBA890Q: 16-lead QIL; plastic (SOT-58).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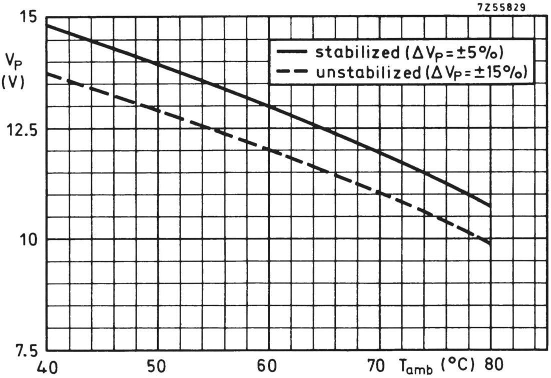
D8
D10
D11
D12
D13
D14
R1 2.6 kΩ
R2 100 Ω
R3 800 Ω
R4 8.67 kΩ
R5 1.39 kΩ
R6 833 Ω
R7 550 Ω
R8 7.2 kΩ
R9 100 Ω
R10 2kΩ
R11 100 Ω
R12 2.23 kΩ
R13 100 Ω
R14 100 Ω
R15 100 Ω
R16 4.2 kΩ
R17 1.1kΩ
R18 1 kΩ
R19 20 Ω
R20 1.1kΩ
R21 471 Ω
R22 7.9 kΩ
R23 9.33 kΩ
R24 1.13 kΩ
R25 1 kΩ
R26 6.86 kΩ
R27 100 Ω
R28 6.6 Ω
R29 4.2 kΩ
R30 9.8 kΩ
R31 233 Ω
R32 154 Ω
R33 4.33 kΩ
R34 100 Ω
R35 300 Ω
R36 3.2 kΩ
R37 2.2 kΩ
R38 2.73 kΩ
R39 500 Ω
R40 1.8 kΩ
R41 533 Ω
R42 47 Ω
R43 9.33 kΩ
R44 2.2 kΩ
R45 1.6 kΩ
R46 700 Ω
R47 200 Ω
R48 666 Ω
R49 1kΩ
R50 6.8kΩ
R51 1kΩ
R52 1 kΩ
R53 76 Ω
R54 10 kΩ
R55 630 Ω
R56 570 Ω
R57 400 Ω
R58 2.3 kΩ
R59 300 Ω
R60 2 kΩ
R61 720 Ω
R62 7.17 kΩ
R63 1.2 kΩ
R64 1.47 kΩ
R65 2.97 kΩ
R66 1kΩ
R68 2.9 kΩ
R69 5.27 kΩ
R70 4.23 kΩ
R71 1.33 kΩ
R72 733 Ω
R73 80 Ω
R74 533 Ω
R75 1kΩ
R76 200 Ω
R77 9.8 kΩ
R78 157 Ω
R79 7.2kΩ
R80 2.17 kΩ
R81 1.47 Ω
R82 3.87 kΩ
R83 1 kΩ
R84 1.6 kΩ
R85 1.4 kΩ
R86 450 Ω
R87 2kΩ
R88 2.1 kΩ
R89 7.1 Ω
R90 7.8 Ω

**RATINGS** Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | | | |
|---|---|---|---|---|---|
| Supply voltage | $V_P$ | max. | | 20 | V[1] |
| Power dissipation | $P_{tot}$ | max. | | 700 | mW |
| Temperatures | | | | | |
| Storage temperature | $T_{stg}$ | -55 | to | +125 | °C |
| Operating ambient temperature | $T_{amb}$ | -25 | to | +80 | °C |



Maximum allowable nominal supply voltage as a function of the maximum ambient temperature.

---

[1] Allowed only while receiver is warming up.

## CHARACTERISTICS

| | | |
|---|---|---|
| Supply voltage range | $V_P$ | See curves on page 3 |

The following characteristics are measured in the circuit on p. 7 at $T_{amb}$ = 25 °C; $V_P$ = 12 V.

### Video amplifier

| | | | | |
|---|---|---|---|---|
| Input resistance | $R_{9-16}$ | > | 30 | kΩ |
| Input capacitance | $C_{9-16}$ | < | 3 | pF |
| Bandwidth (3 dB) | B | > | 5 | MHz |
| Linearity (m) | | > | 0.9 | |
| Rise time and fall time at the output | $t_r$; $t_f$ | < | 50 | ns |
| Voltage gain | $G_v$ | typ. | 7 | dB |
| Video input voltage (peak-to-peak value) | $V_{9-16(p-p)}$ | typ. | 2.7 | V 1) |
| D.C. bias video detector voltage | $V_{bias}$ | typ. | 6 | V 2) |
| Video output voltage (peak-to-peak value) | $V_{11-16(p-p)}$ | typ. | 6 | V 1) |
| Black level at the output | $V_{11-16}$ | typ. | 5 | V 3) |
| Available video output current (peak value) | $I_{11M}$ | ≤ | 30 | mA 4) |

### Tolerances on the video output voltages

| | | | | |
|---|---|---|---|---|
| I.C. processing spreads | $\pm\Delta V_{11-16}$ | < | 420 | mV 5) |
| Temperature drift | $-\Delta V_{11-16}$ | typ. | 1.8 | mV/°C |
| Spreads over a.g.c. expansion (entire range) | $\pm\Delta V_{11-16}$ | < | 100 | mV 6) |
| Supply voltage | $\frac{\Delta V_{11-16}}{\Delta V_P}$ | typ. | 0.5 | |

---

1) Signal with negative going sync.; this value is obtained only when the input signal meets the C.C.I.R. standard.

2) A voltage divider with 5% tolerance resistors is required between pin 9 and supply terminal.

3) Only valid if the video signal is in accordance with the C.C.I.R. standard.

4) The total load on pin 11 must be such that the d.c. output current $I_{11} \leq 15$ mA.

5) The spreads of the voltage divider for the bias of the video detector of ± 5% is included in this figure.

6) Variation about a nominal condition, the i.f. being fully controlled and the tuner uncontrolled.

## CHARACTERISTICS (continued)

### Tolerances on the black level at the output

| | | | | |
|---|---|---|---|---|
| I.C. processing spreads | $\pm\Delta V_{11-16}$ | < | 420 | mV 1) |
| Temperature drift | $-\Delta V_{11-16}$ | typ. | 1.7 | mV/°C |
| Spreads over a.g.c. expansion (entire range) | $\pm\Delta V_{11-16}$ | < | 130 | mV 2) |
| Supply voltage | $\frac{\Delta V_{11-16}}{\Delta V_P}$ | typ. | 0.4 | |

### Video blanking

| | | | | |
|---|---|---|---|---|
| Input voltage (peak-to-peak value) | $V_{10-16(p-p)}$ | | 1 to 5 | V |
| Input resistance | $R_{10-16}$ | typ. | 1 | kΩ |
| Output voltage during blanking | $V_{11-16}$ | < | 500 | mV |

### A.G.C. circuit

| | | | | |
|---|---|---|---|---|
| Range of control voltage i.f. amplifier | $V_{7-16}$ | | 1 to 12 | V 3) |
| Range of control voltage tuner | $V_{6-16}$ | | 0.3 to 12 | V 3) |
| Signal expansion for full control of i.f. amplifier and tuner | | typ. | 0.5 | dB |
| Current i.f. control point | $I_7$ | < | 20 | mA |
| Current tuner control point | $I_6$ | < | 20 | mA |
| Current i.f. control point for tuner take-over | $I_7$ | see note 4 | | |
| Keying input pulse (peak-to-peak value) | $V_{5-16(p-p)}$ | see note 5 | | |
| Input resistance | $R_{5-16}$ | typ. | 2 | kΩ |

---

1) The spreads of the voltage divider for the bias of the video detector of ± 5% is included in this figure (pin 9).

2) Variation about a nominal condition, the i.f. being fully controlled and the tuner uncontrolled.

3) Positive going at increasing input signal.

4) This value depends on the ratio between the external impedances on pins 6 and 7. With equal impedances the current of the i.f. control point at tuner take-over will be about 16% from its maximum value (minimum control voltage).

5) Negative going pulse is required. The voltage during scan should be between 1 V and 2 V.

**CHARACTERISTICS** (continued)

Horizontal synchronization circuit

| | | | | |
|---|---|---|---|---|
| Sync. separator | | see note 1 | | |
| Output voltage range of phase detector | $V_{2-16}$ | | 2 to 10 | V 2) |
| Control steepness | $S_\varphi$ | typ. | 2.5 | V/μs 3) |
| Phase deviation between front edge sync. pulse and front edge flyback pulse | $\varphi_0$ | typ. | 1.5 | μs |
| Variation $\varphi_0$ caused by internal spreads | $\pm\Delta\varphi_0$ | typ. | 0.3 | μs 4) |
| Output voltage range as a frequency detector | $V_{2-16}$ | | 4 to 8 | V 5) |

Vertical synchronization circuit

| | | | | |
|---|---|---|---|---|
| Output voltage vertical sync. pulse generator | $V_{14-16}$ | typ. | 11 | V |
| Output impedance | $R_{14-16}$ | typ. | 2 | kΩ |

---

1) The sync. pulse is sliced about 25% below top sync. level. A sliding bias circuit makes the slicing level independent of the signal strength.

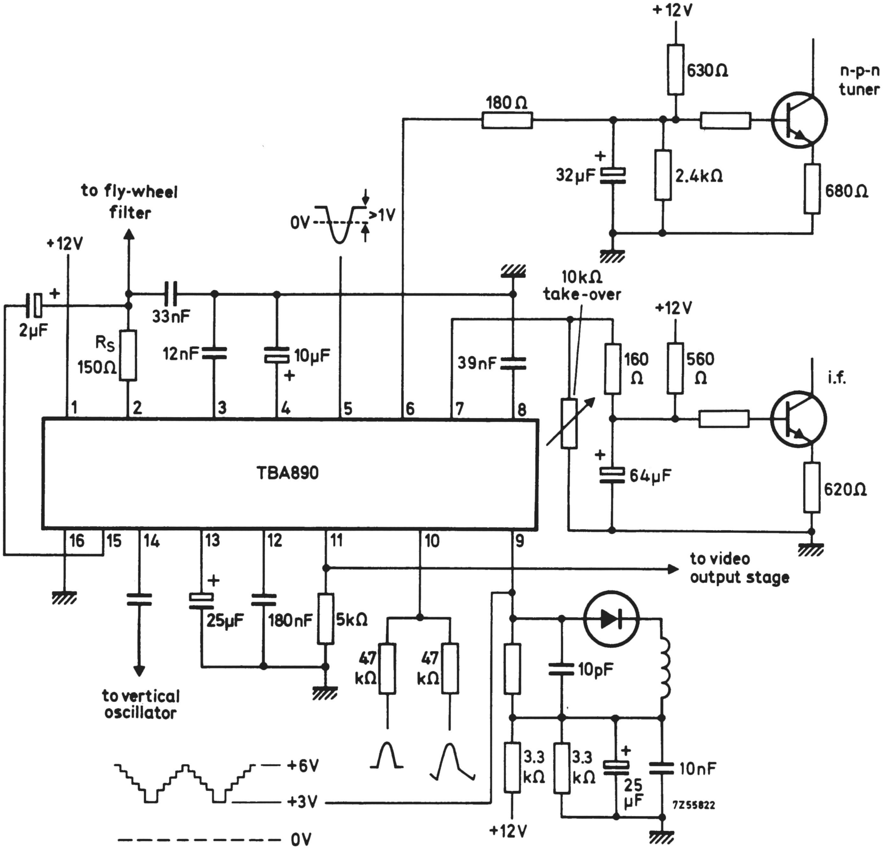
2) Nominal voltage 6 V.

3) Higher values of this control steepness can be obtained by changing $R_S$ (see circuit on page 7). For example $R_S$ = 56 Ω, $S_\varphi$ = 5 V/μs and $R_S$ = 0, $S_\varphi$ = ≥25 V/μs.

4) In addition to this figure ± 7% of the retrace time of the sawtooth generated on pin 3 has to be added to find the total spreads of $\varphi_0$.
This value of ± 7% is obtained only when the tolerance of the capacitor connected to pin 3 does not exceed ± 10%.

5) Nominal voltage 6 V.
The load impedance on pin 2 of the circuit on page 7 is about 50 kΩ.
When a higher impedance is used (tube equipped reactance stage) values from 2 V to 10 V can be reached.

## APPLICATION INFORMATION


+12V
630Ω
n-p-n
tuner
180 Ω
+
32μF
2.4kΩ
680Ω
to fly-wheel
filter
0V
>1V
+12V
+
2μF
33nF
Rs
150Ω
12nF
10μF
+
39nF
10kΩ
take-over
+12V
160
Ω
560
Ω
i.f.
+
64μF
620Ω
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2
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4
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6
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8
TBA890
16
15
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13
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to video
output stage
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25μF
180nF
5kΩ
47
kΩ
47
kΩ
10pF
to vertical
oscillator
+6V
+3V
0V
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kΩ
3.3
kΩ
+
25
μF
10nF
+12V
7Z55822

# HORIZONTAL COMBINATION

The TBA920 is a monolithic integrated circuit intended for television receivers with transistor-thyristor-or tube equipped output stages.
It combines the following functions:
- noise gated sync separator
- line oscillator
- phase comparison between sync pulse and oscillator
- loopgain and time constant switching (also for video recorder applications)
- phase comparison between line-flyback pulse and oscillator
- output stage for drive a variety of line output stages

## QUICK REFERENCE DATA

| | | | | |
|---|---|---|---|---|
| Supply voltage | $V_{1-16}$ | nom. | 12 | V |
| Ambient temperature | $T_{amb}$ | | 25 | °C |
| Input signals | | | | |
| Video input voltage (positive-going sync) top sync to white value | $V_{8-16(p-p)}$ | typ. | 3<br>1 to 7 | V<br>V |
| Noise gate input current (peak value) | $I_{9M}$ | > | 30 | μA |
| Input resistance of noise gate | $R_{9-16}$ | typ. | 200 | Ω |
| Flyback signal input voltage (peak value) | $V_{5-16M}$ | typ. | ±1 | V |
| Flyback signal input current (peak value) | $I_{5M}$ | typ. | 1 | mA |
| Output signals | | | | |
| Line driver output voltage (peak-to-peak value) | $V_{2-16(p-p)}$ | typ. | 10 | V |
| Line driver output current (average value) | $I_{2(AV)}$ | max. | 20 | mA |
| Line driver output current (peak value) | $I_{2M}$ | max. | 200 | mA |
| Composite sync output voltage (peak value) | $V_{7-16M}$ | typ. | 10 | V |

## PACKAGE OUTLINES

TBA920 : 16-lead DIL; plastic (SOT-38).
TBA920Q: 16-lead QIL; plastic (SOT-58).

**RATINGS** Limiting values in accordance with the Absolute Maximum System (IEC134)

Voltages

| | | | | |
|---|---|---|---|---|
| Supply voltage | $V_{1-16}$ | max. | 13,2 | V |
| Pin No. 3 voltage | $V_{3-16}$ | | 0 to 13,2 | V |
| Pin No. 8 voltage | $-V_{8-16}$ | max. | 12 | V |
| Pin No. 10 voltage | $V_{10-16}$ | | −0,5 to +5 | V |

Currents

| | | | | |
|---|---|---|---|---|
| Pin No. 2 current (average value) | $I_{2(AV)}$ | max. | 20 | mA |
| (peak value) | $I_{2M}$ | max. | 200 | mA |
| Pin.No. 5 current (peak value) | $I_{5M}$ | max. | 10 | mA |
| Pin.No. 7 current (peak value) | $I_{7M}$ | max. | 10 | mA |
| Pin No. 8 current (peak value) | $I_{8M}$ | max. | 10 | mA |
| Pin No. 9 current (peak value) | $I_{9M}$ | max. | 10 | mA |

Power dissipation

| | | | | |
|---|---|---|---|---|
| Total power dissipation | $P_{tot}$ | max. | 600 | mW 1) |

Temperatures

| | | | | |
|---|---|---|---|---|
| Storage temperature | $T_{stg}$ | | −55 to +125 | °C |
| Operating ambient temperature | $T_{amb}$ | | −20 to +60 | °C |

**CHARACTERISTICS** at $V_{1-16} = 12$ V; $T_{amb} = 25$ °C

Measured in circuit on page 6 (CCIR standard).

| | | | | |
|---|---|---|---|---|
| Current consumption at $I_2 = 0$ | $I_1$ | typ. | 36 | mA |

**Required input signals**

Video signal

| | | | | |
|---|---|---|---|---|
| Input voltage (positive going sync) peak-to-peak value | $V_{i(p-p)}$ | typ. | 3 | V |
| | | | 1 to 7 | V |
| Input current during sync pulse (peak value) | $I_{8M}$ | typ. | 100 | μA |

Noise gating (pin 9)

| | | | | |
|---|---|---|---|---|
| Input voltage (peak value) | $V_{9-16M}$ | > | 0,7 | V |
| Input current (peak value) | $I_{9M}$ | > | 30 | μA |
| | | < | 10 | mA |
| Input resistance | $R_{9-16}$ | typ. | 200 | Ω |

---

1) 800 mW permissible while tubes are heating up.

## CHARACTERISTICS (continued)

Flyback pulse (pin 5)

| | | | | | |
|---|---|---|---|---|---|
| Input voltage (peak value) | $V_{5-16M}$ | typ. | ±1 | V | |
| Input current (peak value) | $I_{5M}$ | ><br>typ. | 50<br>1 | μA<br>mA | |
| Input resistance | $R_{5-16}$ | typ. | 400 | Ω | |
| Pulse duration at 15625 Hz | $t_5$ | > | 10 | μs | |

**Delivered output signals**

Composite sync pulses (positive; pin 7)

| | | | | | |
|---|---|---|---|---|---|
| Output voltage (peak-to-peak value) | $V_{7-16(p-p)}$ | typ. | 10 | V | |
| Output resistance | | | | | |
| at leading edge of pulse (emitter follower) | $R_{7-16}$ | ≈ | 50 | Ω | |
| at trailing edge | $R_{7-16}$ | typ. | 2, 2 | kΩ | |
| Additional external load resistance | $R_{7-16(ext)}$ | > | 2 | kΩ | |

Driver pulse (pin 2)

| | | | | | |
|---|---|---|---|---|---|
| Output voltage (peak-to-peak value) | $V_{2-16(p-p)}$ | typ. | 10 | V | |
| Average output current | $I_{2(AV)}$ | < | 20 | mA | |
| Peak output current | $I_{2M}$ | < | 200 | mA | |
| Output resistance (low ohmic) | $R_{2-16}$ | typ. | 2,5 or 15 | Ω | 1) |
| Output pulse duration when synchronised | $t_2$ | | 12 to 32 | μs | 2) |
| Permissible delay between leading edge of output pulse and flyback pulse at $t_5 = 12$ μs | $t_{o\ tot}$ | | 0 to 15 | μs | |
| Supply voltage at which output pulses are obtained | $V_{1-16}$ | > | 4 | V | |

---

1) Depends on switch position and polarity output current. $R_{2-16} = 2,5\ \Omega$ is valid for $V_{2-16} = +10,5$ V and a load between pins 2 and 16 (e.g. an external resistor).

2) The output pulse duration is adjusted by shifting the leading edge ($V_{3-16}$ from 6 V to 8 V). The pulse duration is a result of delay in the line output device and the action of the second control loop in the TBA920.
For a line output stage with a BU108 high voltage transistor the resulting duration is about 22 μs, and in such a way that the line output transistor is switched on again about 8 μs after the middle of the line flyback pulse. This pulse duration must be taken into account when designing the driver stage and driver transformer as this way of driving the line output device differs from the usual, i.e. a driver duty cycle of about 50%.

### CHARACTERISTICS (continued)

Oscillator

| | | | | | |
|---|---|---|---|---|---|
| Frequency; free running ($R_{15-16}$ = 3, 3 kΩ) | $f_o$ | | 15 625 | Hz | 1) |
| Spread of frequency at nominal values of peripheral components | $\frac{\Delta f_o}{f_o}$ | < | ±5 | % | 2) |
| Frequency change when decreasing the supply down to minimum 4 V | $\left\lvert\frac{\Delta f_o}{f_o}\right\rvert$ | < | 10 | % | |
| Frequency control sensitivity | $\frac{\Delta f_o}{\Delta I_{15}}$ | typ. | 16, 5 | Hz/μA | |
| Adjustment range of network in circuit on page 6 | $\frac{\Delta f_o}{f_o}$ | typ. | ±10 | % | |
| Influence of supply voltage on frequency at $V_P$ = 12 V | $\frac{\delta f_o}{f_o} \Big/ \frac{\delta V_P}{V_{Pnom}}$ | < | 5 | % | |

Control loop 1 (between sync pulse and oscillator)

| | | | | | |
|---|---|---|---|---|---|
| Control voltage range | $V_{12-16}$ | | 0, 8 to 5, 5 | V | |
| Control current (peak values) | | | | | |
| at $V_{10-16} > 4,5$ V; $V_{6-16} > 1,5$ V | $I_{12M}$ | typ. | ±2 | mA | |
| at $V_{10-16} < 2$ V; $V_{6-16} > 1,5$ V | $I_{12M}$ | typ. | ±6 | mA | |
| Loopgain of APC system | | | | | |
| a. Time coincidence between sync pulse and flyback pulse or $V_{10-16} > 4,5$ V | $\frac{\Delta f}{\Delta t}$ | typ. | 1 | kHz/μs | |
| b. No time coincidence or $V_{10-16} < 2$ V | $\frac{\Delta f}{\Delta t}$ | typ. | 3 | kHz/μs | |
| Catching and holding range | $\Delta f$ | typ. | ±1 | kHz | 3) |

---

1) The oscillator frequency can be changed for other t.v. standards by an appropriate value of $C_{14-16}$.

2) Exclusive external components tolerances.

3) Adjustable with $R_{12-15}$.

**CHARACTERISTICS** (continued)

| | | | | | |
|---|---|---|---|---|---|
| Pull-in time for $\Delta f/f_0 = \pm 3\%$ ($\Delta f$ = 470 Hz) | t | ≈ | 20 | ms | 1) |
| Switch-over from large control sensitivity to small control sensitivity after catching | t | ≈ | 20 | ms | 1) |
| Control loop II (between flyback pulse and oscillator) | | | | | |
| Permissible delay between leading edge of output pulse (pin 2) and leading edge of flyback pulse | $t_{d\ tot}$ | | 0 to 15 | μs | |
| Static control error | $\frac{\Delta t}{\Delta t_d}$ | < | 0, 5 | % | 2) |
| Output current during flyback pulse (peak value) | $I_{4M}$ | typ. | ±0, 7 | mA | |
| Overall phase relation | | | | | |
| Phase relation between leading edge of sync pulse and middle of flyback pulse | t | typ. | 4, 9 | μs | 3) |
| Tolerance of phase relation | $\lvert \Delta t \rvert$ | < | 1 | μs | 4) |
| Voltage for $T_2$ = 12 to 32 μs | $V_{3-16}$ | | 6 to 8 | V | |
| Adjustment sensitivity | $\frac{\Delta T2}{\Delta V_{3-16}}$ | typ. | 10 | μs/V | |
| Input current | $I_3$ | < | 2 | μA | |

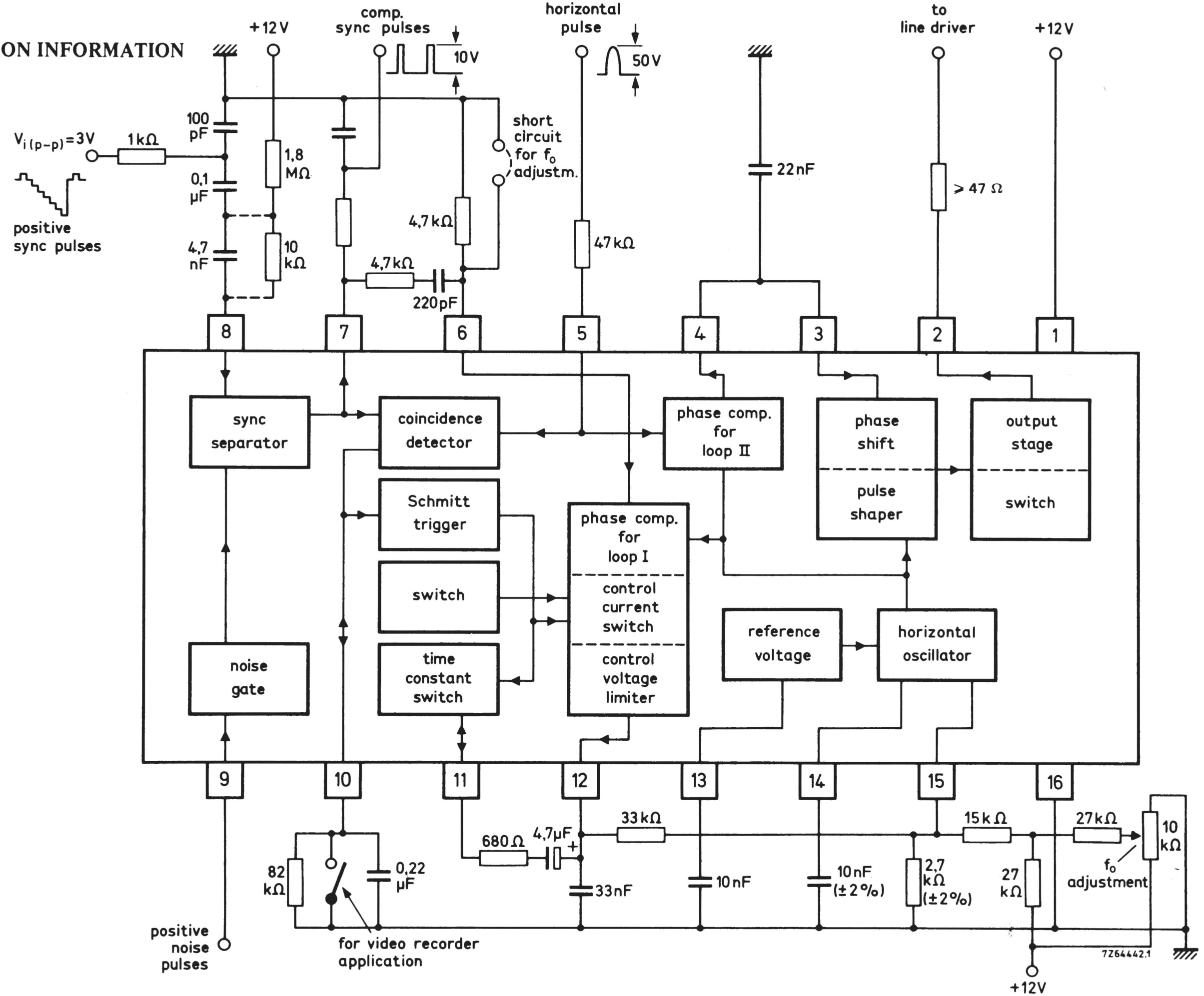
External switch-over of parameters (loop filter and loop gain) of control loop I (e.g. for video recorder application) see note 5.

| | | | | | |
|---|---|---|---|---|---|
| Required switch-over voltage | | | | | |
| at $R_{11-16}$ = 150 Ω | $V_{10-16}$ | > | 4, 5 | V | |
| at $R_{11-16}$ = 2 kΩ | $V_{10-16}$ | < | 2 | V | |
| Required switch-over current | | | | | |
| at $R_{11-16}$ = 150 Ω; $V_{10-16}$ = 4, 5 V | $I_{10}$ | typ. | 80 | μA | 5) |
| at $R_{11-16}$ = 2 kΩ; $V_{10-16}$ = 2 V | $I_{10}$ | typ. | 120 | μA | |

---

1) See application information circuit on page 6.
2) The control error is the remaining error in reference to the nominal phase position between leading edge of the sync pulse and the middle of the flyback pulse caused by a variation in delay of the line output stage.
3) This phase relation assumes a luminance delay line with a delay of 500 ns between the input of the sync separator and the drive to the picuture tube. If the sync separator is inserted after the luminance delay line or if there is no delay line at all (black-and-white sets), then the phase relation is achieved at $C_{5-16}$ = 560 pF.
4) The adjustment of the overall phase relation and consequently the leading edge of the output pulse at pin 2 occurs automatically by the control loop II or by applying a d.c. voltage to pin 3.
5) With sync pulses at pin 7 and 8; without RC network at pin 10.

## APPLICATION INFORMATION

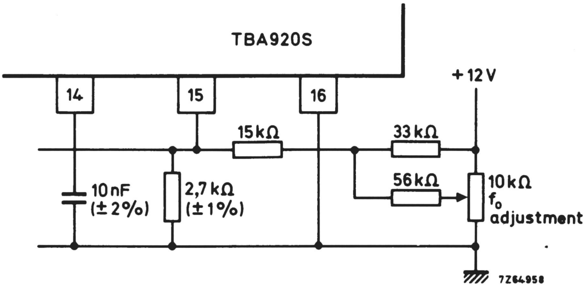

+12V
comp.
sync pulses
10V
horizontal
pulse
50V
to
line driver
+12V
Vi(p-p)=3V
1kΩ
positive
sync pulses
100
pF
0,1
μF
4,7
nF
1,8
MΩ
10
kΩ
short
circuit
for fo
adjustm.
4,7kΩ
4,7kΩ
220pF
47kΩ
22nF
≥ 47 Ω
8
7
6
5
4
3
2
1
sync
separator
coincidence
detector
phase comp.
for
loop II
phase
shift
pulse
shaper
output
stage
switch
Schmitt
trigger
switch
time
constant
switch
phase comp.
for
loop I
control
current
switch
control
voltage
limiter
reference
voltage
horizontal
oscillator
noise
gate
9
10
11
12
13
14
15
16
82
kΩ
0,22
μF
for video recorder
application
positive
noise
pulses
680Ω
4,7μF
+
33nF
33kΩ
10nF
10nF
(±2%)
2,7
kΩ
(±2%)
15kΩ
27
kΩ
27kΩ
10
kΩ
fo
adjustment
+12V
7Z64442.1

# HORIZONTAL COMBINATION

The TBA920S is identical to the TBA920, except for the following data:

Oscillator

| | | | | |
|---|---|---|---|---|
| Spread of frequency at<br>$R_{15-16}$ = 3,3 kΩ; $C_{14-16}$ = 10 nF | $\frac{\Delta f_o}{f_o}$ | < | 1,5 | % |
| Adjustment range of frequency<br>(in network below) | $\frac{\Delta f_o}{f_o}$ | typ. | ± 5 | % |

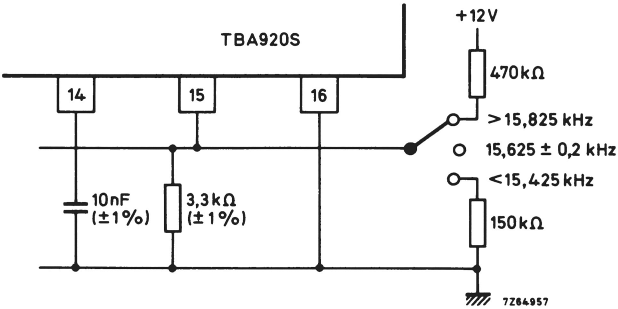

TBA920S
14
15
16
+12 V
15 kΩ
33 kΩ
56 kΩ
10 kΩ
$f_o$
adjustment
10 nF
(± 2%)
2,7 kΩ
(± 1%)
7Z64958

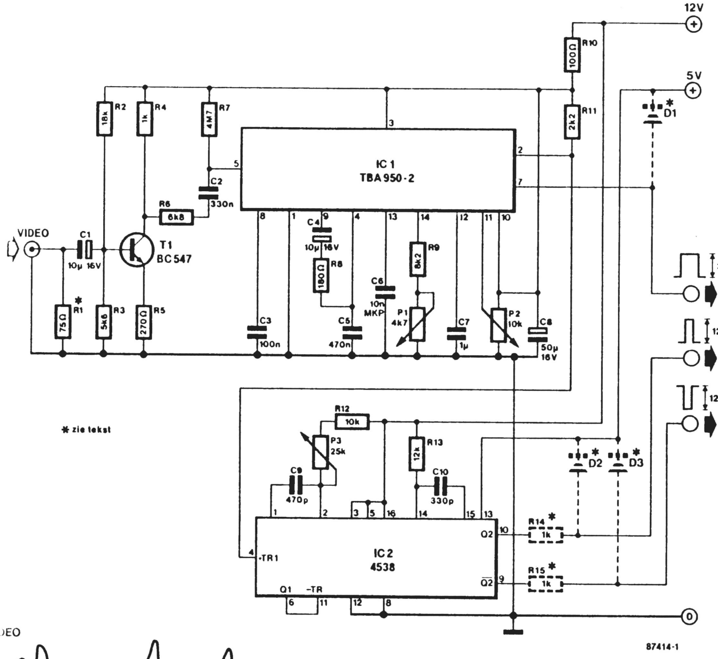
Note: The above network is the only part that differs from the circuit given on page 6 of TBA920 data.

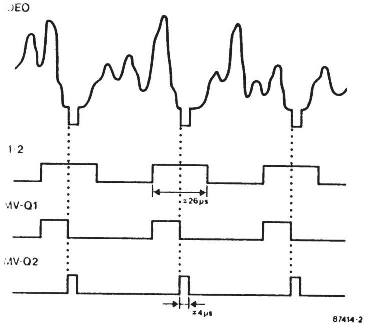
Overall phase relation

| | | | | |
|---|---|---|---|---|
| Tolerance of phase relation between<br>leading edge of sync pulse and<br>middle of flyback pulse | $\lvert\Delta t\rvert$ | < | 0,4 | µs |

Other circuit possibilities for oscillator frequency adjustment


TBA920S
14
15
16
+12 V
470 kΩ
> 15,825 kHz
15,625 ± 0,2 kHz
< 15,425 kHz
150 kΩ
10 nF
(± 1%)
3,3 kΩ
(± 1%)
7Z64957


12V
5V
R10
100Ω
R11
2k2
D1
VIDEO
C1
10µ 16V
R1
75Ω
R2
18k
R3
5k6
R4
1k
R5
270Ω
R6
6k8
R7
4M7
C2
330n
T1
BC547
IC 1
TBA 950-2
C3
100n
C4
10µ 16V
R8
180Ω
C5
470n
C6
10n
MKP
R9
8k2
P1
4k7
C7
1µ
P2
10k
C8
50µ
16V
>8V
12V
12V
R12
10k
P3
25k
R13
12k
C9
470p
C10
330p
D2
D3
R14
1k
R15
1k
IC2
4538
+TR1
Q1
-TR
Q2
Q̄2
0
* zie tekst
87414-1


EO
-2
≈26µs
MV-Q1
MV-Q2
≈4µs
87414-2

instellen op stilstaand beeld. P3 verdraaien totdat de juiste beeldpositie wordt bereikt. Mocht hierbij de juiste beeldpositie niet kunnen worden bereikt, verdraai dan P2 (fase) een beetje en probeer dan nog eens met P3.
Op pen 7 van IC1 staat tenslotte de raster-syncpuls.

N.B. De uitgangsamplitudes liggen ruim boven TTL-nivo. Om op TTL-nivo te komen, kunnen D1 t/m D3 en R14, R15 worden toegevoegd.

# CHROMINANCE AMPLIFIER FOR SECAM OR PAL/SECAM DECODERS

The TCA640 is an integrated chrominance amplifier for either a SECAM decoder or a double standard PAL/SECAM decoder.
Switching of the standard is performed internally, controlled by an external applied d.c. signal.
In addition to the chrominance amplifier the circuit also incorporates a 7, 8 kHz flip-flop and an identification circuit for SECAM.
For PAL identification the circuit included in the TBA540 should be used.
Furthermore, the TCA640 incorporates a blanking circuit, a burst gating circuit and a colour killer detector.

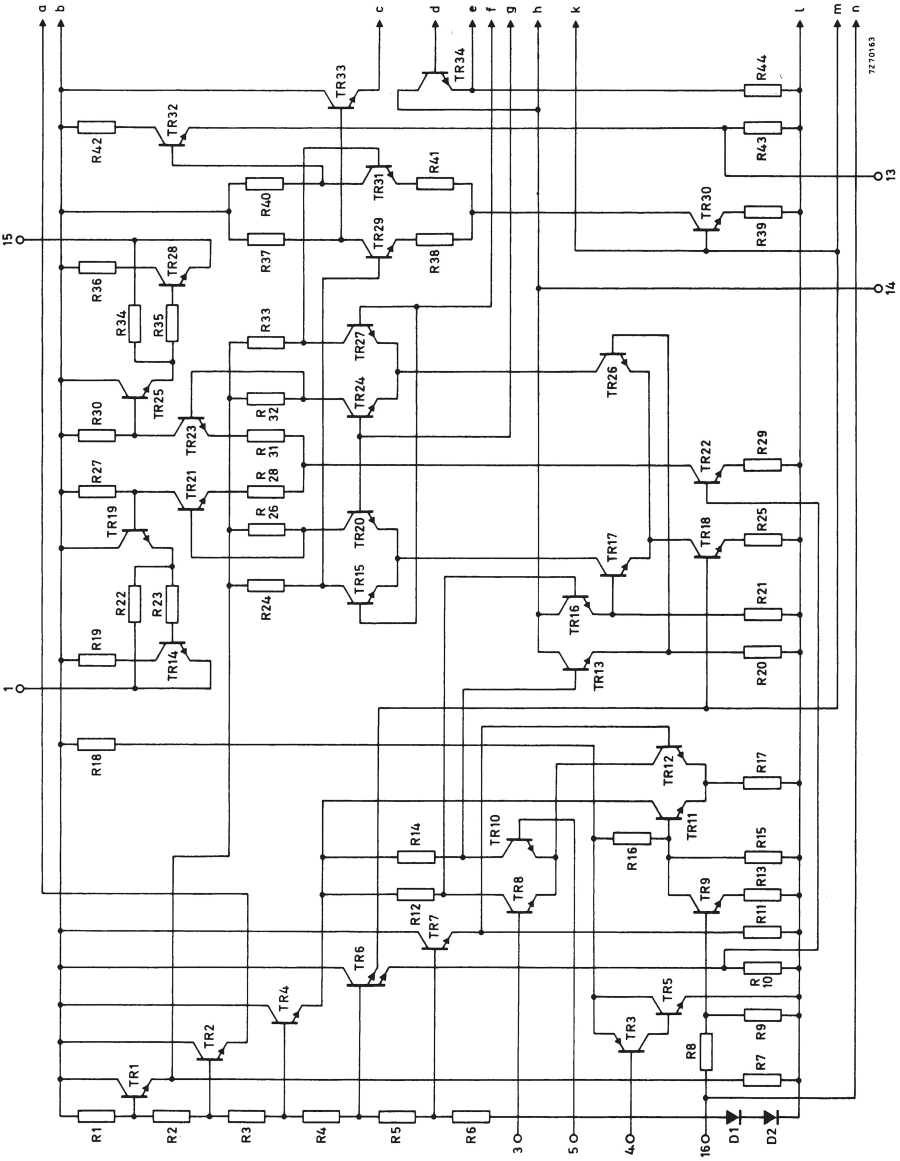
**QUICK REFERENCE DATA**

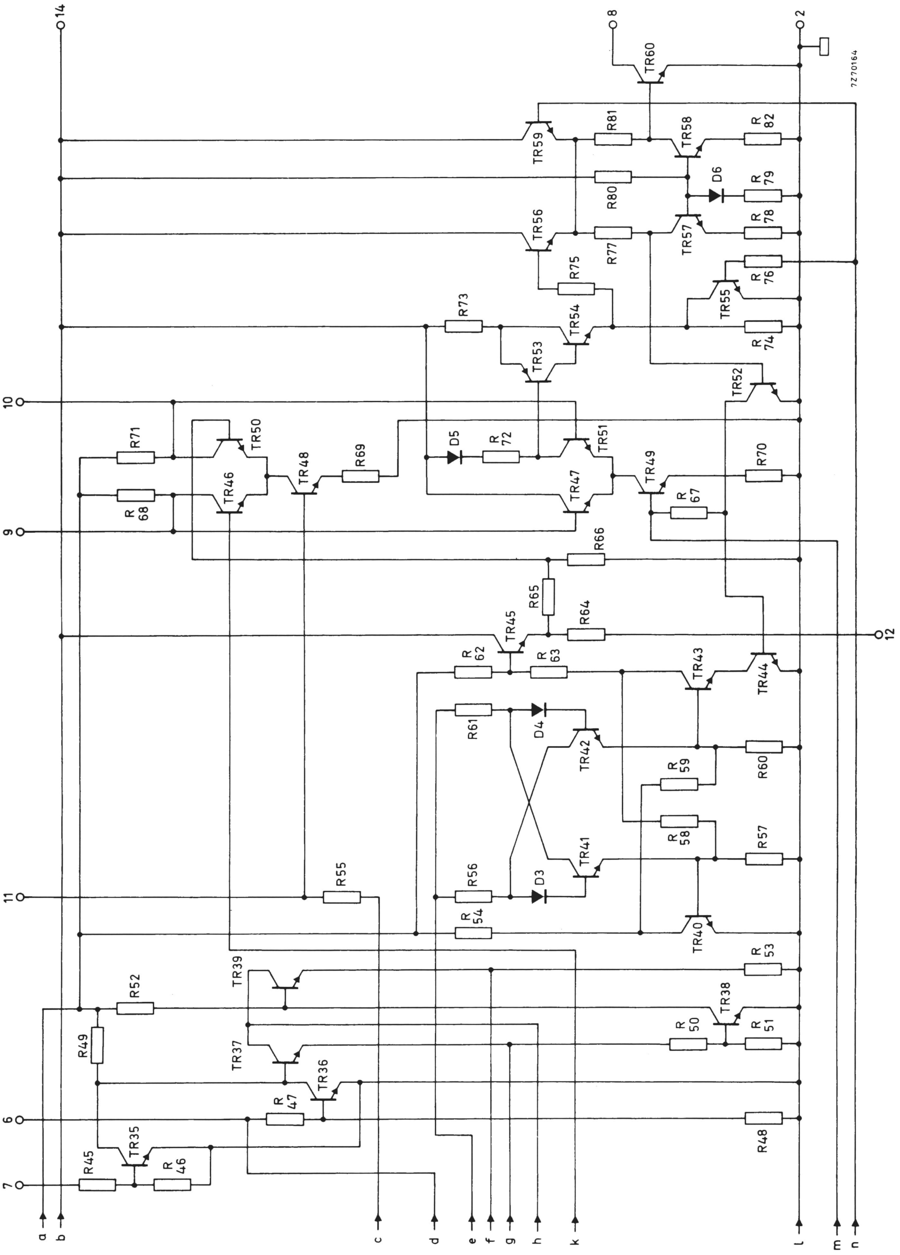
| | | | | |
|---|---|---|---|---|
| Supply voltage | $V_{14-2}$ | nom. | 12 | V |
| Supply current | $I_{14}$ | nom. | 37 | mA |

| | | | PAL | SECAM | |
|---|---|---|---|---|---|
| Chrominance input signals (peak-to-peak value) | $V_{3-5(p-p)}$ | > | 4 | 7 | mV |
| | | < | 80 | 400 | mV |
| Chrominance output signals (peak-to-peak value) | $V_{15-2\,(p-p)}$<br>$V_{1-2\,(p-p)}$ | typ. | 500 | 2000 | mV |
| Burst output (closed a.c.c. loop) (peak-to-peak value) | $V_{13-2(p-p)}$ | typ. | 1 | – | V |
| System switching signal | $V_{4-2}$ | typ. | 12 | 0 | V |
| Burst blanking of chrominance signal | | > | 40 | – | dB |
| Chrominance blanking at field identification | | > | – | 40 | dB |
| Square-wave output (7, 8 kHz) (peak-to-peak value) | $V_{12-2(p-p)}$ | typ. | 3 | 3 | V |

**PACKAGE OUTLINE**

16-lead DIL; plastic (SOT-38).


a
b
c
d
e
f
g
h
k
l
m
n
1
3
4
5
13
14
15
16
7Z70163
TR1
TR2
TR3
TR4
TR5
TR6
TR7
TR8
TR9
TR10
TR11
TR12
TR13
TR14
TR15
TR16
TR17
TR18
TR19
TR20
TR21
TR22
TR23
TR24
TR25
TR26
TR27
TR28
TR29
TR30
TR31
TR32
TR33
TR34
R1
R2
R3
R4
R5
R6
R7
R8
R9
R10
R11
R12
R13
R14
R15
R16
R17
R18
R19
R20
R21
R22
R23
R24
R25
R26
R27
R28
R29
R30
R31
R32
R33
R34
R35
R36
R37
R38
R39
R40
R41
R42
R43
R44
D1
D2


14
8
2
7Z70164
TR60
TR59
R81
TR58
R 82
R80
D6
R 79
TR56
R77
TR57
R 78
R75
R 76
TR55
R73
TR54
R 74
TR53
TR52
10
R71
TR50
TR51
D5
R 72
R69
TR48
TR46
TR47
TR49
R70
R 68
R 67
9
R66
R65
TR45
R64
12
R 62
R 63
TR43
TR44
R61
D4
TR42
R60
R 59
R 58
TR41
R57
11
R55
R56
D3
R 54
TR40
TR39
R 53
R52
TR38
R49
R 50
R 51
TR37
TR36
R 47
6
R48
TR35
R45
R 46
7
a
b
c
d
e
f
g
h
k
l
m
n

**RATINGS** Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | |
|---|---|---|---|
| Voltage | | | |
| Supply voltage | $V_{14-2}$ | max. | 13,2 V |
| Power dissipation | | | |
| Total power dissipation | $P_{tot}$ | max. | 625 mW |
| Temperatures | | | |
| Storage temperature | $T_{stg}$ | | −25 to +125 °C |
| Operating ambient temperature | $T_{amb}$ | | −25 to +65 °C (1) |

**CHARACTERISTICS** measured in the circuit on page 6

| | | | | |
|---|---|---|---|---|
| Supply voltage | $V_{14-2}$ | | typ. | 12 V |
| | | | | 10,2 to 13,2 V |

**Required input signals** at $V_{14-2}$ = 12 V and $T_{amb}$ = 25 °C

| | | | | |
|---|---|---|---|---|
| Chrominance input signal | | | | |
| peak-to-peak value | $V_{3-5(p-p)}$ | PAL | | 4 to 80 mV |
| | | SECAM | | 7 (2) to 400 mV |
| Automatic chrominance control starting | $V_{16-2}$ | PAL | typ. | 1,2 V (3) |
| Flyback pulses for blanking and burst/identification lines-keying | | | See note 4 | |
| Line flyback pulses (positive) | | | | |
| peak-to-peak value | $V_{6-2(p-p)}$ | | | 4,5 to 12 V |
| Field idenfication pulses (positive) | | | | |
| peak-to-peak value | $V_{7-2(p-p)}$ | | | 4 to 12 V |
| System switch signal | $V_{4-2}$ | PAL | | 7 to $V_{14-2}$ V |
| | | SECAM | | 0 to 1 V |
| Colour killer threshold | $V_{16-2}$ | PAL | typ. | 2,5 V (5) |

---

(1) When a stabilized power supply of ⩽12 V is applied, $T_{amb}$ is max. 75 °C.

(2) Start of limiting.

(3) A negative-going potential provides a 26 dB a.c.c. range.

(4) The line flyback pulses also provide the clock pulses for the flip-flop.

(5) The colour killer is operative above the quoted input voltage.

**CHARACTERISTICS** (continued)

**Obtainable output signals**

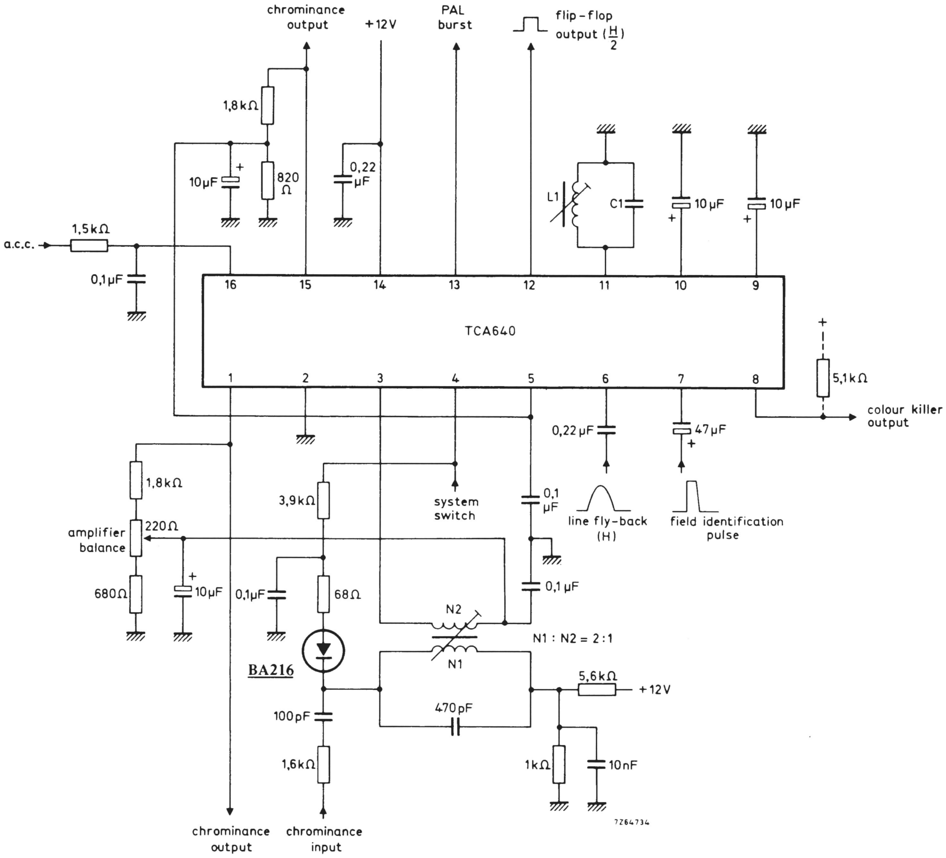
| | | | | | | | |
|---|---|---|---|---|---|---|---|
| Chrominance output signals | | | | | | | |
| peak-to-peak value | | $V_{15-2(p-p)}$ | PAL | | 425 to 575 | mV | |
| | | $V_{1-2(p-p)}$ | SECAM | | 1, 8 to 2, 3 | V | |
| Phase difference between output pins | | $\Delta\varphi_{15-1}$ | PAL | | 170° to 190° | | 1) |
| Burst signal (peak-to-peak value) | | $V_{13-2(p-p)}$ | PAL | typ. | 1 | | 2) |
| Identification signal | | | | | | | |
| peak-to-peak value | | $I_{11(p-p)}$ | SECAM | | 1, 4 to 2, 4 | mA | |
| Output resistance | | $R_{11-2}$ | | | 2 to 2, 9 | kΩ | |
| Flip-flop signal | | | | | | | |
| peak-to-peak value | | $V_{12-2(p-p)}$ | | | 2, 5 to 3, 5 | V | |
| Colour killer | killed | $V_{8-2}$ | | < | 0, 5 | V | |
| | | $I_8$ | | < | 10 | mA | |
| | unkilled | $V_{8-2}$ | | | $V_{14-2}$ | V | |
| | | $I_8$ | | < | 10 | μA | |
| Bandwidth of chrominance amplifier (−1 dB) | | | | | | | |
| at a carrier frequency of 4, 2 MHz | | | | > | ± 1 | MHz | |
| Blanking | | | | | | | |
| burst rejection | | | PAL | > | 40 | dB | |
| rejection identification lines with field identification | | | SECAM | > | 40 | dB | |

---

1) Over the a.c.c. control range the phase difference varies less than 2, 5°.

2) The burst is kept constant at 1 V peak-to-peak by automatic gain control.

## APPLICATION INFORMATION


chrominance output
+12V
PAL burst
flip-flop output ($\frac{H}{2}$)
1,8kΩ
10µF
820 Ω
0,22 µF
L1
C1
10µF
10µF
a.c.c.
1,5kΩ
0,1µF
16
15
14
13
12
11
10
9
TCA640
1
2
3
4
5
6
7
8
5,1kΩ
colour killer output
0,22µF
47µF
line fly-back (H)
field identification pulse
1,8kΩ
3,9kΩ
system switch
0,1 µF
amplifier balance
220Ω
680Ω
10µF
0,1µF
68Ω
0,1 µF
N2
N1
N1 : N2 = 2:1
BA216
5,6kΩ
+12V
470pF
100pF
1,6kΩ
1kΩ
10nF
chrominance output
chrominance input
7Z64734

### Pinning

1. Chrominance output
2. Earth (negative supply)
3. Chrominance input
4. System switch input
5. Chrominance input
6. Line fly-back pulse input
7. Field identification pulse input
8. Colour killer output
9. } Identification integrating
10. } capacitor (SECAM)
11. Identification tank circuit (SECAM)
12. Flip-flop output
13. Burst output (PAL)
14. Supply voltage (12 V)
15. Chrominance output
16. A.C.C. input

## APPLICATION INFORMATION (continued)

**The function is quoted against the corresponding pin number**

1. Chrominance output (in conjunction with pin 15)

   A balanced output is available at pins 1 and 15.
   At SECAM reception a limited signal of 2 V peak-to-peak is available, starting from an input voltage of 15 mV peak-to-peak.
   At PAL reception the output signal is 500 mV peak-to-peak for a burst signal of 1 V peak-to-peak.
   An external d.c. network is required which provides negative feedback to pin 3. The same holds for the feedback from pin 15 to pin 5.
   The figures for input and output signals are based on a 100% saturated colour bar signal.

2. Negative supply (earth)

3. Chrominance input (in conjunction with pin 5)

   The input signal is derived from a bandpass filter which provides the required "bell" shape bandpass for the SECAM signal and a flat bandpass for the PAL signal.
   The input signal can be supplied either in a balanced mode or single ended. Both inputs (pins 3 and 5) require a d.c. potential of about 2,5 V obtained from a resistive divider connected to output pins 1 and 15. The figures for the input signals are based on a 100% saturated colour bar signal and a burst-to-chrominance ratio of 1:3 of the input signal (PAL).

4. System switch input

   Between 7 V and the supply voltage, the gain of the chrominance amplifier is controlled by the a.c.c. voltage at pin 16.
   The chrominance amplifier then provides linear amplification required for the PAL signal.
   Between 0 V and 1 V the chrominance amplifier operates as a limiter for the SECAM signal.

5. Chrominance input (see pin 3)

6. Line fly-back pulse input (in conjunction with pin 11)

   Positive going pulses provide

   - blanking of the chrominance signal at the outputs (pins 1 and 15).
   - burst gating for both PAL and SECAM.
     The carrier signal present during the second half of the back porch of the SECAM signal is gated. It provides line identification when the circuit $L_1C_1$ (see circuit on page 6) is tuned to 4,25 MHz (at $C_1$ = 470 pF).
   - trigger signal for the flip-flop.

7. Field identification pulse input (in conjunction with pin 11)

   Like the line fly-back pulses, positive going identification pulses provide blanking and burst gating.
   To operate the TCA640 on the identification lines (SECAM) in the field blanking period the circuit $L_1C_1$ (see circuit on page 6) should be tuned to 3,9 MHz and the capacitor $C_1$ should be increased to 1 nF. The field fly-back pulse should be shaped so that its amplitude exceeds 4 V during the identification lines.

## APPLICATION INFORMATION (continued)

8. Colour killer output

   This pin is driven from the collector of an internal switching transistor and requires an external load resistor connected to the supply voltage. The killer is operative when the a.c.c. voltage exceeds the threshold, when the SECAM chrominance signal at the input is below the limiting level or when the flip-flop operates in the wrong phase.

9. Identification integrating capacitor (SECAM)

10. Identification integrating capacitor (SECAM)

11. Identification detector tank circuit (see pins 6 and 7)

12. Flip-flop output

    A square wave of 7,8 kHz with an amplitude of 3 V is available at this pin.
    An external load resistor is not required.

13. Burst output (PAL)

    A 1 V peak-to-peak burst (kept constant by the a.c.c. system) is produced here.

14. Supply voltage (12 V)

    Correct operation occurs within the range 10,2 to 13,2 V.
    The power dissipation must not exceed 625 mW at 65 °C ambient temperature.

15. Chrominance output (see pin 1)

16. A.C.C. input

    With the system switch input (pin 4) connected for PAL operation, a negative going potential gives a 26 dB range of a.c.c. starting at + 1,2 V
    During SECAM operation, the voltage at the input should not exceed + 0,5 V, otherwise the SECAM identification circuit and the colour killer become inoperative.

# CHROMINANCE DEMODULATOR FOR SECAM OR PAL/SECAM DECODERS

The TCA650 is an integrated synchronous demodulator for both the SECAM and PAL chrominance signals.
Switching of the standard is performed internally, controlled by an external applied d.c. signal.
In addition to the synchronous demodulator, which delivers colour difference signals, the circuit also incorporates:

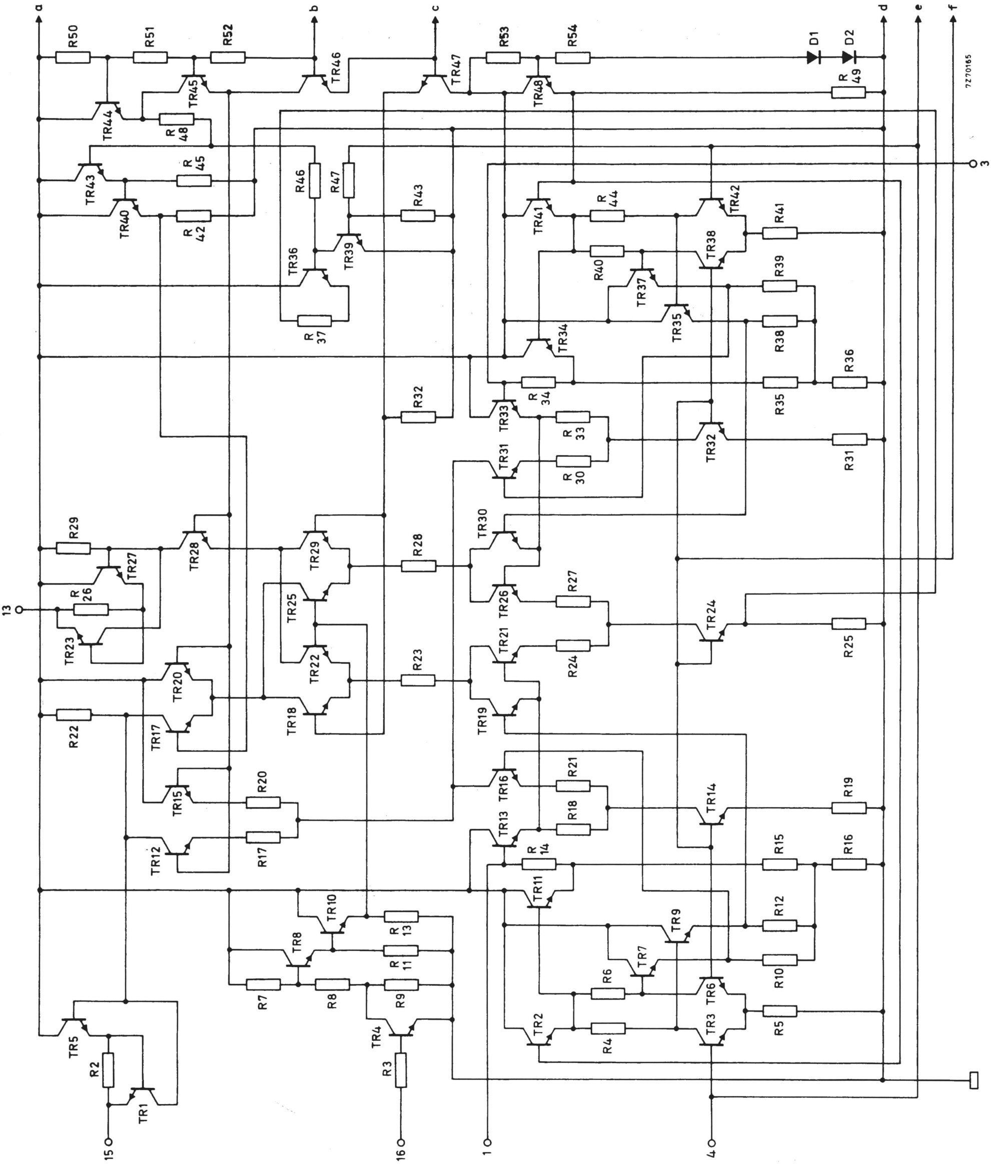
- a PAL matrix, used for adding the delayed and non-delayed signals to obtain separately the (R-Y) and (B-Y) components of the chrominance signal.
- a PAL switch, which reverses the phase of the (R-Y) component of the chrominance signal on alternating lines.
- a SECAM switch, which performs the separation of the $D_R$ and $D_B$ components of the chrominance signal by switching the delayed and non-delayed signals.
- a SECAM limiter.

## QUICK REFERENCE DATA

| | | | | | | |
|---|---|---|---|---|---|---|
| Supply voltage | | $V_{14-2}$ | nom. | | 12 | V |
| Supply current | | $I_{14}$ | nom. | | 36 | mA |
| | | | | PAL | SECAM | |
| Chrominance input signals (peak-to-peak value) | | $V_{1-2(p-p)}$<br>$V_{3-2(p-p)}$ | typ. | 50 | 200 | mV |
| System switch input | | $V_{4-2}$ | typ. | 12 | 0 | V |
| Colour difference output signals (peak-to-peak value) | (R-Y): | $V_{12-2(p-p)}$ | typ. | | 1,1 | V |
| | (B-Y): | $V_{10-2(p-p)}$ | typ. | | 1,47 | V |
| Reference input signals (PAL) (peak-to-peak value) | | $V_{6-2(p-p)}$<br>$V_{7-2(p-p)}$ | typ. | | 1 | V |
| Square-wave input (peak-to-peak value) | | $V_{16-2(p-p)}$ | typ. | | 3 | V |

**PACKAGE OUTLINE**

16-lead DIL; plastic (SOT-38).


a
b
c
d
e
f
3
13
15
16
1
4
7Z70165
D1
D2
R50
R51
R52
R53
R54
R49
TR44
TR45
TR46
TR47
TR48
R48
TR43
TR40
R45
R42
R46
R47
R43
TR36
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TR16
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TR14
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TR10
R13
TR9
R12
TR8
R11
TR7
R10
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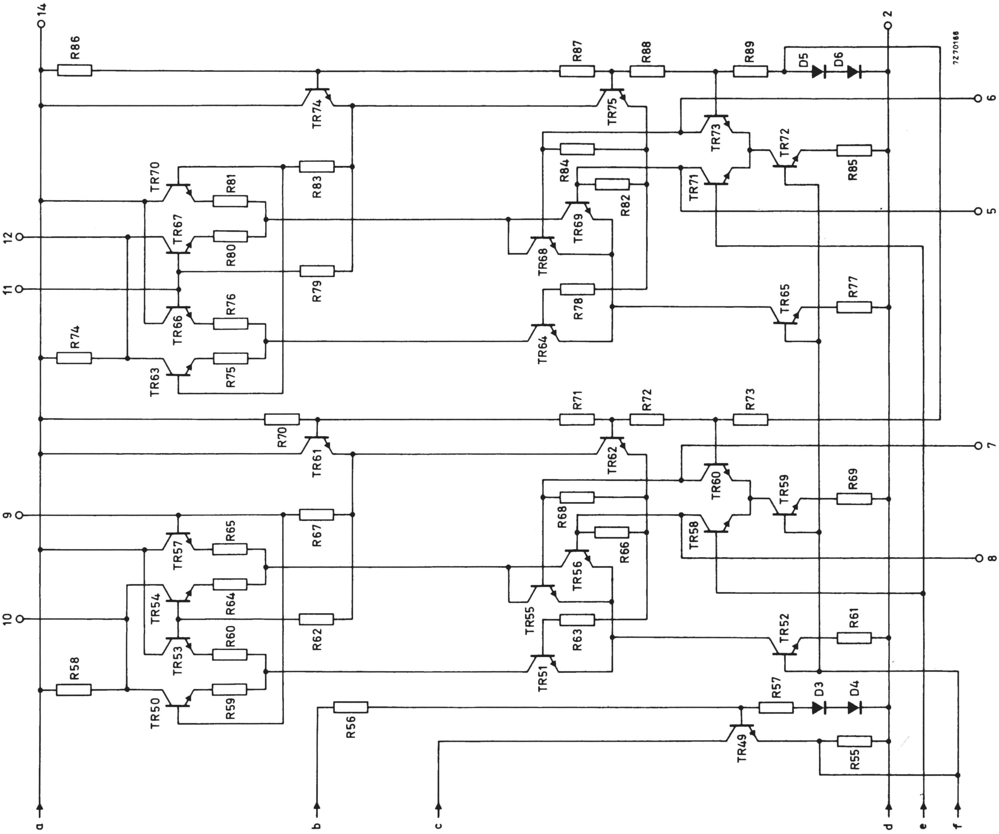
R4
TR3
R5
TR5
R2
TR4
R3
TR1


14
12
11
9
10
2
6
5
7
8
a
b
c
d
e
f
R86
R87
R88
R89
D5
D6
TR74
TR75
TR73
TR72
TR71
TR70
R81
R83
R84
R82
R85
TR67
R80
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TR68
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TR60
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R67
TR57
R65
R66
TR58
TR56
TR54
R64
TR55
R62
R63
R61
TR52
R60
TR53
R58
TR50
R59
TR51
R57
D3
D4
R56
TR49
R55
7Z70188

**RATINGS** Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | | |
|---|---|---|---|---|
| Voltage | | | | |
| Supply voltage | $V_{14-2}$ | max. | 13,2 | V |
| Power dissipation | | | | |
| Total power dissipation | $P_{tot}$ | max. | 510 | mW |
| Temperatures | | | | |
| Storage temperature | $T_{stg}$ | | −25 to +125 | °C |
| Operating ambient temperature | $T_{amb}$ | | −25 to +65 | °C 1) |

**CHARACTERISTICS** measured in the circuit on page 6

| | | | | | |
|---|---|---|---|---|---|
| Supply voltage | $V_{14-2}$ | | typ. | 12 | V |
| | | | | 10,2 to 13,2 | V |

**Required input signals** at $V_{14-2}$ = 12 V and $T_{amb}$ = 25 °C

| | | | | | |
|---|---|---|---|---|---|
| Chrominance input signal | | | | | |
| peak-to-peak value | $V_{1-2(p-p)}$ | PAL | | 35 to 75 | mV |
| | $V_{3-2(p-p)}$ | SECAM | | 150 to 400 | mV |
| Input impedance | $\|Z_{1-2}\|$<br>$\|Z_{3-2}\|$ | | | 1,2 to 2,6 | kΩ |
| PAL matrix | | | | | |
| Gain from both inputs to pin 13 | | | | 2,3 to 3,3 | |
| Gain from both inputs to pin 15 | | | | 2,6 to 3,6 | |
| Gain difference from line-to-line | | | < | 5 | % |
| Phase errors from line-to-line in the (R-Y) output for zero error in the (B-Y) output | | | < | 2,5° | |
| Output impedance | $\|Z_{13-2}\|$<br>$\|Z_{15-2}\|$ | | < | 100 | Ω |
| SECAM permutator | | | | | |
| Diaphotie | | | < | −46 | dB |
| Output signal (peak-to-peak value) | $V_{13-2(p-p)}$<br>$V_{15-2(p-p)}$ | | | 1,6 2) to 2,2 | V |
| Output impedance | $\|Z_{13-2}\|$<br>$\|Z_{15-2}\|$ | | < | 100 | Ω |

---

1) When a stabilized power supply of ≤ 12 V is applied, $T_{amb}$ is max. 75 °C.

2) At an input voltage of 0, 15 V; at an input voltage > 0, 2 V the figure is 1, 7 V.

## CHARACTERISTICS (continued)

### Demodulator

| | | | | |
|---|---|---|---|---|
| Chrominance input signal amplitude | | | | |
| PAL: (B-Y); peak-to-peak value | $V_{9-2(p-p)}$ | typ. | 0,22 | V |
| (R-Y); peak-to-peak value | $V_{11-2(p-p)}$ | typ. | 0,28 | V |
| SECAM: peak-to-peak value | $V_{9-2(p-p)}$<br>$V_{11-2(p-p)}$ | | 1,5 to 3 | V |
| Input impedance | $\lvert Z_{9-2}\rvert$<br>$\lvert Z_{11-2}\rvert$ | > | 1 | kΩ |
| Reference input signal amplitude | | | | |
| PAL: peak-to-peak value | $V_{6-2(p-p)}$<br>$V_{7-2(p-p)}$ | | 0,5 to 1,5 | V |
| SECAM: peak-to-peak value | $V_{5-2(p-p)}$<br>$V_{8-2(p-p)}$ | | 0,18 [1] to 1,5 | V |
| Input impedance | $\lvert Z_{5-2}\rvert$; $\lvert Z_{7-2}\rvert$<br>$\lvert Z_{6-2}\rvert$; $\lvert Z_{8-2}\rvert$ | | 0,75 to 1,25 | kΩ |

### Colour difference output signal

| | | | | |
|---|---|---|---|---|
| (R-Y); peak-to-peak value | $V_{12-2(p-p)}$ | | 0,99 to 1,21 | V [2] |
| (B-Y); peak-to-peak value | $V_{10-2(p-p)}$ | | 1,32 to 1,62 | V [2] |
| Output impedance | $\lvert Z_{10-2}\rvert$<br>$\lvert Z_{12-2}\rvert$ | | 2,4 to 4,2 | kΩ |

### Diaphotie at SECAM operation

| | | | | |
|---|---|---|---|---|
| Diaphotie of the total circuit at frequencies corresponding to saturated green $D_R$ = 4,72 MHz and $D_B$ = 4,04 MHz | | < | −40 | dB |

### Square wave input

| | | | | |
|---|---|---|---|---|
| peak-to-peak value | $V_{16-2(p-p)}$ | | 2,5 to 3,5 | V |
| Input impedance | $\lvert Z_{16-2}\rvert$ | > | 3,8 | kΩ |

### System switch input [3]

| | | | | |
|---|---|---|---|---|
| PAL: | | | 7 to $V_{14-2}$ | V |
| SECAM: | | | 0 to 1 | V |

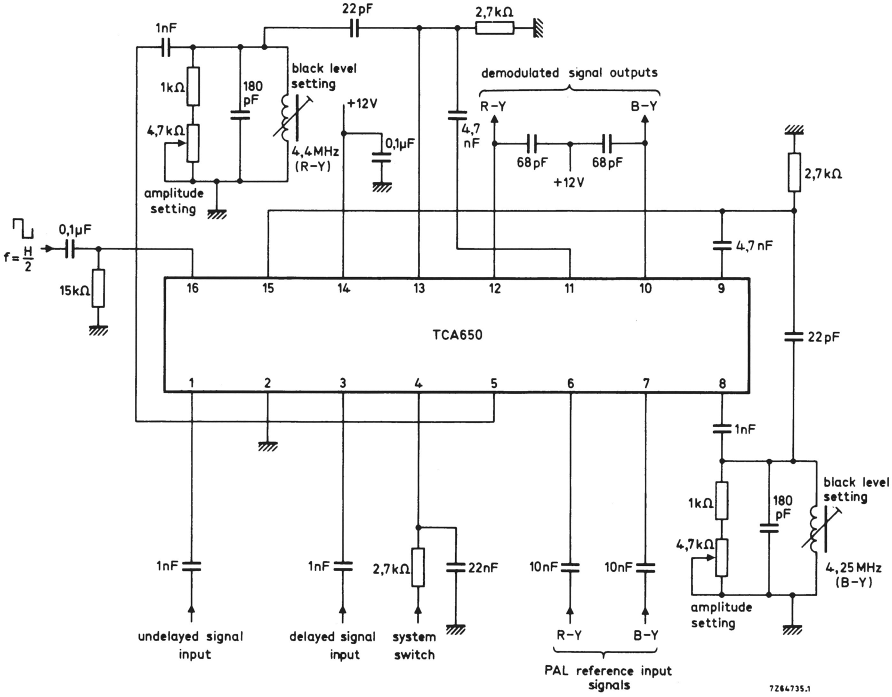
---

[1] Limiting starts at the quoted value.

[2] The peak-to-peak clipping level for PAL is about 4,7 V for (B-Y) and 3 V for (R-Y). The discriminator characteristic allows a maximum peak-to-peak output signal of 3,6 V for (B-Y) and 2,4 V for (R-Y) (SECAM).

[3] The switching signal is applied to pin 4 via a resistor of 2,7 kΩ (±10%).

## APPLICATION INFORMATION


22pF
2,7kΩ
1nF
1kΩ
180 pF
black level setting
4,7kΩ
+12V
0,1μF
4,7 nF
4,4MHz (R-Y)
amplitude setting
demodulated signal outputs
R-Y
B-Y
68pF
68pF
+12V
2,7kΩ
0,1μF
f = H/2
15kΩ
4,7nF
TCA650
22pF
1nF
1kΩ
180 pF
black level setting
4,7kΩ
4,25MHz (B-Y)
amplitude setting
1nF
1nF
2,7kΩ
22nF
10nF
10nF
undelayed signal input
delayed signal input
system switch
R-Y
B-Y
PAL reference input signals
7Z64735.1

### Pinning

1. Chrominance input
2. Earth (negative supply)
3. Chrominance input
4. System switch input
5. Reference (R-Y) input SECAM
6. Reference (R-Y) input PAL
7. Reference (B-Y) input PAL
8. Reference (B-Y) input SECAM
9. Chrominance (B-Y), $D_B$ input
10. Colour difference (B-Y) output
11. Chrominance (R-Y), $D_R$ input
12. Colour difference (R-Y) output
13. Chrominance (R-Y), $D_R$ output
14. Supply voltage (12 V)
15. Chrominance (B-Y), $D_B$ output
16. Square wave input

## APPLICATION INFORMATION (continued)

**The function is quoted against the corresponding pin number**

1. Chrominance input

   The blanked composite chrominance signal from pin 1 of the TCA640 is applied to this input via a resistive divider.

2. Negative supply (earth)

3. Chrominance input

   The blanked composite chrominance signal from pin 15 of the TCA640 is applied to this input via a delay-line, which has a delay time of 64 μs.

4. System switch input

   The control voltage for switching the standard is applied to this input via a resistor of 2,7 kΩ (± 10%). A decoupling capacitor of at least 10 nF is recommended. Between 7 V and the supply voltage the circuit operates in the PAL mode, whereas between 0 V and 1 V the mode SECAM is selected.

5. Reference input for the (R-Y) demodulator

   The SECAM reference signal is applied to this pin. The reference signal is obtained from pin 11 via a tank circuit. The tank circuit is tuned such that the level at the (R-Y) output (pin 12) during black ($f_0$ = 4,4 MHz) equals the level during blanking (no signal). The output voltage amplitude at pin 12 can be adjusted by damping the tank circuit.

6. Reference input for the (R-Y) demodulator

   A PAL reference signal having (R-Y) phase is applied to this pin.

7. Reference input for the (B-Y) demodulator

   A PAL reference signal having (B-Y) phase is applied to this pin.

8. Reference input for the (B-Y) demodulator

   The SECAM reference signal is applied to this pin. The reference signal is obtained from pin 15 via a tank circuit. The tank circuit is tuned such that the level at the (B-Y) output (pin 10) during black ($f_0$ = 4,25 MHz) equals the level during blanking (no signal). The output voltage amplitude at pin 10 can be adjusted by damping the tank circuit.

9. Chrominance input to the (B-Y), $D_B$ demodulator

   The output signal of pin 15 is applied via a coupling capacitor of 4,7 nF.

10. Output of the (B-Y) demodulator

    The output signal of the balance demodulator contains an r.f. ripple of twice the chrominance frequency to be filtered by a π filter. At SECAM the required de-emphasis circuit should be applied.

11. Chrominance input to the (R-Y), $D_R$ demodulator

    The output signal of pin 13 is applied via a coupling capacitor of 4,7 nF.

**APPLICATION INFORMATION** (continued)

12. Output of the (R-Y) demodulator

    See pin 10.

13. Chrominance (R-Y), $D_R$ output

    The (R-Y) component of the chrominance signal ($D_R$ component at SECAM) is present at this pin.
    The signal is applied to the input of the (R-Y) demodulator (pin 11) and to the tank circuit for the SECAM reference signal.
    The emitter follower output should be loaded with a 2, 7 kΩ resistor to obtain an output impedance of $<100\ \Omega$.

14. Supply voltage (12 V)

    Correct operation occurs within the range 10, 2 to 13, 2 V.
    The power dissipation must not exceed 510 mW at 65 $^{o}$C ambient temperature.

15. Chrominance (B-Y), $D_B$ output

    The (B-Y) component of the chrominance signal ($D_B$ component at SECAM) is present at this pin.
    The signal is applied to the input of the (B-Y) demodulator (pin 9) and to the tank circuit for the SECAM reference signal.
    The emitter follower output should be loaded with a 2, 7 kΩ resistor to obtain an output impedance of $<100\ \Omega$.

16. Square wave input

    A square wave with an amplitude of 3 V drives the PAL switch or the SECAM permutator.
    The square wave is available at pin 12 of the TCA640.

# CONTRAST, SATURATION AND BRIGHTNESS CONTROL CIRCUIT FOR COLOUR DIFFERENCE AND LUMINANCE SIGNALS

The TCA660B is an integrated circuit performing the control functions of contrast, saturation and brightness in colour television receivers.
Contrast is controlled by three tracking electronic potentiometers; one for the luminance signal and the other two for the (R-Y) and (B-Y) colour difference signals.
In addition two tracking electronic potentiometers provide the saturation control of the colour difference signals.
Brightness is controlled by varying the black level of the luminance signal at the output.
An inverting amplifier is also included for matrixing the (G-Y) signal from the (R-Y) and (B-Y) colour difference signals.

**QUICK REFERENCE DATA**

| | | | | | |
|---|---|---|---|---|---|
| Supply voltage | $V_{13-4}$ | nom. | 12 | V | |
| Supply current | $I_{13}$ | nom. | 35 | mA | |
| Luminance input current (black-to-white positive video signal) | $I_{16}$ | typ. | 0,7 | mA | |
| Luminance output voltage (black-to-white positive video signal; peak-to-peak value) | $V_{1-4(p-p)}$ | typ. | 3 | V | 1) |
| Black level (nominal value) | $V_{1-4}$ | typ. | 4,2 | V | |
| Brightness control (around nominal black level) | $V_{1-4}$ | | +1 to −2 | V | |
| Gain of the (R-Y) and (B-Y) amplifier | | typ. | 5 | dB | 1) 2) |
| Gain of the (G-Y) amplifier | | typ. | 1 | | |
| Contrast control range | | | +3 to −20 | dB | 3) |
| Saturation control range | | | +6 to −20 | dB | 3) |

---

1) At nominal contrast setting (max. contrast −3 dB)

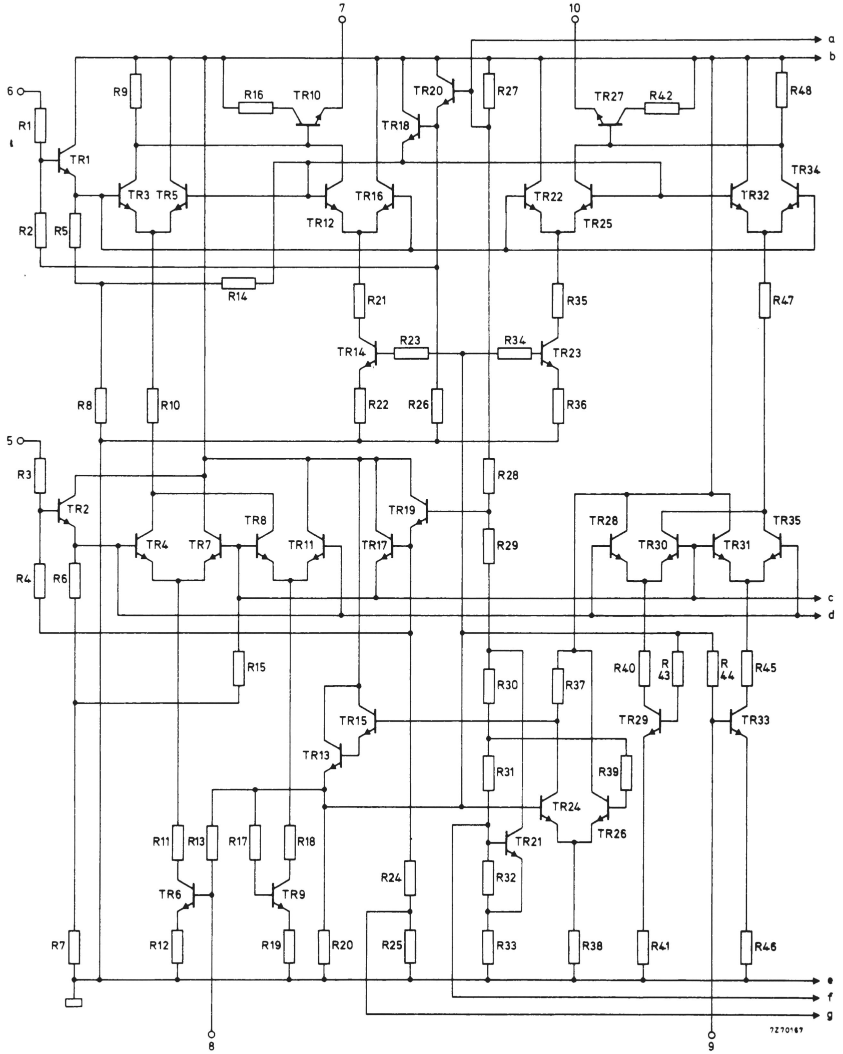
2) At nominal saturation control setting (max. saturation −6 dB)

3) Nominal contrast and nominal saturation are specified as 0 dB.

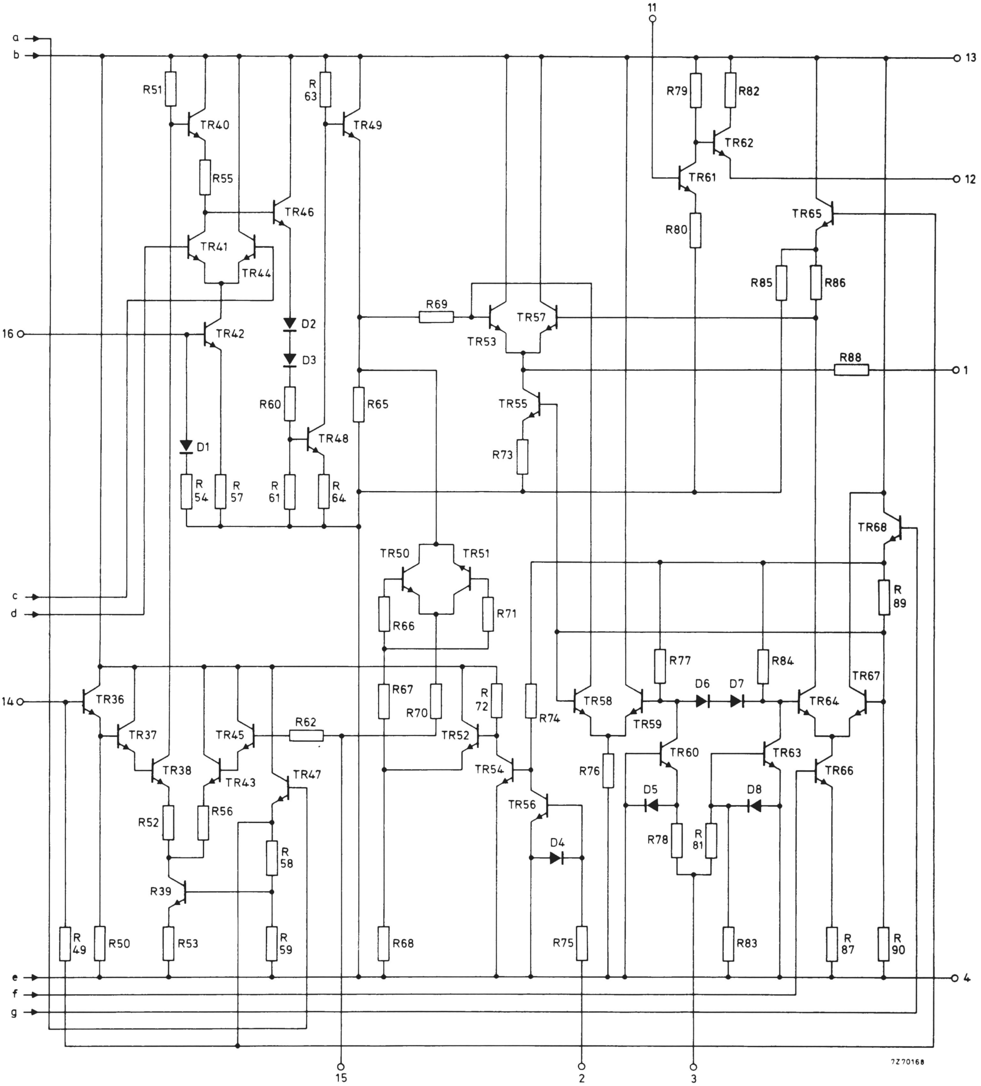
**PACKAGE OUTLINE**

16-lead DIL; plastic (SOT-38).

## CIRCUIT DIAGRAM


7
10
a
b
6
R1
R9
R16
TR10
TR20
R27
TR27
R42
R48
TR18
TR1
TR3
TR5
TR16
TR22
TR34
TR32
R2
R5
TR12
TR25
R14
R21
R35
R47
R23
R34
TR14
TR23
R8
R10
R22
R26
R36
5
R3
R28
TR2
TR19
TR28
TR35
TR8
TR4
TR7
TR11
TR17
R29
TR30
TR31
R4
R6
c
d
R15
R40
R
43
R
44
R45
R30
R37
TR15
TR29
TR33
TR13
R31
R39
TR24
TR26
R11
R13
R17
R18
TR21
R24
R32
TR6
TR9
R7
R12
R19
R20
R25
R33
R38
R41
R46
e
f
g
8
9
7Z70167

## CIRCUIT DIAGRAM (continued)


11
a
b
13
R51
TR40
R
63
TR49
R79
R82
TR62
TR61
12
R55
TR46
TR65
TR41
TR44
R80
R85
R86
R69
TR57
TR53
16
TR42
D2
D3
R88
1
R60
R65
TR55
TR48
D1
R73
R
54
R
57
R
61
R
64
TR68
TR50
TR51
c
d
R66
R71
R
89
R77
R84
TR67
14
TR36
R67
R
72
R74
TR58
TR59
D6
D7
TR64
TR37
TR45
R62
R70
TR52
TR60
TR63
TR38
TR43
TR47
TR54
R76
TR66
D5
D8
TR56
R52
R56
R
58
D4
R78
R
81
R39
R
49
R50
R53
R
59
R68
R75
R83
R
87
R
90
e
f
g
4
15
2
3
7Z70168

**RATINGS** Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | |
|---|---|---|---|
| Voltage | | | |
| Supply voltage | $V_{13-4}$ | max. | 13,2 V |
| Power dissipation | | | |
| Total power dissipation | $P_{tot}$ | max. | 600 mW |
| Temperatures | | | |
| Storage temperature | $T_{stg}$ | | −25 to +125 °C |
| Operating ambient temperature | $T_{amb}$ | | −25 to +65 °C [1] |

**CHARACTERISTICS** measured in the circuit on page 7

| | | | |
|---|---|---|---|
| Supply voltage | $V_{13-4}$ | typ. | 12 V<br>10,2 to 13,2 V |

Required input signals at $V_{13-4}$ = 12 V and $T_{amb}$ = 25 °C

| | | | |
|---|---|---|---|
| Luminance input current | | | |
| black-to-white positive video signal | $I_{16}$ | typ. | 0,7 mA<br>0 to 2,5 mA |
| Input impedance at $I_{16}$ = 1 mA | $\|Z_{16-4}\|$ | | 60 to 90 Ω |
| Input impedance variation for an input current variation $\Delta I_{16}$ = ± 0,5 mA | $\|\Delta Z_{16-4}\|$ | | ∓25 Ω |
| Colour difference input voltage | | | |
| (R-Y); peak-to-peak value | $V_{9-4(p-p)}$ | < | 0,7 V |
| (B-Y); peak-to-peak value | $V_{8-4(p-p)}$ | < | 0,9 V |
| Input voltage variation before clipping of the output voltage occurs | $\Delta V_{8-4}$<br>$\Delta V_{9-4}$ | typ. | 0,8 V |
| Input impedance | $\|Z_{8-4}\|$<br>$\|Z_{9-4}\|$ | | 3,5 to 6,5 kΩ |
| Blanking pulse (peak value) | $V_{3-4M}$ | | −1,5 to −10 V |
| Black level reinsertion pulse (peak value) | $V_{3-4M}$ | | +2 to +12 V [2] |
| Black level clamp pulse (peak value) | $V_{2-4M}$ | | +1 to +12 V |
| Luminance output voltage at nominal contrast | | | |
| black-to-white positive video signal; peak-to-peak value | $V_{1-4(p-p)}$ | | 2 to 4 V [3] |

---

[1] When a stabilized power supply of ≤ 12 V is applied, $T_{amb}$ is max. 75 °C.

[2] During scan $V_{3-4}$ must be kept lower than 0,7 V (positive and negative) to avoid blanking of the luminance signal.

[3] Nominal contrast is specified as maximum contrast −3 dB.

## CHARACTERISTICS (continued)

| | | | | | |
|---|---|---|---|---|---|
| Black level at nominal brightness setting | $V_{1-4}$ | typ. | 4, 2 | V | 1) |
| Black level variation with brightness setting | $\Delta V_{1-4}$ | | +1 to −2 | V | |
| Contrast control voltage range | $V_{5-4}$ | See graph on page 6 | | | |
| Black level variation with contrast control | $\Delta V_{1-4}$ | < | 40 | mV | 2) |
| Black level variation with video contents | $\Delta V_{1-4}$ | < | 20 | mV | 3) |
| Variation between video black level and reinserted black level at $\Delta T_{amb} = 25\ ^{o}C$ and $\Delta V_{13-4} \pm 10\%$ | $V_{1-4}$ | < | ±20 | mV | |
| Blanking level with respect to nominal brightness | $V_{1-4}$ | | −0, 8 to −1, 2 | V | |
| Bandwidth (−3 dB) of luminance signal | B | > | 6 | MHz | |
| Colour difference output signal for nominal contrast and saturation 4) 5) | | | | | |
| (R-Y); peak-to-peak value | $V_{10-4(p-p)}$ | typ. | 1, 25 | V | 6) |
| (B-Y); peak-to-peak value | $V_{7-4(p-p)}$ | typ. | 1, 6 | V | 6) |
| D.C. output level | $V_{7-4}$<br>$V_{10-4}$ | typ. | 6, 1 | V | |
| Output level variation with contrast and saturation control | $\Delta V_{7-4}$<br>$\Delta V_{10-4}$ | < | 500 | mV | |
| Permissible d.c. load impedance | $\lvert Z_{7-4} \rvert$<br>$\lvert Z_{10-4} \rvert$ | > | 4 | kΩ | |
| Saturation control voltage range | $V_{6-4}$ | See graph on page 6 | | | |
| Saturation control at $V_{6-4} < 0,5$ V | | < | −50 | dB | |
| Bandwidth (−3 dB) of colour difference signal | B | > | 2, 5 | MHz | |

---

1) Nominal brightness setting $V_{14-4} = 5,7$ V.
2) Only valid if the input current does not exceed 0, 5 mA during black.
3) For a.c. coupling only.
4) Nominal contrast is specified as maximum contrast −3 dB.
5) Nominal saturation is specified as maximum saturation −6 dB.
6) This value is obtained at the specified maximum input voltage.

## CHARACTERISTICS (continued)

(G-Y) amplifier

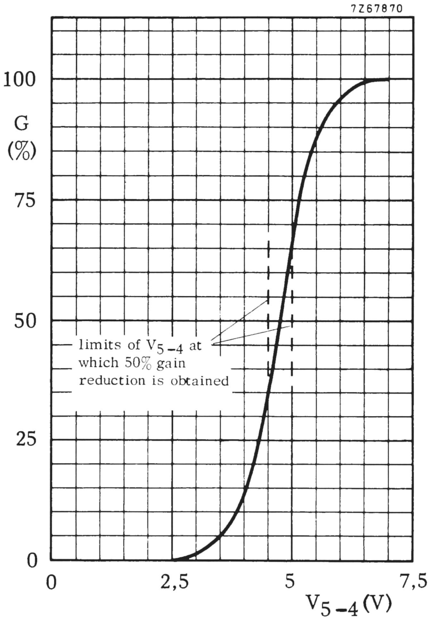
| | | | | |
|---|---|---|---|---|
| input voltage (peak-to-peak value) | $V_{11-4(p-p)}$ | < | 1 | V |
| output voltage (peak-to-peak value) | $V_{12-2(p-p)}$ | < | 1 | V |
| voltage gain | $G_{11-12}$ | | -1 to +0,5 | dB |

Tracking during contrast and saturation control

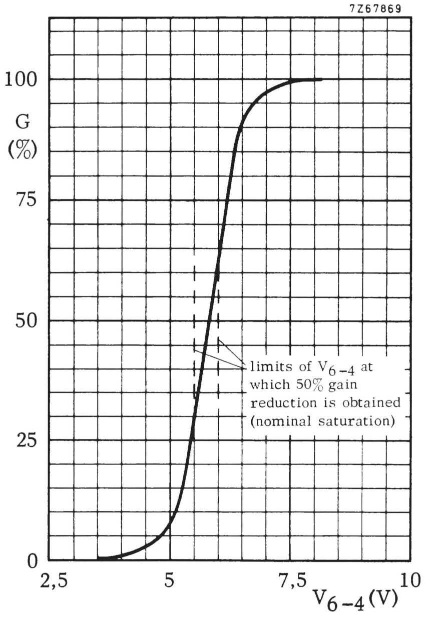
| | | | |
|---|---|---|---|
| at a contrast decrease of 20 dB | | | |
| change of the ratio $\frac{(R-Y)}{(B-Y)}$ | < | ±1 | dB |
| change of the ratio $\frac{Y}{(B-Y)}$ | | 0 to 4 | dB |
| at a saturation decrease of 20 dB | | | |
| change of the ratio $\frac{(R-Y)}{(B-Y)}$ | < | ±1 | dB |

Cross coupling

| | | | |
|---|---|---|---|
| luminance signal to colour difference signal | < | -40 | dB |
| (B-Y) signal to (R-Y) signal | < | -30 | dB |
| colour difference signal to luminance signal | < | -40 | dB |

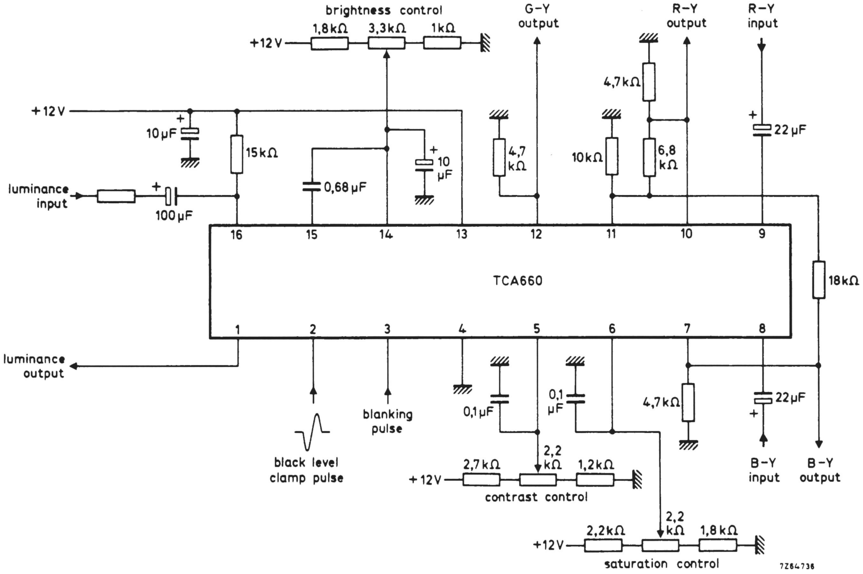


Contrast control of luminance amplifier



Saturation control of chrominance amplifier

## APPLICATION INFORMATION


brightness control
1,8 kΩ
3,3 kΩ
1 kΩ
+12 V
G–Y output
R–Y output
R–Y input
+12 V
10 µF
+
15 kΩ
4,7 kΩ
+
22 µF
+
10 µF
0,68 µF
4,7 kΩ
10 kΩ
6,8 kΩ
luminance input
+
100 µF
16
15
14
13
12
11
10
9
TCA660
18 kΩ
1
2
3
4
5
6
7
8
luminance output
0,1 µF
0,1 µF
4,7 kΩ
22 µF
+
blanking pulse
black level clamp pulse
2,2 kΩ
2,7 kΩ
1,2 kΩ
+12 V
contrast control
B–Y input
B–Y output
2,2 kΩ
2,2 kΩ
1,8 kΩ
+12 V
saturation control
7Z64736

### Pinning

1. Luminance signal output
2. Black level clamp pulse input
3. Blanking pulse input
4. Earth (negative supply)
5. Contrast control input
6. Saturation control input
7. (B-Y) signal output
8. (B-Y) signal input
9. (R-Y) signal input
10. (R-Y) signal output
11. (G-Y) signal input
12. (G-Y) signal output
13. Supply voltage (12 V)
14. Brightness control input
15. Black level clamp capacitor
16. Luminance signal input

## APPLICATION INFORMATION (continued)

**The function is quoted against the corresponding pin number**

1. Luminance signal output

   A positive video signal of 3 V peak-to-peak is available at nominal contrast setting. The black level is clamped internally on the back porch.
   By means of the brightness control the black level can be varied between 2,2 V and 5,2 V. The blanking level of the output signal will assume a value of 3,0 to 3,4 V.

2. Black level clamp pulse input

   A positive pulse with a peak value between +1 V and +12 V will clamp the black level of the video signal to a nominal level of 4,2 V. The pulse may only be present during the back porch and should have a duration of about 3 μs.

3. Blanking pulse input

   Two modes operation can be selected by the choice of the amplitude of the pulse applied:

   - blanking

   - black level reinsertion

   Blanking of the luminance output signal is obtained when the peak value of the pulse ranges from −1,5 to −10 V. An artificial black level of nominally + 4,2 V is inserted in the luminance output signal during the blanking period when the peak value of the pulse ranges from +2 to + 12 V.
   During scan the amplitude at pin 3 should remain between +0,7 V and −0,7 V to avoid blanking.

4. Negative supply (earth)

5. Contrast control input

   The contrast curve is given on page 4. To avoid damaging of the circuit by flash-over pulses, picked-up by the leads, it is recommended that a capacitor of 100 nF be connected between this pin and earth.

6. Saturation control input

   The control curve is given on page 4. To avoid damaging of the circuit by flash-over pulses, picked-up by the leads, it is recommended that a capacitor of 100 nF be connected between this pin and earth.

7. (B-Y) signal output

   The amplitude of this signal is controlled by the contrast setting and the saturation setting simultaneously. At nominal contrast and nominal saturation setting an amplitude of 1,6 V peak-to-peak is obtained at an input amplitude of 0,9 V peak-to-peak. The average level is typically 6,1 V.

8. (B-Y) signal input

   The signal has to be a.c. coupled to the input.
   To cope with the variation of picture contents an input voltage margin of ±0,8 V is provided, whereas the input signal has a typical value of ± 0,45 V for a saturated colour bar signal.

**APPLICATION INFORMATION** (continued)

9. (R-Y) signal input

   The signal has to be a.c. coupled to the input.
   To cope with the variation of picture contents an input voltage margin of ± 0,8 V is provided, whereas the input signal has a typical value of ± 0,35 V for a saturated colour bar input.

10. (R-Y) signal output

    The amplitude of this signal is controlled by the contrast setting and saturation setting simultaneously. At nominal contrast and nominal saturation setting an amplitude of 1,25 V peak-to-peak is obtained at an input amplitude of 0,7 V peak to peak.
    The average level is typically 6,1 V.

11. (G-Y) signal input

    The (G-Y) signal is obtained by matrixing a part of the (R-Y) and (B-Y) signals in a resistor network. The input may range from 1 to 6,5 V.
    An average level of typical 5,9 V is required to produce an average output level of 6,1 V.
    The gain of the inverter stage is typically 1.

12. (G-Y) signal output

    An inverted signal with an amplitude of maximum 1 V peak-to-peak is available at this pin.

13. Supply voltage (12 V)

    Correct operation occurs within the range 10,2 to 13,2 V.
    The power dissipation must not exceed 600 mW at 65 °C ambient temperature.

14. Brightness control input

    The black level of the luminance output signal tracks the potential applied to this pin.
    A typical value for setting the brightness control is 5,7 V, for which a black level of 4,2 V is obtained.
    It is recommended that a capacitor of at least 10 μF be connected between this pin and earth.

15. Black level clamp capacitor

    The level of the back porch of the luminance output signal is stored in an external capacitor of about 0,68 μF; the latter to be connected between pins 14 and 15.

16. Luminance signal input

    A positive luminance signal of 0,7 mA peak-to-peak between black and white level drives the luminance amplifier.
    A black level of about 0,3 mA is recommended. For a.c. coupling a bias resistor to the supply line is required to bias the amplifier properly.
    The resistance depends on the signal amplitude e.g.: 15 kΩ is recommended for a input signal of 0,7 mA peak-to-peak.

# DOUBLE BALANCED MODULATOR/DEMODULATOR

The TDA0820T is a monolithic integrated circuit for use at frequencies up to 650 MHz.
Typical applications are:

- modulator
- mixer
- switch/chopper
- a.m. synchronous demodulator
- f.m. quadrature demodulator
- phase comparator
- differential amplifier

The circuit is arranged to offer very flexible circuit design possibilities. The excellent matching and temperature tracking of the transistors in the circuit allow the use of circuit techniques which are not available when using discrete devices.

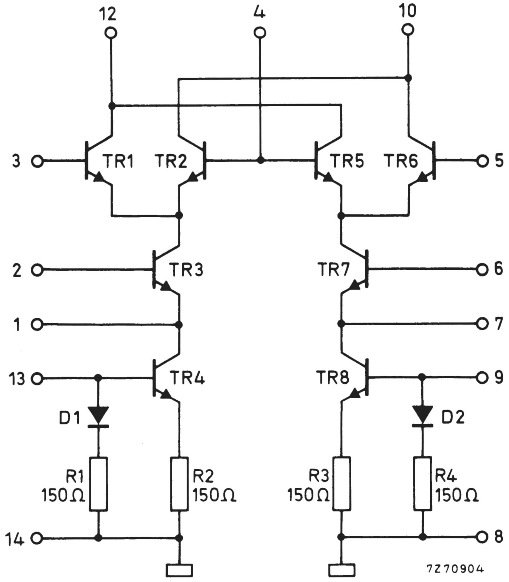

12
4
10
3
TR1
TR2
TR5
TR6
5
2
TR3
TR7
6
1
7
13
TR4
TR8
9
D1
D2
R1 150 Ω
R2 150 Ω
R3 150 Ω
R4 150 Ω
14
8
7Z70904

Fig. 1 Circuit diagram.

**PACKAGE OUTLINE**

14-lead mini-pack; plastic (SO-14; SOT-108A).

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | |
|---|---|---|---|
| Supply voltage range | $V_{10\text{-}8}; V_{10\text{-}14}; V_{12\text{-}8}; V_{12\text{-}14}$ | | 0 to 13,2 V |
| **Voltages** (each transistor) | | | |
| Collector-substrate voltage (open base) and emitter) | $V_{CSO}$ | max. | 15 V |
| Collector-base voltage (open emitter) | $V_{CBO}$ | max. | 12 V |
| Collector-emitter voltage (open base) | $V_{CEO}$ | max. | 10 V |
| Emitter-base voltage (open collector) | $V_{EBO}$ | max. | 5 V |
| **Currents** (each transistor) | | | |
| Emitter current | $I_E$ | max. | 10 mA |
| Base current | $I_B$ | max. | 10 mA |
| Total power dissipation when mounted on a printed-circuit board | $P_{tot}$ | max. | 250 mW |
| Storage temperature | $T_{stg}$ | | −55 to + 125 °C |
| Operating ambient temperature | $T_{amb}$ | | 0 to + 70 °C |

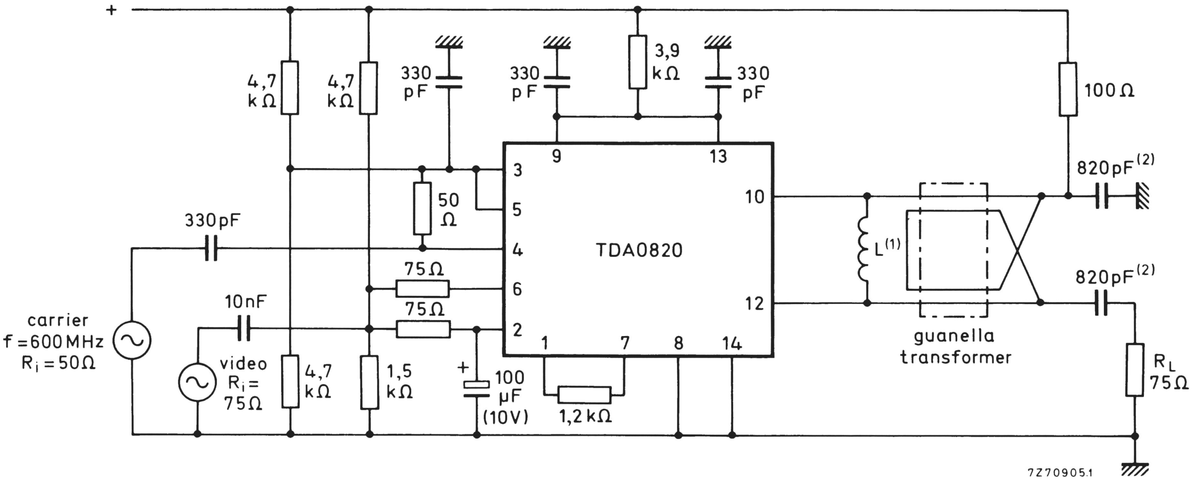
## THERMAL RESISTANCE

| | | | |
|---|---|---|---|
| From junction to ambient | $R_{th\ j\text{-}a}$ | = | 220 K/W |

## CHARACTERISTICS

$V_{10\text{-}8} = V_{10\text{-}14} = V_{12\text{-}8} = V_{12\text{-}14} = 12$ V; $T_{amb} = 25$ °C; measured in Fig. 2

| | | | |
|---|---|---|---|
| Supply current | $I_{10} + I_{12}$ | typ.<br>< | 2,5 mA<br>3 mA |
| Input signals | | | |
| carrier signal (r.m.s. value) | $V_{3\text{-}4(rms)}; V_{5\text{-}4(rms)}$ | < | 100 mV |
| video signal; negative modulated (peak-to-peak value) | $V_{6\text{-}2(p\text{-}p)}$ | < | 1,4 V |
| Output signal at top sync over 75 Ω (peak-to-peak value) | $V_{10\text{-}12(p\text{-}p)}$ | > | 22 mV |
| Carrier suppression in balanced condition | $V_{10\text{-}12}$ | > | 38 dB |
| Differential phase | | < | 6° |
| Differential gain | | < | 15 % |
| Distortion of video signal | | < | −38 dB |


+
4,7 kΩ
4,7 kΩ
330 pF
330 pF
3,9 kΩ
330 pF
100 Ω
820pF(2)
820pF(2)
9
13
3
5
4
6
2
1
7
8
14
10
12
TDA0820
50 Ω
330pF
75Ω
75Ω
10nF
carrier
f = 600 MHz
Ri = 50Ω
video
Ri = 75Ω
4,7 kΩ
1,5 kΩ
+
100 μF (10V)
1,2 kΩ
L(1)
guanella transformer
RL 75Ω
7Z70905.1

(1) L = air coil; 3 turns; $\phi$ 3 mm.
(2) U.H.F. decoupling capacitor 2212 669 98003.

Fig. 2 Test circuit.

# SIGNAL-SOURCES SWITCH

The TDA1028 is a quadruple operational amplifier connected as an impedance converter. Each amplifier has 2 switchable inputs which are protected by clamping diodes. The input currents are independent of the switch position and the outputs are short-circuit protected.

The device is intended as an electronic four-channel signal-sources switch in a.f. amplifiers.

## QUICK REFERENCE DATA

| | | | | |
|---|---|---|---|---|
| Supply voltage range (pin 9) | $V_P$ | | 6 to 23 | V |
| Operating ambient temperature | $T_{amb}$ | | −30 to + 80 | °C |
| Supply voltage (pin 9) | $V_P$ | typ. | 20 | V |
| Current consumption (pins 4, 5, 12, 13 unloaded) | $I_g$ | typ. | 2,9 | mA |
| Maximum input signal handling (r.m.s. value) | $V_{i(rms)}$ | typ. | 6 | V |
| Voltage gain | $G_v$ | typ. | 1 | |
| Total harmonic distortion | $d_{tot}$ | typ. | 0,01 | % |
| Crosstalk | $\alpha$ | typ. | 70 | dB |
| Signal-to-noise ratio | S/N | typ. | 120 | dB |

## PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).

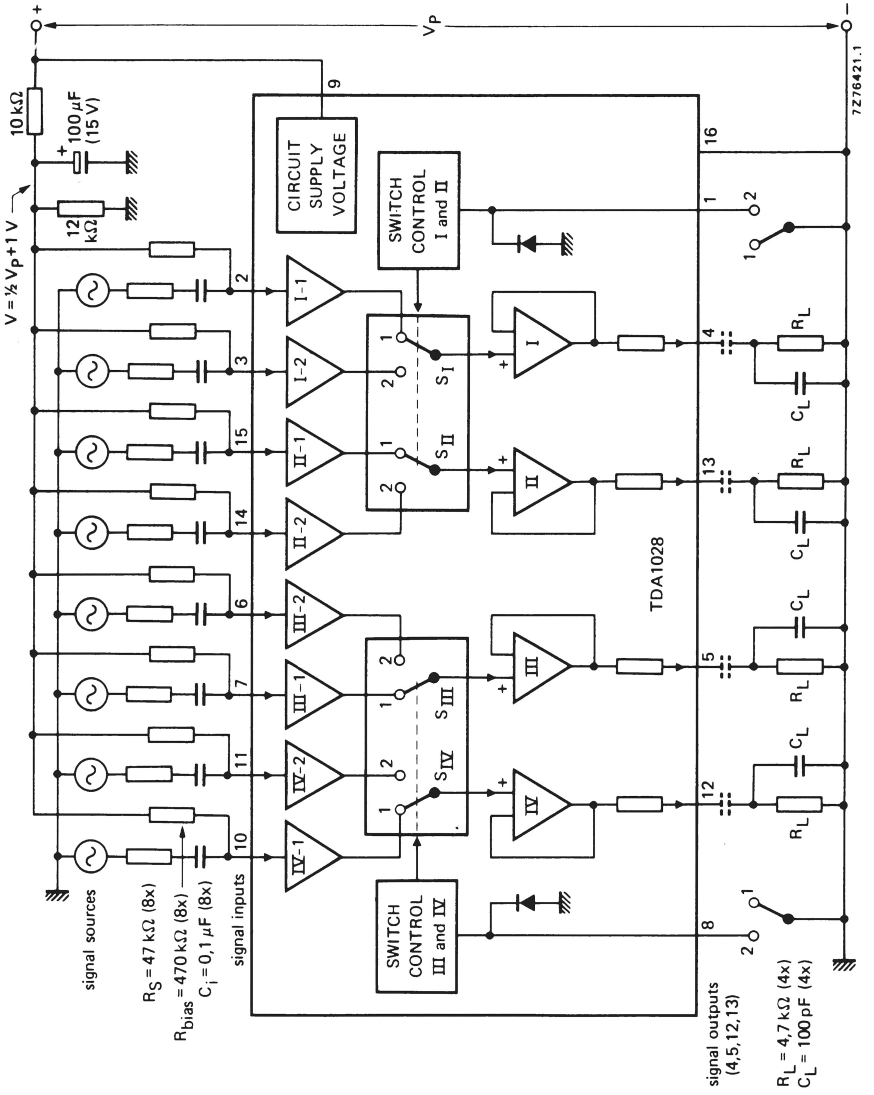

+
−
V_P
7Z76421.1
10 kΩ
100 µF
(15 V)
+
12 kΩ
V = ½ V_P + 1 V
9
CIRCUIT SUPPLY VOLTAGE
SWITCH CONTROL I and II
SWITCH CONTROL III and IV
16
1
2
1
2
8
I-1
I-2
II-1
II-2
III-2
III-1
IV-2
IV-1
S_I
S_II
S_III
S_IV
I
II
III
IV
+
4
13
5
12
R_L
C_L
TDA1028
signal sources
R_S = 47 kΩ (8x)
R_bias = 470 kΩ (8x)
C_i = 0,1 µF (8x)
signal inputs
signal outputs (4,5,12,13)
R_L = 4,7 kΩ (4x)
C_L = 100 pF (4x)

Fig. 1 Block diagram.

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | | |
|---|---|---|---|---|
| Supply voltage (pin 9) | $V_P$ | max. | 23 | V |
| Input voltages (pins 2, 3, 6, 7, 10, 11, 14, 15) | $V_I$ | max. | $V_P$ | |
| | $-V_I$ | max. | 0,5 | V |
| Switch control voltage (pin 1 and 8) | $V_S$ | | 0 to 23 | V |
| Input current | $\pm I_I$ | max. | 20 | mA |
| Switch control current | $-I_S$ | max. | 50 | mA |
| Total power dissipation | $P_{tot}$ | max. | 800 | mW |
| Storage temperature | $T_{stg}$ | | −55 to + 150 | °C |
| Operating ambient temperature | $T_{amb}$ | | −30 to + 80 | °C |

## CHARACTERISTICS

$V_P = 20$ V; $T_{amb} = 25$ °C; unless otherwise specified

| | | | | |
|---|---|---|---|---|
| Current consumption without load; $I_{4;\,5;\,12;\,13} = 0$ | $I_9$ | typ. | 2,9 | mA |
| | | | 1,6 to 4,2 | mA |
| Supply voltage range | $V_P$ | | 6 to 23 | V |

**Signal inputs**

| | | | | |
|---|---|---|---|---|
| Input offset voltage of switched-on inputs ($R_S < 1$ kΩ) | $V_{io}$ | typ. | 2 | mV |
| | | < | 10 | mV |
| Input offset current of switched-on inputs | $I_{io}$ | typ. | 20 | nA |
| | | < | 200 | nA |
| Input offset current of a switched-on input with respect to a non-switched-on input | $I_{io}$ | typ. | 20 | nA |
| | | < | 200 | nA |
| Input bias current independent of switch position | $I_i$ | typ. | 250 | nA |
| | | < | 950 | nA |
| Capacitance between adjacent inputs | C | typ. | 0,5 | pF |
| D.C. input voltage range | $V_I$ | | 3 to 19 | V |
| Supply voltage rejection ratio; $R_S < 10$ kΩ | SVRR | typ. | 100 | μV/V |
| Equivalent input noise voltage $R_S \leqslant 1$ kΩ; f = 20 Hz to 20 kHz (r.m.s. value) | $V_{n(rms)}$ | typ. | 3,5 | μV |
| Equivalent input noise current f = 20 Hz to 20 kHz (r.m.s. value) | $I_{n(rms)}$ | typ. | 0,05 | nA |
| Crosstalk between a switched-on input and a non-switched-on input; measured at the output at $R_S < 1$ kΩ; f = 1 kHz | $\alpha$ | typ. | 100 | dB |

**Signal amplifier**

| | | | | |
|---|---|---|---|---|
| Voltage gain of a switched-on input at $I_{4;\,5;\,12;\,13} = 0$; $R_L = \infty$ | $G_v$ | typ. | 1 | |
| Current gain of a switched-on amplifier | $G_i$ | typ. | $10^5$ | |

**CHARACTERISTICS** (continued)

**Signal outputs**

| | | | |
|---|---|---|---|
| Output resistance | $R_o$ | typ. | 400 Ω |
| Output current capability (pins 4, 5, 12 and 13) | $\pm I_o$ | > | 5 mA |
| Frequency limit of the output voltage<br>at $V_{i(p-p)} = 1$ V; $R_S < 1$ kΩ;<br>$R_L = 10$ MΩ; $C_L = 10$ pF | f | typ. | 1,3 MHz |
| Slew rate (unity gain) $\Delta V_{4;\,5;\,12;\,13\text{-}16}/\Delta t$<br>at $R_L = 10$ MΩ; $C_L = 10$ pF | S | typ. | 2 V/μs |

**Switch control**

| switched-on inputs | interconnected pins | control voltages | |
|---|---|---|---|
| | | $V_{1\text{-}16}$ | $V_{8\text{-}16}$ |
| I-1, II-1 | 2-4, 15-13 | H | – |
| I-2, II-2 | 3-4, 14-13 | L | – |
| III-1, IV-1 | 7-5, 10-12 | – | H |
| III-2, IV-2 | 6-5, 11-12 | – | L |

**Control inputs** (pins 1 and 8)

| | | | |
|---|---|---|---|
| Required voltage | | | |
| HIGH | $V_{SH}$ | > | 3,3 V * |
| LOW | $V_{SL}$ | < | 2,1 V |
| Input current | | | |
| HIGH (leakage current) | $I_{SH}$ | < | 1 μA |
| LOW (control current) | $-I_{SL}$ | < | 200 μA |

---

* Or control inputs open; $R_{1\text{-}16}$, $R_{8\text{-}16} > 33$ MΩ.

## APPLICATION INFORMATION

$V_P$ = 20 V; $T_{amb}$ = 25 °C; measured in Fig. 1; $R_S$ = 47 kΩ; $C_i$ = 0,1 μF; $R_{bias}$ = 470 kΩ; $R_L$ = 4,7 kΩ; $C_L$ = 100 pF (unless otherwise specified)

| | | | | |
|---|---|---|---|---|
| Voltage gain | $G_v$ | typ. | −1,5 | dB |
| D.C. output voltage variation when switching the inputs (pins 4, 5, 12 and 13) | $\Delta V_o$ | typ.<br>$<$ | 10<br>100 | mV<br>mV |
| Total harmonic distortion | | | | |
| over most of signal range (see Fig. 4) | $d_{tot}$ | typ. | 0,01 | % |
| at $V_i$ = 5 V; f = 1 kHz | $d_{tot}$ | typ. | 0,02 | % |
| at $V_i$ = 5 V; f = 20 Hz to 20 kHz | $d_{tot}$ | typ. | 0,03 | % |
| Output signal handling $d_{tot}$ = 0,1%; f = 1 kHz (r.m.s. value) | $V_{o(rms)}$ | $>$<br>typ. | 5,0<br>5,3 | V<br>V |
| Noise output voltage (unweighted) f = 20 Hz to 20 kHz (r.m.s. value) | $V_{n(rms)}$ | typ. | 5 | μV |
| Noise output voltage (weighted) f = 20 Hz to 20 kHz (in accordance with DIN 45405) | $V_n$ | typ. | 12 | μV |
| Amplitude response (pins 4, 5, 12 and 13) $V_i$ = 5 V; f = 20 Hz to 20 kHz | $\Delta V_o$ | typ. | 0,1 | dB * |
| Crosstalk between a switched-on input and a non-switched-on input; measured at the output at f = 1 kHz | $\alpha$ | typ. | 75 | dB ** |
| Crosstalk between switched-on inputs and the outputs of the other channels; at f = 1 kHz | $\alpha$ | typ. | 90 | dB ** |

---

* The lower cut-off frequency depends on values of $R_{bias}$ and $C_i$.

** Depends on external circuitry and $R_S$. The value will be fixed mostly by capacitive crosstalk of the external components.

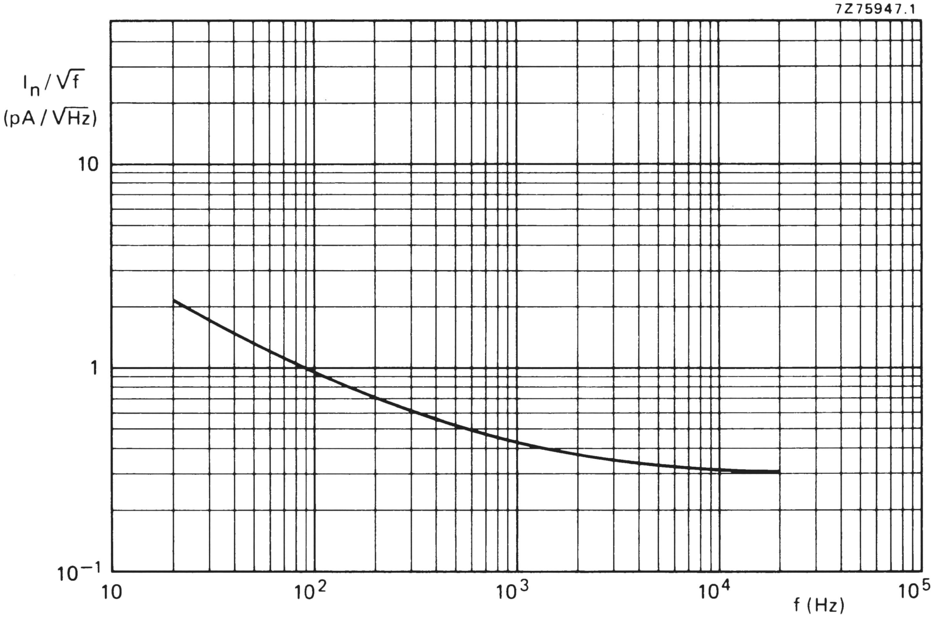


Fig. 2 Equivalent input noise current.

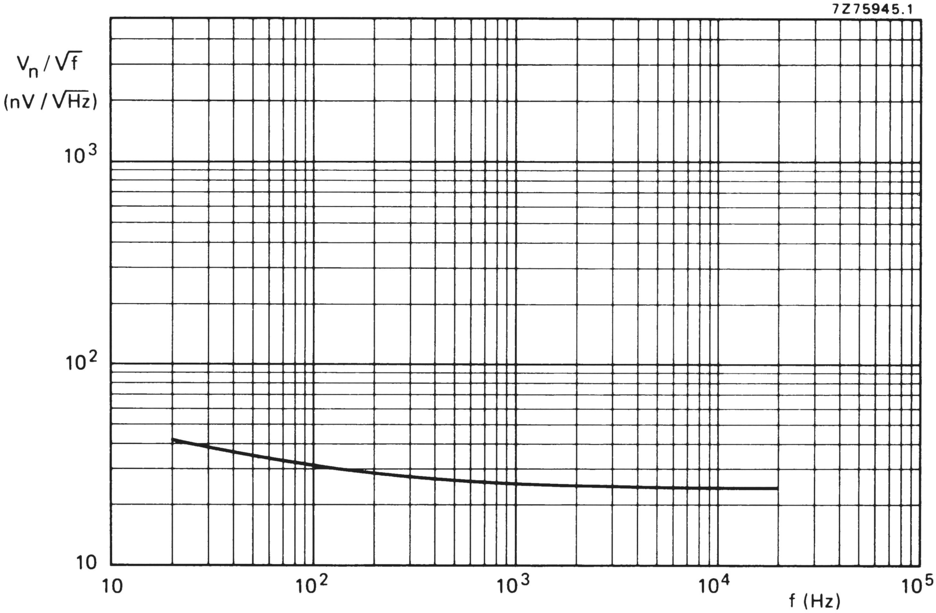


Fig. 3 Equivalent input noise voltage.

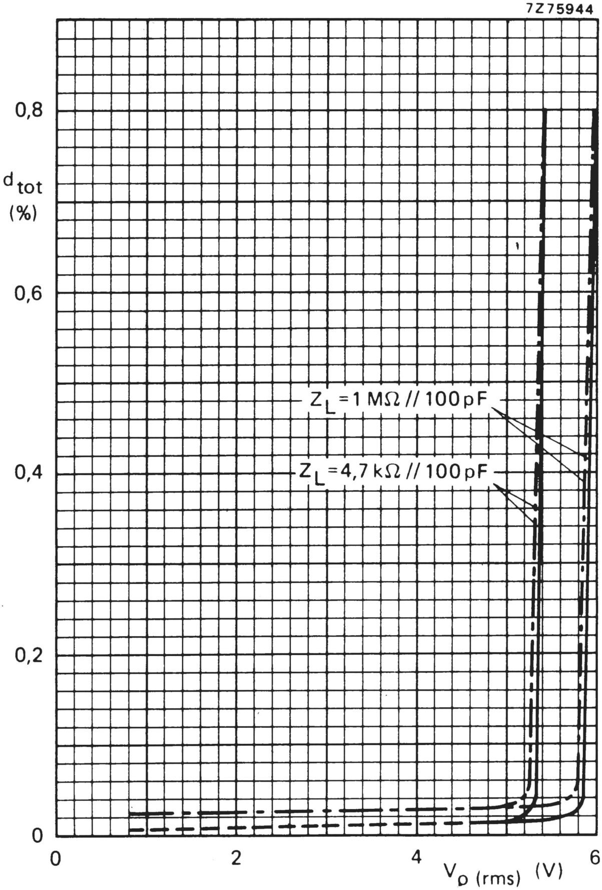


Fig. 4 Total harmonic distortion as a function of r.m.s. output voltage.
—— f = 1 kHz; — - — - f = 20 kHz.

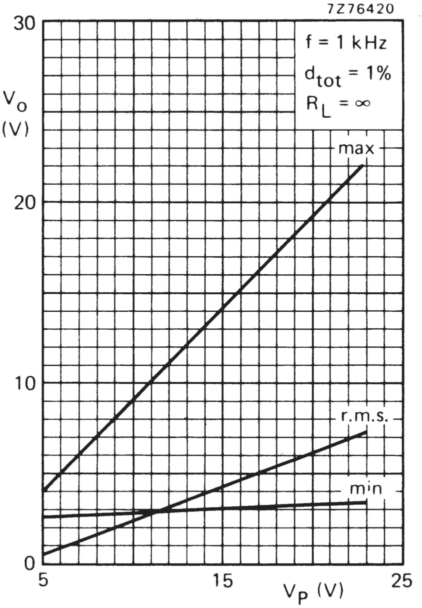


Fig. 5 Output voltage as a function of supply voltage.

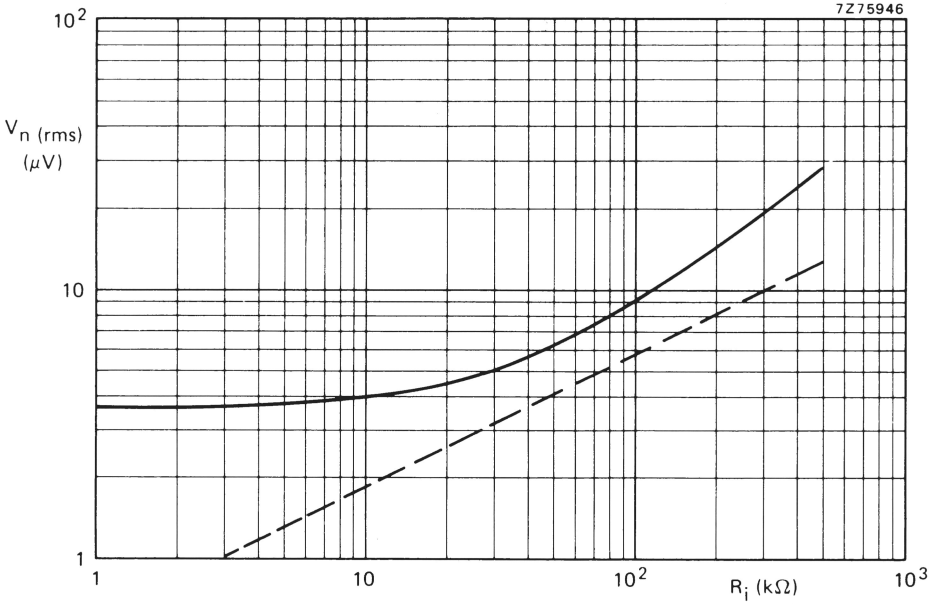


Fig. 6 Noise output voltage as a function of input resistance; $G_V = 1$; f = 20 Hz to 20 kHz.
—— $V_n$ (output); – – – $V_n$ ($R_S$).

## APPLICATION NOTES

### Input protection circuit and indication

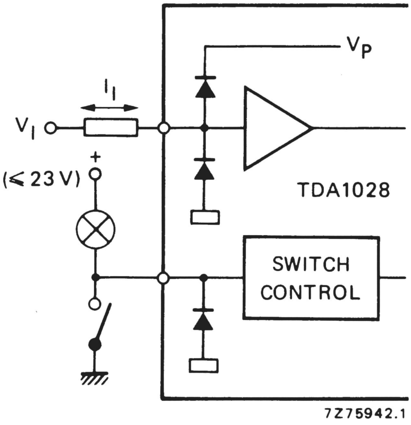


Fig. 7 Circuit diagram showing input protection and indication.

### Unused signal inputs

Any unused inputs must be connected to a d.c. (bias) voltage, which is within the d.c. input voltage range.

### Circuits with standby operation

The control inputs (pins 1 and 8) are high-ohmic at $V_{SH} \leqslant 20$ V ($I_{SH} \leqslant 1$ $\mu$A), as well as, when the supply voltage (pin 9) is switched off.

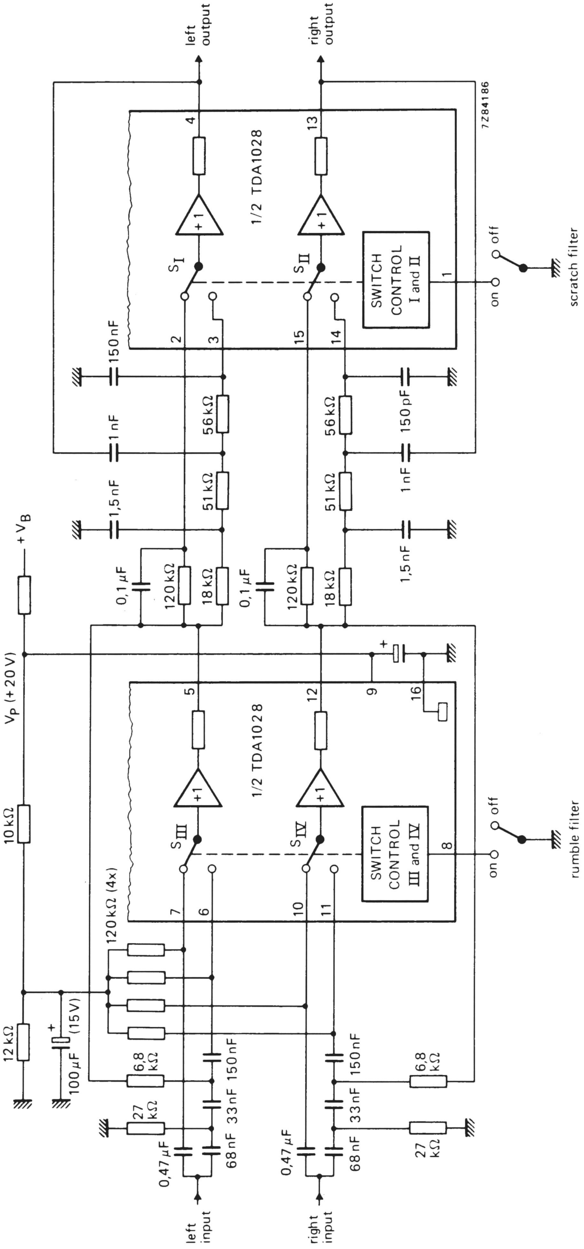

left output
right output
7Z84186
1/2 TDA1028
+1
SI
SII
SIII
SIV
SWITCH CONTROL I and II
SWITCH CONTROL III and IV
on
off
scratch filter
rumble filter
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
150 nF
150 pF
1 nF
56 kΩ
51 kΩ
1,5 nF
0,1 μF
120 kΩ
18 kΩ
+VB
VP (+20 V)
10 kΩ
12 kΩ
100 μF
(15V)
120 kΩ (4x)
6,8 kΩ
27 kΩ
0,47 μF
33 nF
68 nF
left input
right input

Fig. 8 Typical application diagram for a switchable scratch/rumble filter.

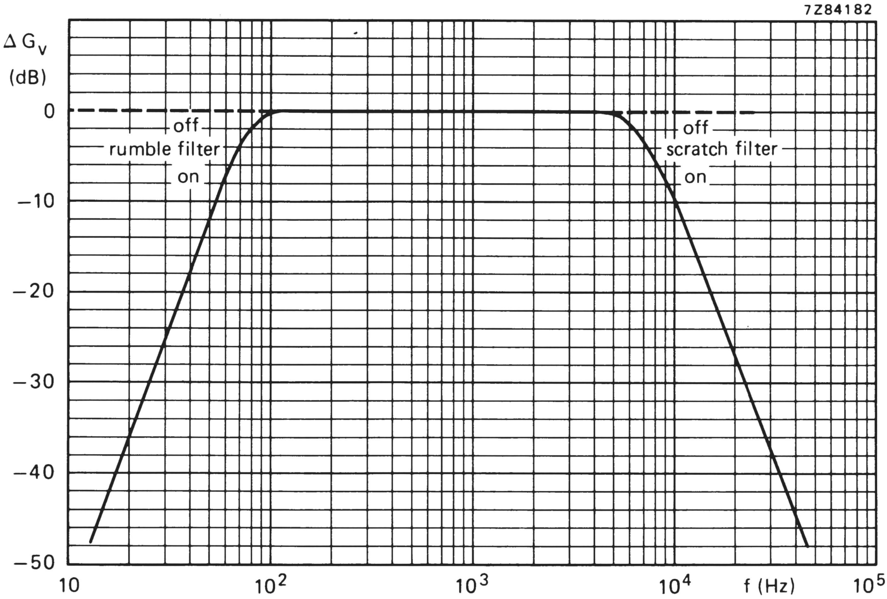


Fig. 9 Frequency response curves for scratch/rumble filters in Fig. 8.

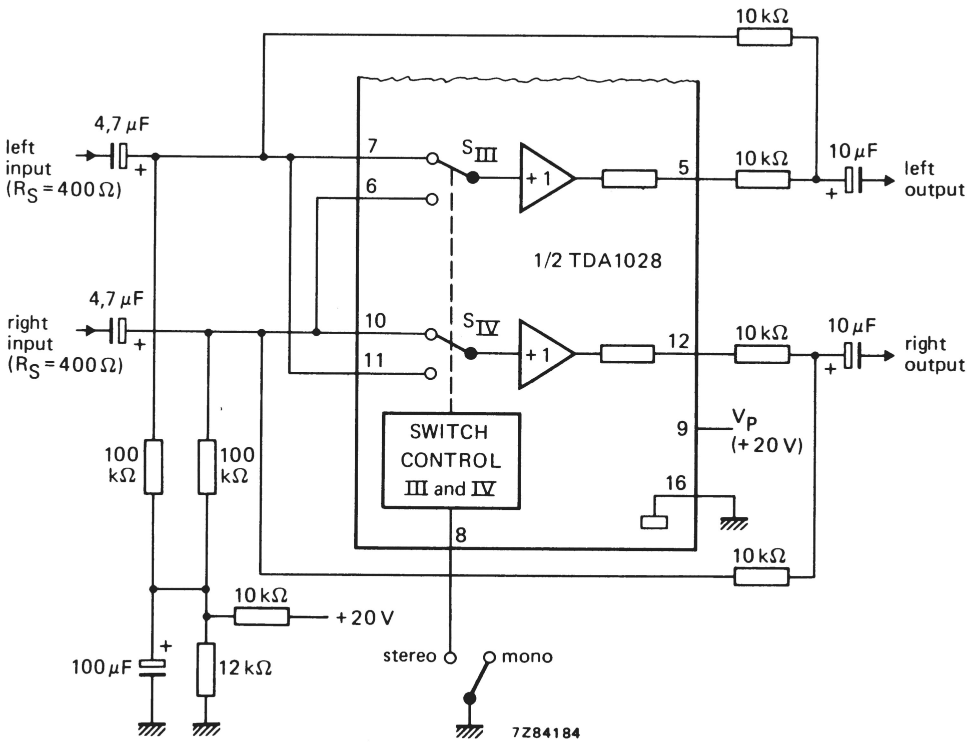

left
input
($R_S$ = 400 Ω)
4,7 μF
+
right
input
($R_S$ = 400 Ω)
4,7 μF
+
10 kΩ
7
6
10
11
$S_{III}$
$S_{IV}$
+ 1
+ 1
1/2 TDA1028
5
12
10 kΩ
10 kΩ
10 μF
+
left
output
10 μF
+
right
output
9
$V_P$
(+ 20 V)
16
SWITCH
CONTROL
III and IV
8
10 kΩ
100
kΩ
100
kΩ
10 kΩ
+ 20 V
100 μF
+
12 kΩ
stereo
mono
7Z84184

Fig. 10 Half of TDA1028 used as a mono/stereo switch.

# SIGNAL-SOURCES SWITCH

The TDA1029 is a dual operational amplifier (connected as an impedance converter) each amplifier having 4 mutually switchable inputs which are protected by clamping diodes. The input currents are independent of switch position and the outputs are short-circuit protected.

The device is intended as an electronic two-channel signal-source switch in a.f. amplifiers.

## QUICK REFERENCE DATA

| | | | | |
|---|---|---|---|---|
| Supply voltage range (pin 14) | $V_P$ | | 6 to 23 | V |
| Operating ambient temperature | $T_{amb}$ | | −30 to + 80 | °C |
| Supply voltage (pin 14) | $V_P$ | typ. | 20 | V |
| Current consumption | $I_{14}$ | typ. | 3,5 | mA |
| Maximum input signal handling (r.m.s. value) | $V_{i(rms)}$ | typ. | 6 | V |
| Voltage gain | $G_v$ | typ. | 1 | |
| Total harmonic distortion | $d_{tot}$ | typ. | 0,01 | % |
| Crosstalk | $\alpha$ | typ. | 70 | dB |
| Signal-to-noise ratio | S/N | typ. | 120 | dB |

## PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).

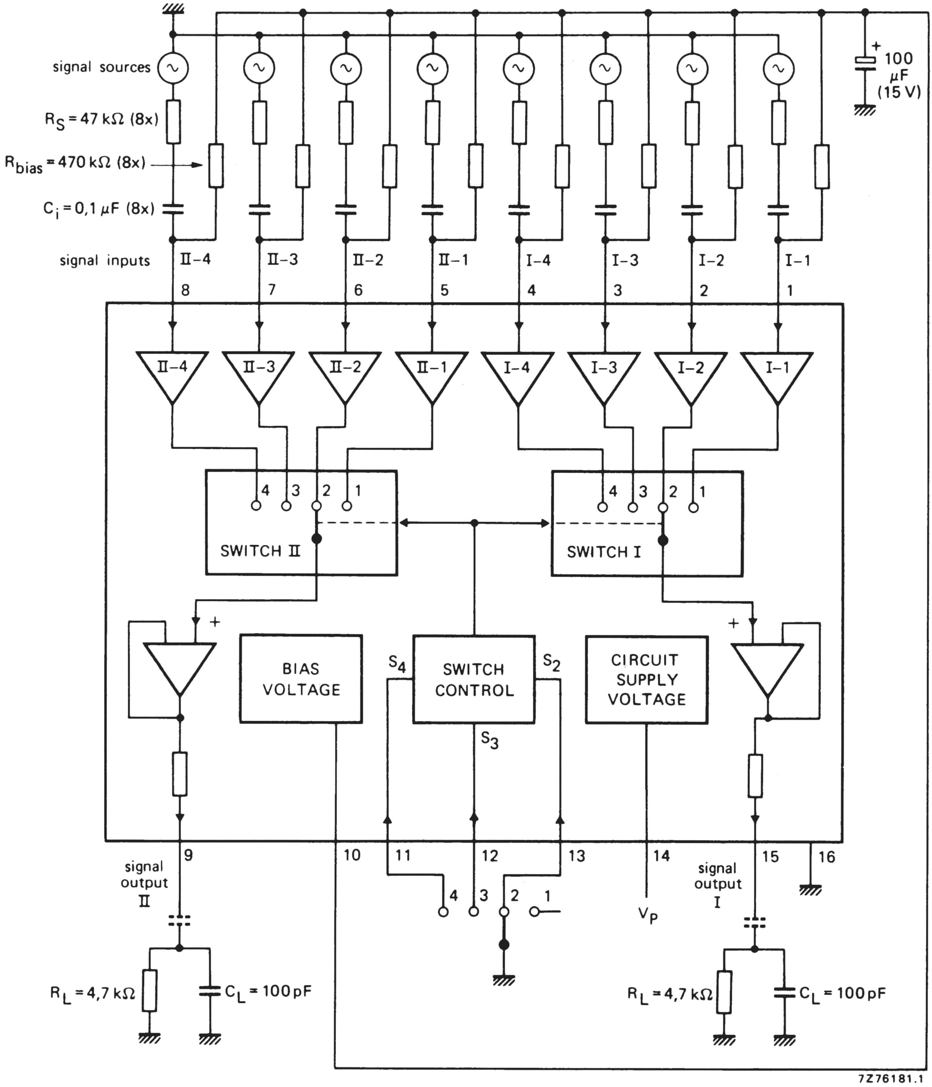

signal sources
$R_S$ = 47 kΩ (8x)
$R_{bias}$ = 470 kΩ (8x)
$C_i$ = 0,1 μF (8x)
signal inputs
II-4
II-3
II-2
II-1
I-4
I-3
I-2
I-1
8
7
6
5
4
3
2
1
100 μF (15 V)
SWITCH II
SWITCH I
BIAS VOLTAGE
SWITCH CONTROL
CIRCUIT SUPPLY VOLTAGE
$S_4$
$S_2$
$S_3$
9
10
11
12
13
14
15
16
signal output II
signal output I
$V_P$
$R_L$ = 4,7 kΩ
$C_L$ = 100 pF
7Z76181.1

Fig. 1 Block diagram.

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | | |
|---|---|---|---|---|
| Supply voltage (pin 14) | $V_P$ | max. | 23 | V |
| Input voltage (pins 1 to 8) | $V_I$ | max. | $V_P$ | |
| | $-V_I$ | max. | 0,5 | V |
| Switch control voltage (pins 11, 12 and 13) | $V_S$ | | 0 to 23 | V |
| Input current | $\pm I_I$ | max. | 20 | mA |
| Switch control current | $-I_S$ | max. | 50 | mA |
| Total power dissipation | $P_{tot}$ | max. | 800 | mW |
| Storage temperature | $T_{stg}$ | | −55 to + 150 | °C |
| Operating ambient temperature | $T_{amb}$ | | −30 to + 80 | °C |

## CHARACTERISTICS

$V_P = 20$ V; $T_{amb} = 25$ °C; unless otherwise specified

| | | | | |
|---|---|---|---|---|
| Current consumption without load; $I_9 = I_{15} = 0$ | $I_{14}$ | typ. | 3,5<br>2 to 5 | mA<br>mA |
| Supply voltage range (pin 14) | $V_P$ | | 6 to 23 | V |

**Signal inputs**

| | | | | |
|---|---|---|---|---|
| Input offset voltage of switched-on inputs<br>$R_S \leqslant 1$ kΩ | $V_{io}$ | typ.<br>< | 2<br>10 | mV<br>mV |
| Input offset current of switched-on inputs | $I_{io}$ | typ.<br>< | 20<br>200 | nA<br>nA |
| Input offset current of a switched-on input with respect to a non-switched-on input of a channel | $I_{io}$ | typ.<br>< | 20<br>200 | nA<br>nA |
| Input bias current independent of switch position | $I_i$ | typ.<br>< | 250<br>950 | nA<br>nA |
| Capacitance between adjacent inputs | C | typ. | 0,5 | pF |
| D.C. input voltage range | $V_I$ | | 3 to 19 | V |
| Supply voltage rejection ratio; $R_S \leqslant 10$ kΩ | SVRR | typ. | 100 | μV/V |
| Equivalent input noise voltage<br>$R_S = 0$; f = 20 Hz to 20 kHz (r.m.s. value) | $V_{n(rms)}$ | typ. | 3,5 | μV |
| Equivalent input noise current<br>f = 20 Hz to 20 kHz (r.m.s. value) | $I_{n(rms)}$ | typ. | 0,05 | nA |
| Crosstalk between a switched-on input and a non-switched-on input; measured at the output at $R_S = 1$ kΩ; f = 1 kHz | $\alpha$ | typ. | 100 | dB |

**CHARACTERISTICS** (continued)

**Signal amplifier**

| | | | |
|---|---|---|---|
| Voltage gain of a switched-on input at $I_9 = I_{15} = 0$; $R_L = \infty$ | $G_v$ | typ. | 1 |
| Current gain of a switched-on amplifier | $G_i$ | typ. | $10^5$ |

**Signal outputs**

| | | | |
|---|---|---|---|
| Output resistance (pins 9 and 15) | $R_o$ | typ. | 400 Ω |
| Output current capability at $V_P$ = 6 to 23 V | $\pm I_9$; $\pm I_{15}$ | typ. | 5 mA |
| Frequency limit of the output voltage $V_{i(p\text{-}p)}$ = 1 V; $R_S$ = 1 kΩ; $R_L$ = 10 MΩ; $C_L$ = 10 pF | f | typ. | 1,3 MHz |
| Slew rate (unity gain); $\Delta V_{9\text{-}16}/\Delta t$; $\Delta V_{15\text{-}16}/\Delta t$ $R_L$ = 10 MΩ; $C_L$ = 10 pF | S | typ. | 2 V/μs |

**Bias voltage**

| | | | |
|---|---|---|---|
| D.C. output voltage | $V_{10\text{-}16}$ | typ.<br>10,2 to 11,8 | 11 V *<br>V |
| Output resistance | $R_{10\text{-}16}$ | typ. | 8,2 kΩ |

**Switch control**

| switched-on inputs | interconnected pins | control voltages | | |
|---|---|---|---|---|
| | | $V_{11\text{-}16}$ | $V_{12\text{-}16}$ | $V_{13\text{-}16}$ |
| I-1, II-1 | 1-15, 5-9 | H | H | H |
| I-2, II-2 | 2-15, 6-9 | H | H | L |
| I-3, II-3 | 3-15, 7-9 | H | L | H |
| I-4, II-4 | 4-15, 8-9 | L | H | H |
| I-4, II-4 | 4-15, 8-9 | L | L | H |
| I-4, II-4 | 4-15, 8-9 | L | H | L |
| I-4, II-4 | 4-15, 8-9 | L | L | L |
| I-3, II-3 | 3-15, 7-9 | H | L | L |

In the case of offset control, an internal blocking circuit of the switch control ensures that not more than one input will be switched on at a time. In that case safe switching-through is obtained at $V_{SL} \leqslant 1{,}5$ V.

**Control inputs** (pins 11, 12 and 13)

| | | | |
|---|---|---|---|
| Required voltage | | | |
| HIGH | $V_{SH}$ | > | 3,3 V ** |
| LOW | $V_{SL}$ | < | 2,1 V |
| Input current | | | |
| HIGH (leakage current) | $I_{SH}$ | < | 1 μA |
| LOW (control current) | $-I_{SL}$ | < | 250 μA |

* $V_{10\text{-}16}$ is typically $0{,}5 \cdot V_{14\text{-}16} + 1{,}5 \cdot V_{BE}$.

** Or control inputs open ($R_{11,12,13-16} > 33$ MΩ).

## APPLICATION INFORMATION

$V_P$ = 20 V; $T_{amb}$ = 25 °C; measured in Fig. 1; $R_S$ = 47 kΩ; $C_i$ = 0,1 μF; $R_{bias}$ = 470 kΩ; $R_L$ = 4,7 kΩ; $C_L$ = 100 pF (unless otherwise specified)

| | | | | |
|---|---|---|---|---|
| Voltage gain | $G_v$ | typ. | −1,5 | dB |
| Output voltage variation when switching the inputs | $\Delta V_{9-16}$; $\Delta V_{15-16}$ | typ. | 10 | mV |
| | | < | 100 | mV |
| Total harmonic distortion | | | | |
| over most of signal range (see Fig. 4) | $d_{tot}$ | typ. | 0,01 | % |
| $V_i$ = 5 V; f = 1 kHz | $d_{tot}$ | typ. | 0,02 | % |
| $V_i$ = 5 V; f = 20 Hz to 20 kHz | $d_{tot}$ | typ. | 0,03 | % |
| Output signal handling $d_{tot}$ = 0,1%; f = 1 kHz (r.m.s. value) | $V_{o(rms)}$ | > | 5,0 | V |
| | | typ. | 5,3 | V |
| Noise output voltage (unweighted) f = 20 Hz to 20 kHz (r.m.s. value) | $V_{n(rms)}$ | typ. | 5 | μV |
| Noise output voltage (weighted) f = 20 Hz to 20 kHz (in accordance with DIN 45405) | $V_n$ | typ. | 12 | μV |
| Amplitude response $V_i$ = 5 V; f = 20 Hz to 20 kHz; $C_i$ = 0,22 μF | $\Delta V_{9-16}$; $\Delta V_{15-16}$ | < | 0,1 | dB * |
| Crosstalk between a switched-on input and a non-switched-on input; measured at the output at f = 1 kHz | α | typ. | 75 | dB ** |
| Crosstalk between switched-on inputs and the outputs of the other channels | α | typ. | 90 | dB ** |

---

* The lower cut-off frequency depends on values of $R_{bias}$ and $C_i$.

** Depends on external circuitry and $R_S$. The value will be fixed mostly by capacitive crosstalk of the external components.

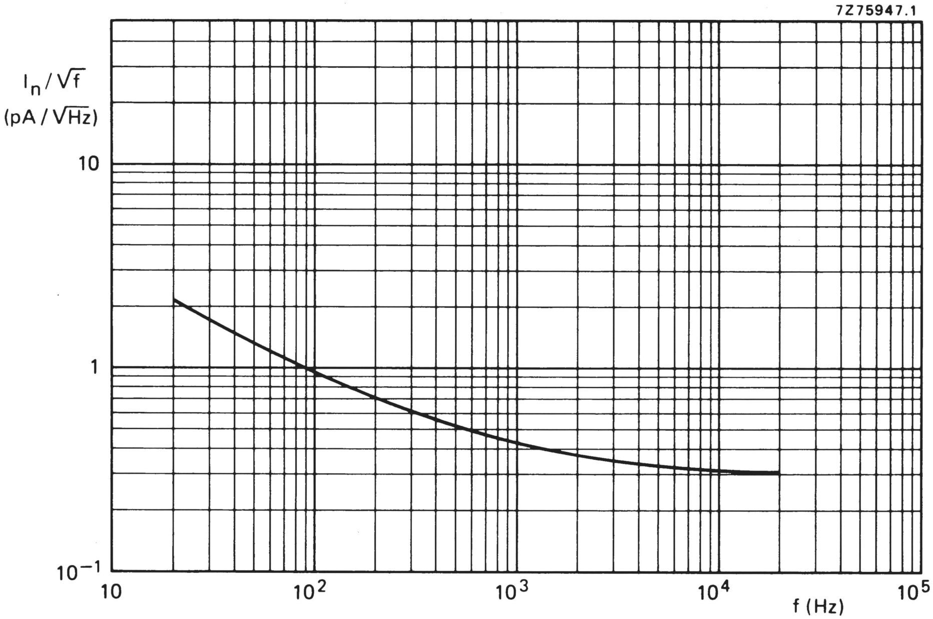


Fig. 2 Equivalent input noise current.

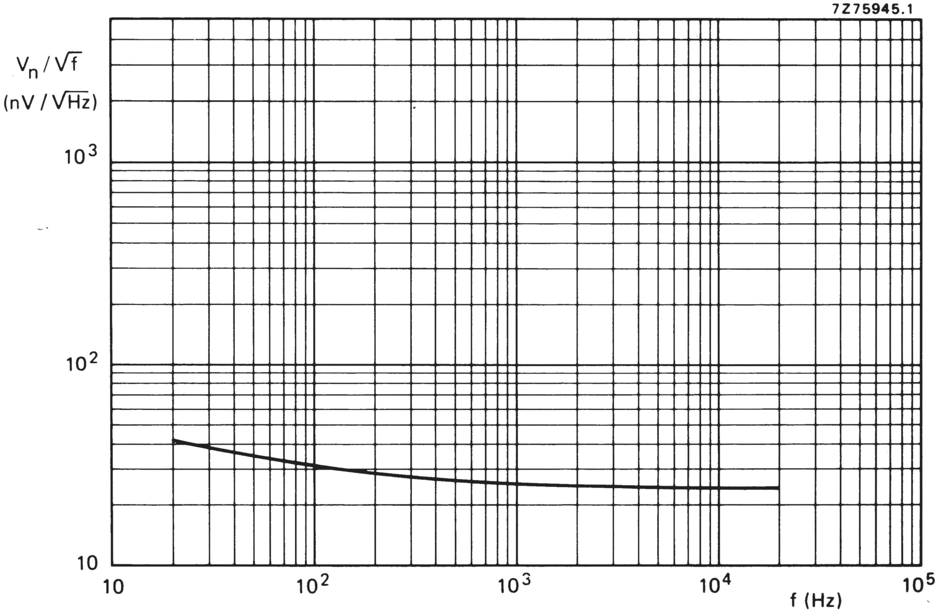


Fig. 3 Equivalent input noise voltage.

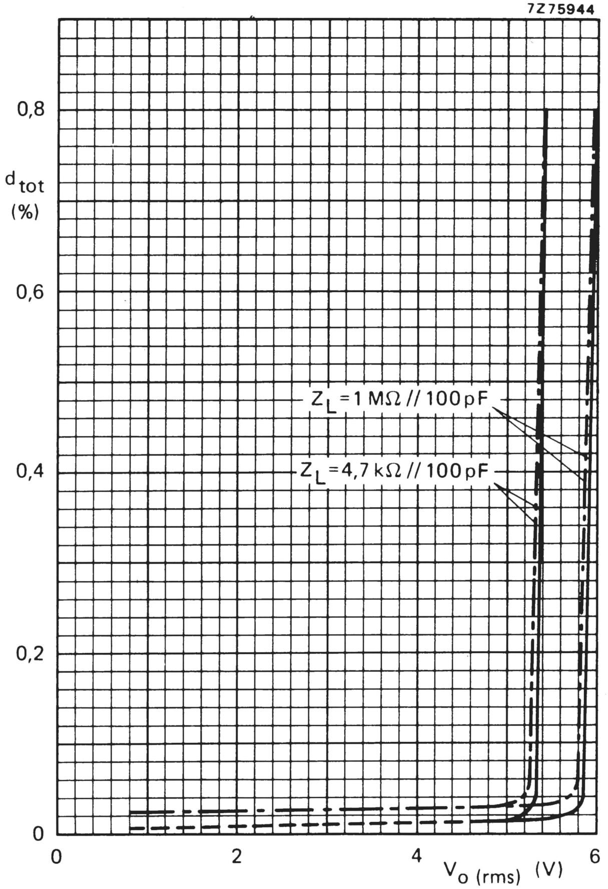


Fig. 4 Total harmonic distortion as a function of r.m.s. output voltage.
—— f = 1 kHz; — - — - f = 20 kHz.

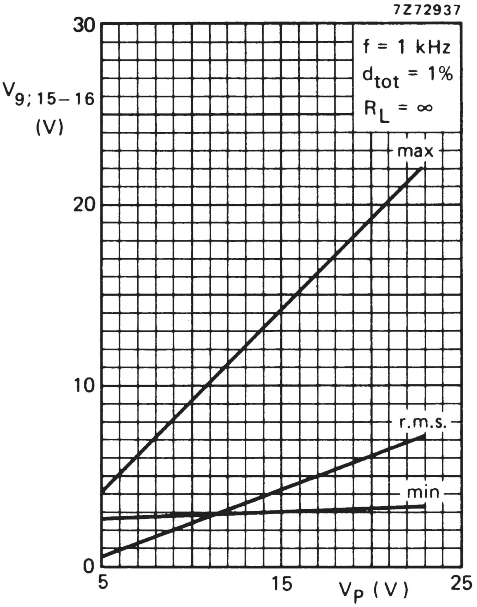


Fig. 5 Output voltage as a function of supply voltage.

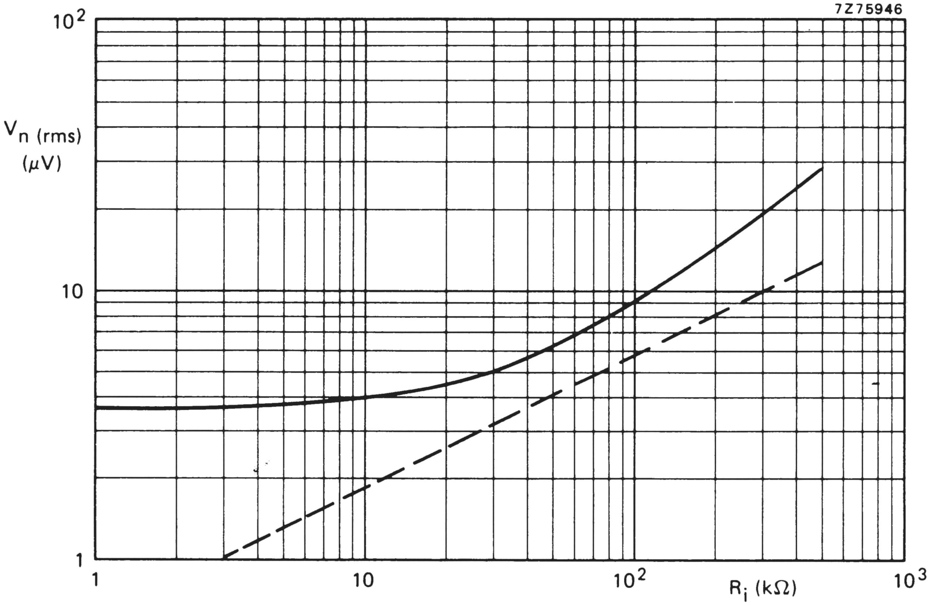


Fig. 6 Noise output voltage as a function of input resistance; $G_V = 1$; f = 20 Hz to 20 kHz.
—— $V_n$ (output); – – – $V_n$ ($R_S$).

## APPLICATION NOTES

### Input protection circuit and indication

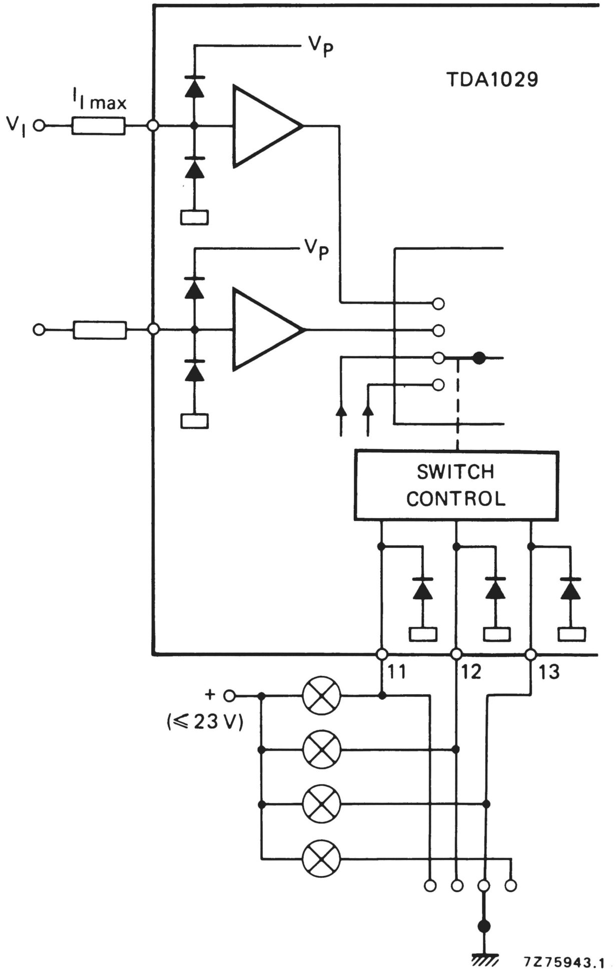

V_P
TDA1029
$I_{I\,max}$
$V_I$
V_P
SWITCH CONTROL
11
12
13
+
(≤ 23 V)
7Z75943.1

Fig. 7 Circuit diagram showing input protection and indication.

### Unused signal inputs

Any unused inputs must be connected to a d.c. (bias) voltage, which is within the d.c. input voltage range; e.g. unused inputs can be connected directly to pin 10.

### Circuits with standby operation

The control inputs (pins 11, 12 and 13) are high-ohmic at $V_{SH} \leqslant 20$ V ($I_{SH} \leqslant 1\ \mu$A), as well as, when the supply voltage (pin 14) is switched off.

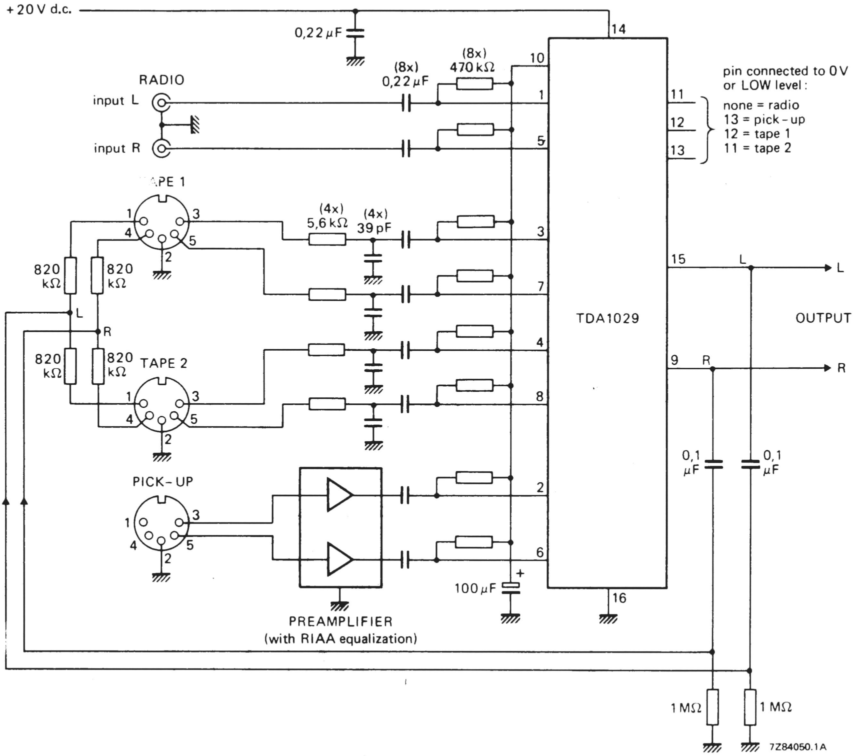

+20 V d.c.
0,22 μF
14
(8x)
0,22 μF
(8x)
470 kΩ
10
RADIO
input L
1
input R
5
pin connected to 0 V
or LOW level:
none = radio
13 = pick-up
12 = tape 1
11 = tape 2
11
12
13
TAPE 1
(4x)
5,6 kΩ
(4x)
39 pF
3
7
4
8
820 kΩ
L
R
TAPE 2
15
9
TDA1029
OUTPUT
L
R
PICK-UP
2
6
0,1 μF
100 μF
PREAMPLIFIER
(with RIAA equalization)
16
1 MΩ
7Z84050.1A

Fig. 8 TDA1029 connected as a four input stereo source selector.

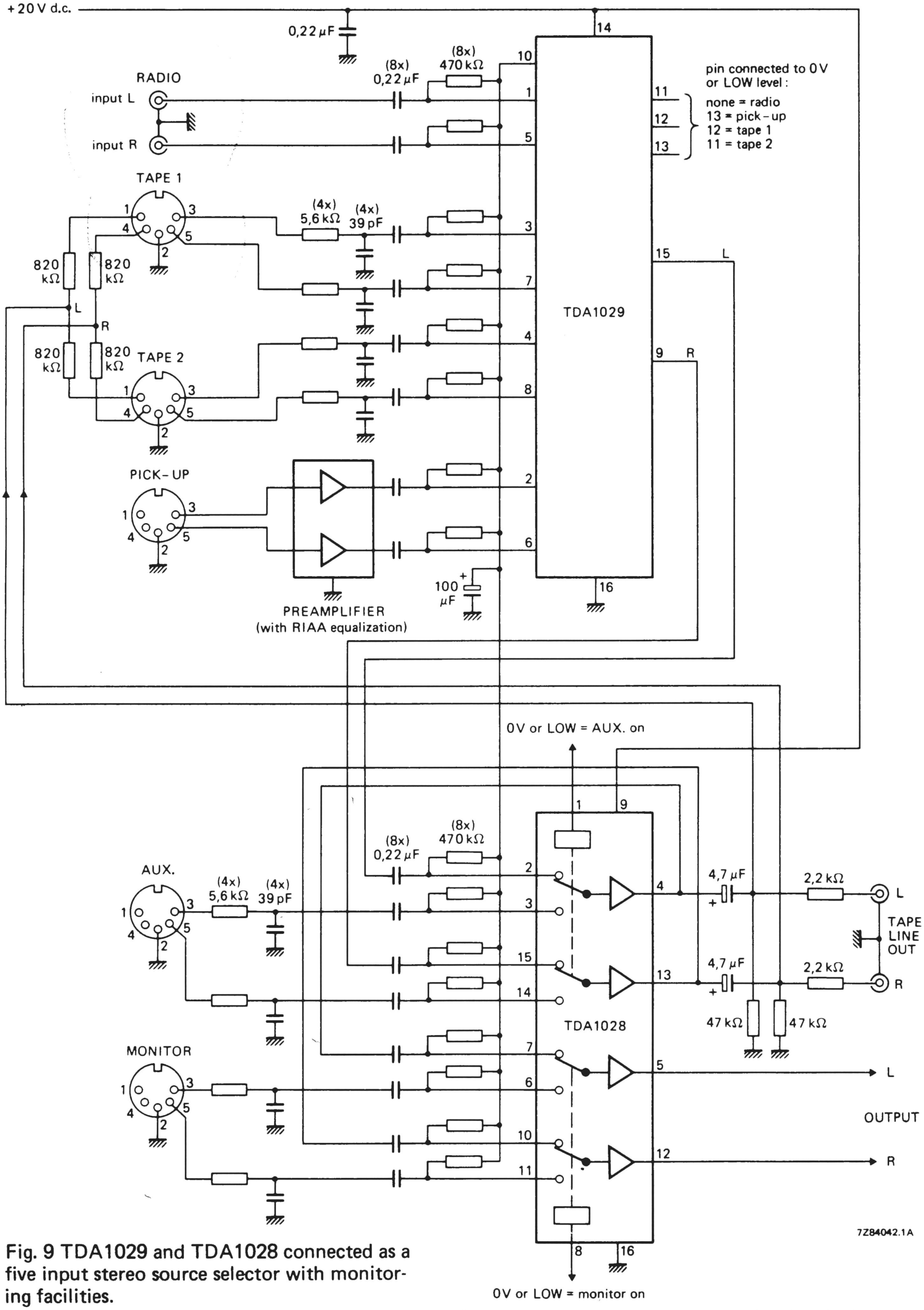

+20 V d.c.
0,22 μF
14
10
(8x)
470 kΩ
(8x)
0,22 μF
RADIO
input L
input R
1
5
pin connected to 0 V
or LOW level:
none = radio
13 = pick-up
12 = tape 1
11 = tape 2
11
12
13
TAPE 1
(4x)
5,6 kΩ
(4x)
39 pF
3
7
820 kΩ
820 kΩ
L
R
15
L
TDA1029
4
9
R
820 kΩ
820 kΩ
TAPE 2
8
PICK-UP
2
6
PREAMPLIFIER
(with RIAA equalization)
100 μF
16
0V or LOW = AUX. on
1
9
(8x)
0,22 μF
(8x)
470 kΩ
AUX.
(4x)
5,6 kΩ
(4x)
39 pF
2
3
4
4,7 μF
2,2 kΩ
L
TAPE
LINE
OUT
15
14
13
4,7 μF
2,2 kΩ
R
47 kΩ
47 kΩ
TDA1028
MONITOR
7
6
5
L
OUTPUT
10
11
12
R
8
16
0V or LOW = monitor on
7Z84042.1A

Fig. 9 TDA1029 and TDA1028 connected as a five input stereo source selector with monitoring facilities.

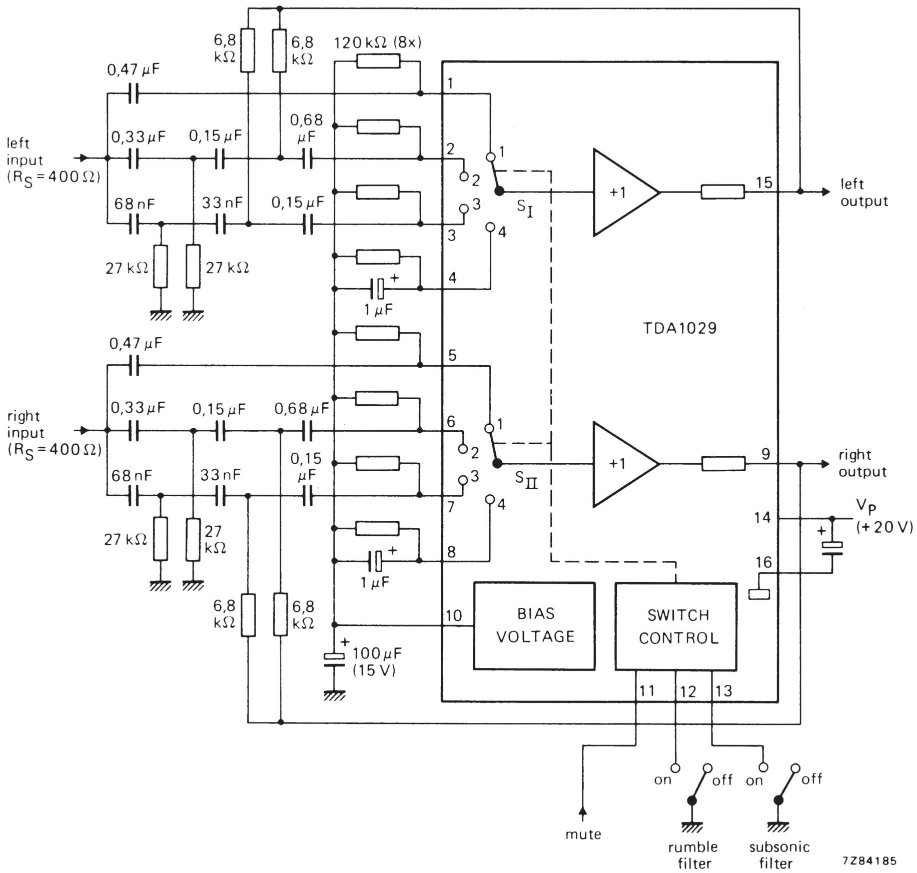

6,8 kΩ
6,8 kΩ
120 kΩ (8x)
0,47 µF
1
left input (R_S = 400 Ω)
0,33 µF
0,15 µF
0,68 µF
2
1
2
68 nF
33 nF
0,15 µF
3
3
4
S_I
+1
15
left output
27 kΩ
27 kΩ
4
+
1 µF
TDA1029
0,47 µF
5
right input (R_S = 400 Ω)
0,33 µF
0,15 µF
0,68 µF
6
1
2
68 nF
33 nF
0,15 µF
3
7
4
S_II
+1
9
right output
27 kΩ
27 kΩ
14
V_P (+20 V)
+
8
+
1 µF
16
6,8 kΩ
6,8 kΩ
10
BIAS VOLTAGE
SWITCH CONTROL
+
100 µF (15 V)
11
12
13
on
off
on
off
mute
rumble filter
subsonic filter
7Z84185

Fig. 10 TDA1029 connected as a third-order active high-pass filter with Butterworth response and component values chosen according to the method proposed by Fjällbrant. It is a four-function circuit which can select mute, rumble filter, subsonic filter and linear response.

Switch control

| function | $V_{11\text{-}16}$ | $V_{12\text{-}16}$ | $V_{13\text{-}16}$ |
|---|---|---|---|
| linear | H | H | H |
| subsonic filter 'on' | H | H | L |
| rumble filter 'on' | H | L | X |
| mute 'on' | L | X | X |

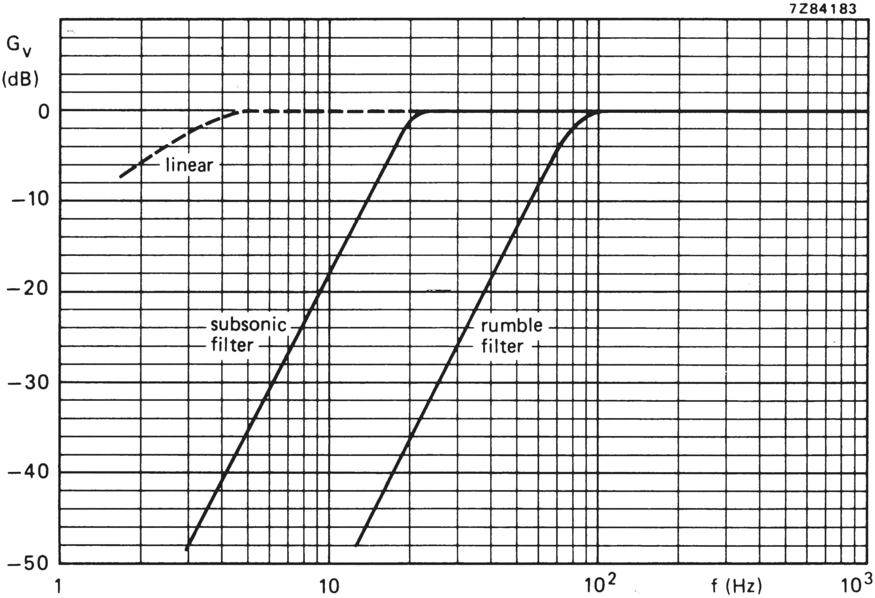


Fig. 11 Frequency response curves for the circuit of Fig. 10.

# 12 TO 20 W HI-FI AUDIO POWER AMPLIFIER

The TDA1512 is a monolithic integrated hi-fi audio power amplifier designed for asymmetrical power supplies for mains-fed apparatus.
Special features are:

- Thermal protection
- Low intermodulation distortion
- Low transient intermodulation distortion
- Built-in output current limiter
- Low input offset voltage
- Output stage with low cross-over distortion
- Single in-line (SIL) power package

## QUICK REFERENCE DATA

| | | | | |
|---|---|---|---|---|
| Supply voltage range | $V_P$ | | 15 to 35 | V |
| Total quiescent current at $V_P = 25$ V | $I_{tot}$ | typ. | 65 | mA |
| Output power at $d_{tot} = 0,7\%$ | | | | |
| sine-wave power | | | | |
| $V_P = 25$ V; $R_L = 4\ \Omega$ | $P_o$ | typ. | 13 | W |
| $V_P = 25$ V; $R_L = 8\ \Omega$ | $P_o$ | typ. | 7 | W |
| music power | | | | |
| $V_P = 32$ V; $R_L = 4\ \Omega$ | $P_o$ | typ. | 21 | W |
| $V_P = 32$ V; $R_L = 8\ \Omega$ | $P_o$ | typ. | 12 | W |
| Closed-loop voltage gain (externally determined) | $G_c$ | typ. | 30 | dB |
| Input resistance (externally determined) | $R_i$ | typ. | 20 | kΩ |
| Signal-to-noise ratio at $P_o = 50$ mW | S/N | typ. | 72 | dB |
| Supply voltage ripple rejection at f = 100 Hz | RR | typ. | 50 | dB |

## PACKAGE OUTLINES

TDA1512: 9-lead SIL; plastic power (SOT-131B).
TDA1512Q: 9-lead SIL-bent-to-DIL; plastic power (SOT-157B).

**PINNING**

1. Non-inverting input
2. Input ground (substrate)
3. Compensation
4. Ground potential
5. Output
6. Positive supply ($V_P$)
7. Externally connected to pin 6
8. Ripple rejection
9. Inverting input (feedback)

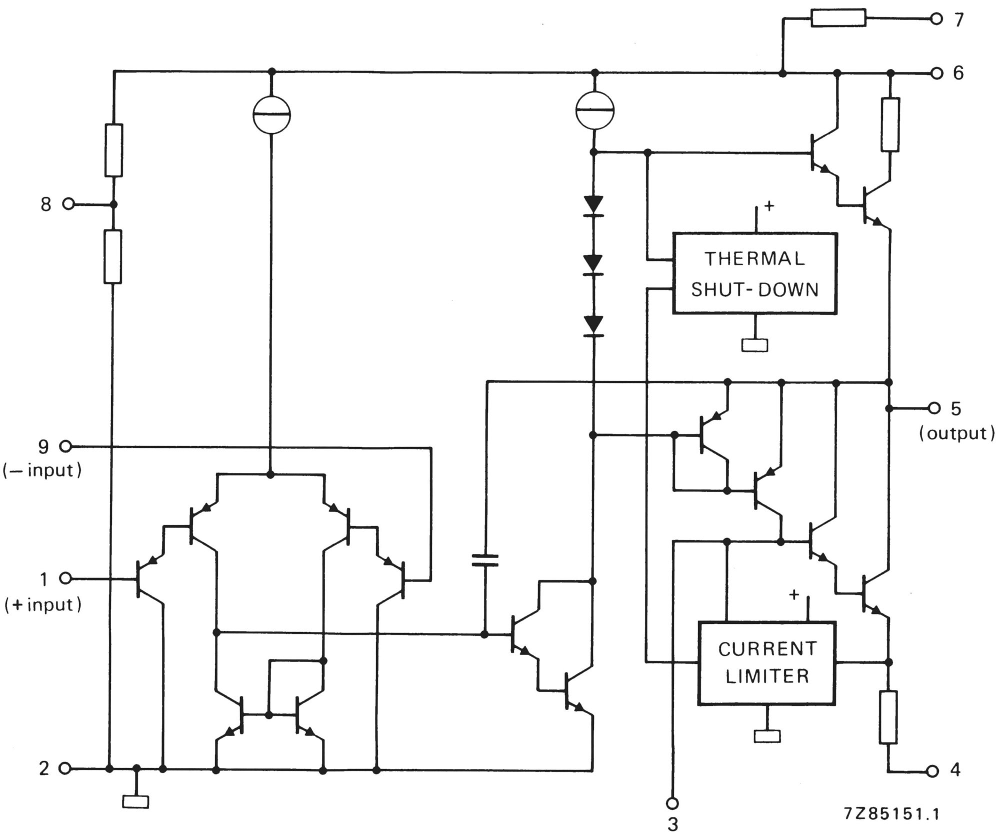

7
6
8
9
(– input)
1
(+ input)
2
THERMAL
SHUT-DOWN
+
5
(output)
CURRENT
LIMITER
+
4
3
7Z85151.1

Fig. 1 Simplified internal circuit diagram.

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | |
|---|---|---|---|
| Supply voltage | $V_P$ | max. | 35 V |
| Repetitive peak output current | $I_{ORM}$ | max. | 3,2 A |
| Non-repetitive peak output current | $I_{OSM}$ | max. | 5 A |
| Total power dissipation | see derating curve Fig. 2 | | |
| Storage temperature | $T_{stg}$ | | −55 to + 150 °C |
| Operating ambient temperature | $T_{amb}$ | | −25 to + 150 °C |
| A.C. short-circuit duration of load during full-load sine-wave drive $R_L = 0$; $V_P = 30$ V with $R_i = 4\ \Omega$ | $t_{sc}$ | max. | 100 hours |

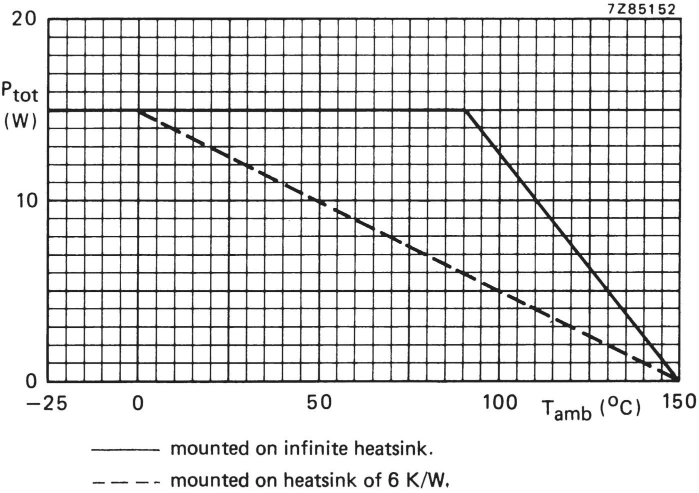


Fig. 2 Power derating curves.

## THERMAL RESISTANCE

| | | | |
|---|---|---|---|
| From junction to mounting base | $R_{th\ j\text{-}mb}$ | typ. | 3 K/W |
| | | $\leqslant$ | 4 K/W |

## D.C. CHARACTERISTICS

| | | | | |
|---|---|---|---|---|
| Supply voltage range | $V_P$ | | 15 to 35 | V |
| Total quiescent current at $V_P = 25$ V | $I_{tot}$ | typ. | 65 | mA |

## A.C. CHARACTERISTICS

$V_P = 25$ V; $R_L = 4\ \Omega$; f = 1 kHz; $T_{amb} = 25\ ^{\circ}C$; measured in test circuit of Fig. 3; unless otherwise specified

| | | | | |
|---|---|---|---|---|
| Output power | | | | |
| sine-wave power at $d_{tot} = 0,7$ % | | | | |
| $R_L = 4\ \Omega$ | $P_o$ | typ. | 13 | W |
| $R_L = 8\ \Omega$ | $P_o$ | typ. | 7 | W |
| music power at $V_P = 32$ V | | | | |
| $R_L = 4\ \Omega$; $d_{tot} = 0,7$ % | $P_o$ | typ. | 21 | W |
| $R_L = 4\ \Omega$; $d_{tot} = 10$ % | $P_o$ | typ. | 25 | W |
| $R_L = 8\ \Omega$; $d_{tot} = 0,7$ % | $P_o$ | typ. | 12 | W |
| $R_L = 8\ \Omega$; $d_{tot} = 10$ % | $P_o$ | typ. | 15 | W |
| Power bandwidth; −1,5 dB; $d_{tot} = 0,7$% | B | | 40 Hz to 16 | kHz |
| Voltage gain | | | | |
| open-loop | $G_o$ | typ. | 74 | dB |
| closed-loop | $G_c$ | typ. | 30 | dB |
| Input resistance (pin 1) | $R_i$ | > | 100 | kΩ |
| Input resistance of test circuit (Fig. 3) | $R_i$ | typ. | 20 | kΩ |
| Input sensitivity | | | | |
| for $P_o = 50$ mW | $V_i$ | typ. | 16 | mV |
| for $P_o = 10$ W | $V_i$ | typ. | 210 | mV |
| Signal-to-noise ratio | | | | |
| at $P_o = 50$ mW; $R_S = 2$ kΩ; f = 20 Hz to 20 kHz; unweighted | S/N | > | 68 | dB |
| weighted; measured according to IEC 173 (A-curve) | S/N | typ. | 76 | dB |
| Ripple rejection at f = 100 Hz | RR | typ. | 50 | dB |
| Total harmonic distortion at $P_o = 10$ W | $d_{tot}$ | typ.<br>< | 0,1<br>0,3 | %<br>% |
| Output resistance (pin 5) | $R_o$ | typ. | 0,1 | Ω |

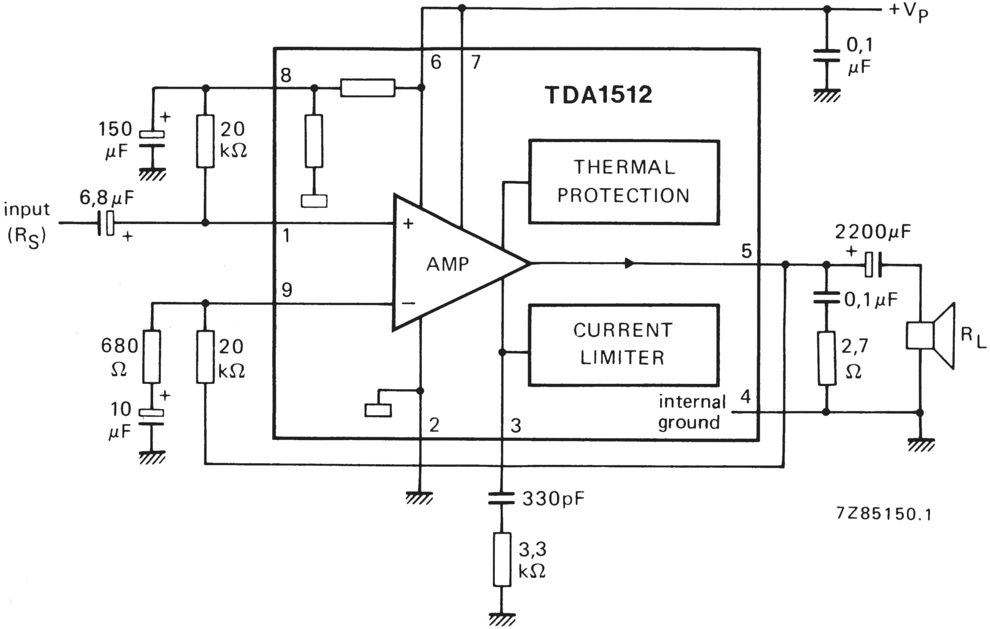

+V_P
0,1 μF
TDA1512
6
7
8
150 μF
+
20 kΩ
input (R_S)
6,8 μF
+
1
AMP
+
−
9
THERMAL PROTECTION
CURRENT LIMITER
5
2200μF
+
0,1μF
2,7 Ω
R_L
680 Ω
10 μF
+
20 kΩ
internal ground
4
2
3
330pF
3,3 kΩ
7Z85150.1

Fig. 3 Test circuit.

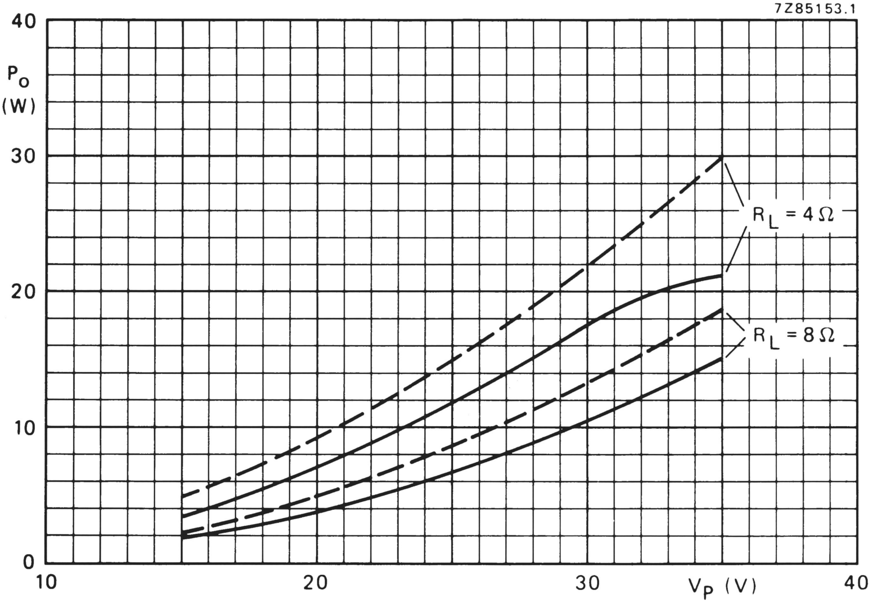


Fig. 4 Output power as a function of the supply voltage; f = 1 kHz;
——— $d_{tot}$ = 0,7 %; – – – $d_{tot}$ = 10 %.

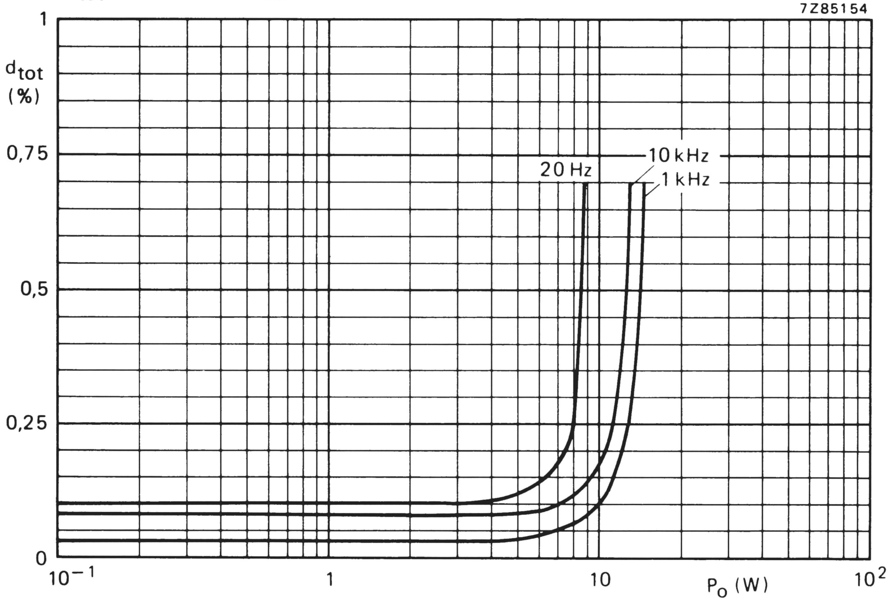


Fig. 5 Total harmonic distortion as a function of the output power.

# 20 W HI-FI AUDIO POWER AMPLIFIER

The TDA1520 is a monolithic integrated hi-fi audio power amplifier designed for asymmetrical or symmetrical power supplies for mains-fed apparatus.
Special features are:

- Thermal protection
- Very low intermodulation distortion
- Very low transient intermodulation distortion
- Built-in output current limiter
- Low input offset voltage
- Output stage with low cross-over distortion
- Single in-line (SIL) power package
- A.C. short-circuit protected

## QUICK REFERENCE DATA

| | | | | |
|---|---|---|---|---|
| Supply voltage range | $V_P$ | | 15 to 40 | V |
| Total quiescent current at $V_P = 33$ V | $I_{tot}$ | typ. | 45 | mA |
| Output power at $d_{tot} = 0,5\%$ | | | | |
| sine-wave power | | | | |
| $V_P = 33$ V; $R_L = 4\ \Omega$ | $P_o$ | typ. | 22 | W |
| $V_P = 33$ V; $R_L = 4\ \Omega$ | $P_o$ | > | 20 | W |
| $V_P = 33$ V; $R_L = 8\ \Omega$ | $P_o$ | typ. | 11 | W |
| Closed-loop voltage gain (externally determined) | $G_c$ | typ. | 30 | dB |
| Input resistance (externally determined by $R_{8-1}$) | $R_i$ | typ. | 20 | kΩ |
| Signal-to-noise ratio at $P_o = 50$ mW | S/N | typ. | 76 | dB |
| Supply voltage ripple rejection at f = 100 Hz | RR | typ. | 70 | dB |

## PACKAGE OUTLINE

9-lead SIL; plastic power (SOT-131A).

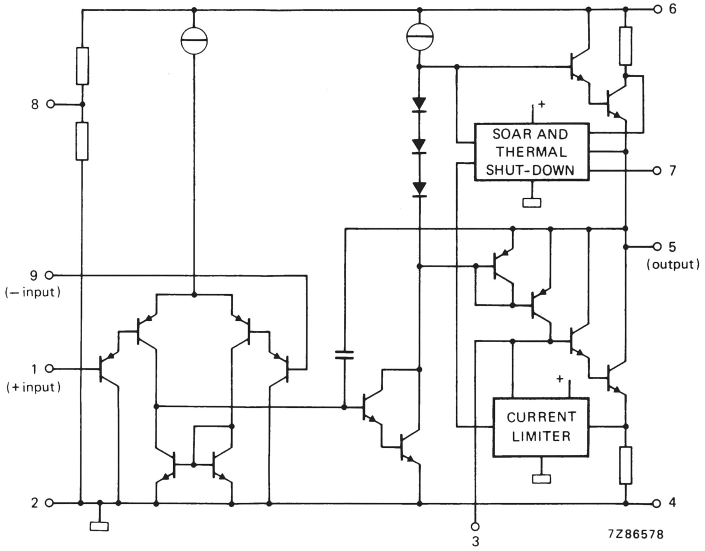

6
8
SOAR AND THERMAL SHUT-DOWN
7
5
(output)
9
(− input)
1
(+ input)
CURRENT LIMITER
2
3
4
7Z86578

Fig. 1 Simplified internal circuit diagram.

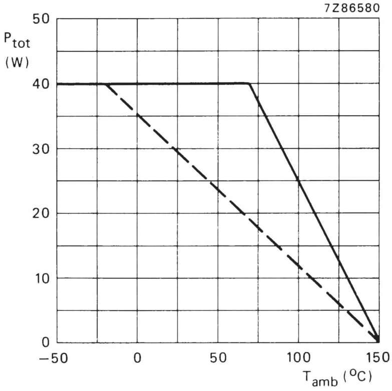
## PINNING

1. Non-inverting input
2. Input ground (substrate)
3. Compensation
4. Negative supply (ground)
5. Output
6. Positive supply ($V_P$)
7. Internally connected
8. Ripple rejection
9. Inverting input (feedback)

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | | |
|---|---|---|---|---|
| Supply voltage | $V_P$ | max. | 44 | V |
| Repetitive peak output current | $I_{ORM}$ | max. | 4 | A |
| Non-repetitive peak output current | $I_{OSM}$ | max. | 5 | A |
| Total power dissipation | see derating curve Fig. 2 | | | |
| Storage temperature | $T_{stg}$ | −55 to + 150 | | °C |
| Operating ambient temperature | $T_{amb}$ | −25 to + 150 | | °C |
| A.C. short-circuit duration of load during full-load sine-wave drive $R_L = 0$; $V_P = 28$ V with $R_i = 4\ \Omega$ | $t_{sc}$ | max. | 100 | hours |



——— mounted on infinite heatsink.

– – – mounted on heatsink of 2,3 K/W.

Fig. 2 Power derating curves.

## THERMAL RESISTANCE

| | | | | |
|---|---|---|---|---|
| From junction to mounting base | $R_{th\ j\text{-}mb}$ | $\leqslant$ | 2 | K/W |

## D.C. CHARACTERISTICS

| | | | | |
|---|---|---|---|---|
| Supply voltage range | $V_P$ | | 15 to 40 | V |
| Total quiescent current at $V_P = 33$ V | $I_{tot}$ | typ. | 45 | mA |

## A.C. CHARACTERISTICS

$V_P = 33$ V; $R_L = 4\ \Omega$; f = 1 kHz; $T_{amb} = 25\ ^{o}C$; measured in test circuit of Fig. 3; unless otherwise specified

| | | | | |
|---|---|---|---|---|
| Output power | | | | |
| sine-wave power at $d_{tot} = 0,5\%$ | | | | |
| $R_L = 4\ \Omega$ | $P_o$ | typ. | 22 | W |
| $R_L = 4\ \Omega$ | $P_o$ | > | 20 | W |
| $R_L = 8\ \Omega$ | $P_o$ | typ. | 11 | W |
| Power bandwidth; –3 dB; $d_{tot} = 0,5\%$ | B | 20 Hz to | 20 | kHz |
| Voltage gain | | | | |
| open-loop | $G_o$ | typ. | 74 | dB |
| closed-loop | $G_c$ | typ. | 30 | dB |
| Input resistance (pin 1) | $R_i$ | > | 1 | MΩ |
| Input resistance of test circuit (Fig. 3) | $R_i$ | typ. | 20 | kΩ |
| Input sensitivity | | | | |
| for $P_o = 50$ mW | $V_i$ | typ. | 16 | mV |
| for $P_o = 16$ W | $V_i$ | typ. | 260 | mV |
| Signal-to-noise ratio | | | | |
| at $P_o = 50$ mW; $R_S = 2$ kΩ; f = 20 Hz to 20 kHz; unweighted | S/N | typ. | 76 | dB |
| weighted; measured according to IEC 173 (A-curve) | S/N | typ. | 80 | dB |
| Ripple rejection at f = 100 Hz | RR | typ. | 70 | dB |
| Total harmonic distortion at $P_o = 16$ W | $d_{tot}$ | typ. | 0,01 | % |
| Output resistance (pin 5) | $R_o$ | typ. | 0,01 | Ω |
| | $R_o$ | < | 0,1 | Ω |

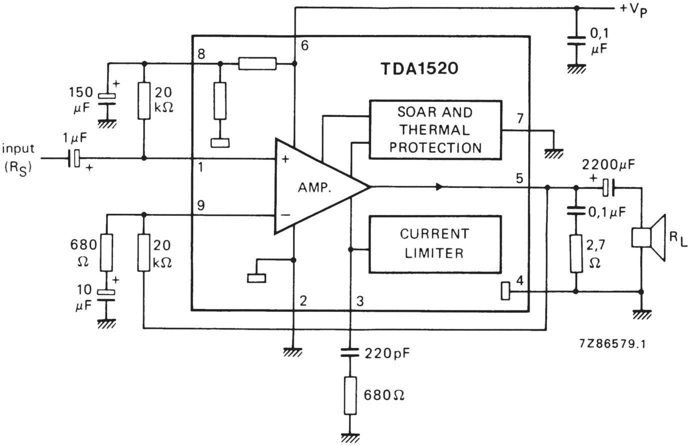

+V_P
0,1 μF
6
8
TDA1520
150 μF
20 kΩ
SOAR AND THERMAL PROTECTION
7
input (R_S)
1 μF
1
AMP.
2200μF
5
9
0,1 μF
680 Ω
20 kΩ
CURRENT LIMITER
R_L
2,7 Ω
10 μF
4
2
3
220pF
680Ω
7Z86579.1

Fig. 3 Test circuit.

This information is derived from development samples
made available for evaluation. It does not necessarily
imply that the device will go into regular production.

# STEREO-TONE VOLUME CONTROL CIRCUIT

## GENERAL DESCRIPTION

The TDA1524 is a monolithic integrated circuit designed as an active stereo-tone volume control for car radios, TV receivers and mains-fed equipment. It includes functions for bass and treble control, volume control with built-in contour (can be switched off) and balance. All these functions can be controlled by d.c. voltages or by single linear potentiometers.

### Features

- Few external components necessary
- Low noise due to internal gain
- Base emphasis can be increased by an additional filter
- Wide power supply voltage range

## QUICK REFERENCE DATA

| | | | | |
|---|---|---|---|---|
| Supply voltage (pin 3) | $V_P = V_{3\text{-}18}$ | typ. | 12 | V |
| Supply current (pin 3) | $I_P = I_3$ | typ. | 35 | mA |
| Maximum input signal with d.c. feedback (r.m.s. value) | $V_{i(rms)}$ | typ. | 3 | V |
| Maximum output signal with d.c. feedback (r.m.s. value) | $V_{o(rms)}$ | typ. | 3 | V |
| Volume control range | $G_v$ | −80 to | +21,5 | dB |
| Bass control range at 40 Hz | $\Delta G_v$ | typ. | ± 15 | dB |
| Treble control range at 16 kHz | $\Delta G_v$ | typ. | ± 15 | dB |
| Total harmonic distortion | THD | max. | 0,5 | % |
| Output noise voltage (r.m.s. value) | $V_{no(rms)}$ | max. | 100 | μV |
| Cross-talk attenuation at $G_v$ = −20 to + 21,5 dB | $\alpha_{ct}$ | typ. | 60 | dB |
| Tracking between channels at $G_v$ = −20 to + 21,5 dB | $\Delta G_v$ | max. | 2,5 | dB |
| Ripple rejection at 100 Hz | $\alpha_{100}$ | typ. | 50 | dB |
| Supply voltage range (pin 3) | $V_P = V_{3\text{-}18}$ | 7,5 to | 16,5 | V |
| Operating ambient temperature range | $T_{amb}$ | −30 to | + 80 | °C |

**A COMPLETE DATA SHEET IS AVAILABLE UPON REQUEST**

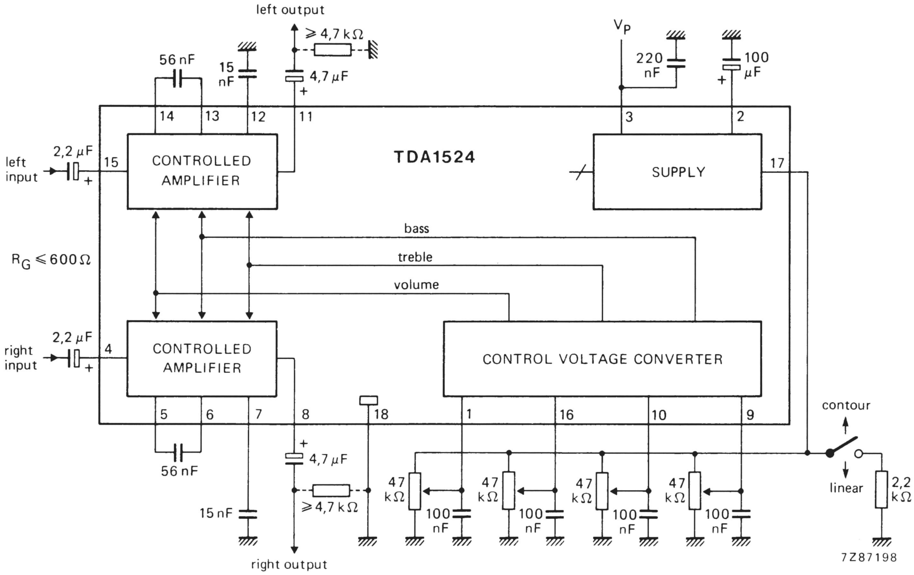

left output
≥ 4,7 kΩ
56 nF
15 nF
4,7 μF
+
VP
220 nF
100 μF
+
14
13
12
11
3
2
left input
2,2 μF
+
15
CONTROLLED AMPLIFIER
TDA1524
SUPPLY
17
bass
treble
volume
RG ≤ 600 Ω
right input
2,2 μF
+
4
CONTROLLED AMPLIFIER
CONTROL VOLTAGE CONVERTER
5
6
7
8
18
1
16
10
9
contour
linear
2,2 kΩ
56 nF
+
4,7 μF
≥ 4,7 kΩ
15 nF
47 kΩ
100 nF
47 kΩ
100 nF
47 kΩ
100 nF
47 kΩ
100 nF
right output
7Z87198

Fig. 1 Block diagram and application circuit.

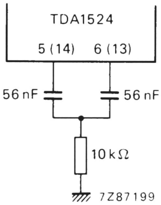

TDA1524
5 (14)
6 (13)
56 nF
56 nF
10 kΩ
7Z87199

Fig. 2 Double-pole low-pass filter for improved bass-boost.

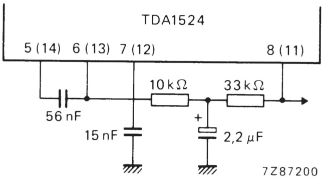

TDA1524
5 (14)
6 (13)
7 (12)
8 (11)
10 kΩ
33 kΩ
56 nF
15 nF
+
2,2 μF
7Z87200

Fig. 3 D.C. feedback with filter network for improved signal handling.

# CHROMINANCE COMBINATION

The TDA2510 is an integrated chrominance amplifier circuit for colour television receivers incorporating the following functions:

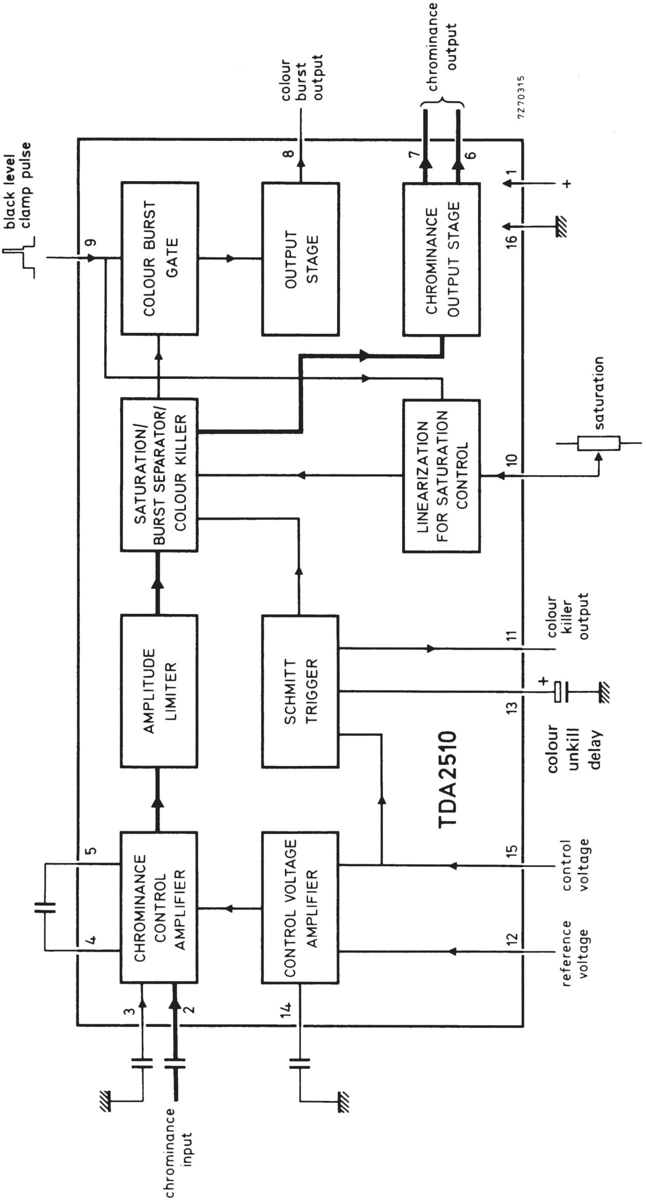
- chrominance amplifier with a.c c.
- control voltage amplifier
- burst separator
- colour killer and colour killer voltage detector
- linear electronic potentiometer for saturation control
- Schmitt trigger for colour killer
- chrominance delay line driver stage
- colour burst output stage

| QUICK REFERENCE DATA | | | | |
|---|---|---|---|---|
| Supply voltage | $V_{1-16}$ | typ. | 12 | V |
| Input signal (colour bars) peak-to-peak value | $V_{2-16(p-p)}$ | typ. | 100 | mV |
| Output signal (colour bars) peak-to-peak value | $V_{7-16(p-p)}$ | typ. | 0,5 | V |
| Burst signal output peak-to-peak value | $V_{8-16(p-p)}$ | typ. | 0,5 | V |

**PACKAGE OUTLINES**

TDA2510 : 16-lead DIL; plastic (SOT-38).
TDA2510Q : 16-lead QIL; plastic (SOT-58).

## BLOCK DIAGRAM


TDA2510
CHROMINANCE CONTROL AMPLIFIER
AMPLITUDE LIMITER
SATURATION/ BURST SEPARATOR/ COLOUR KILLER
COLOUR BURST GATE
CONTROL VOLTAGE AMPLIFIER
SCHMITT TRIGGER
OUTPUT STAGE
LINEARIZATION FOR SATURATION CONTROL
CHROMINANCE OUTPUT STAGE
black level clamp pulse
colour burst output
chrominance output
chrominance input
reference voltage
control voltage
colour unkill delay
colour killer output
saturation
+
+
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
7Z70315

**RATINGS** Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltage

| | | | | |
|---|---|---|---|---|
| Supply voltage (pin 1) | $V_{1-16}$ | max. | 15 | V |

Power dissipation

| | | | | |
|---|---|---|---|---|
| Total power dissipation | $P_{tot}$ | max. | 500 | mW |

Temperatures

| | | | | |
|---|---|---|---|---|
| Storage temperature | $T_{stg}$ | | −20 to +125 | °C |
| Operating ambient temperature | $T_{amb}$ | | −20 to +60 | °C |

**CHARACTERISTICS** at $V_{1-16} = 12$ V; $T_{amb} = 25$ °C

**Chrominance input signal**

| | | | | |
|---|---|---|---|---|
| Input voltage (symmetrical or asymmetrical) colour bars (peak-to-peak value) | $V_{2-16(p-p)}$ | typ. | 100 | mV |
| Input voltage range | $V_{2-16}$ | | 10 to 200 | mV |
| Input impedance | $\lvert Z_{2-16} \rvert$ | > | 2 | kΩ |

**Burst signal output** (emitter follower)

| | | | | |
|---|---|---|---|---|
| D.C. voltage | $V_{8-16}$ | typ. | 9 | V |
| Output signal (peak-to-peak value) | $V_{8-16(p-p)}$ | typ. | 0,5 | V (1) |
| Limiting level of output signal (peak-to-peak value) | $V_{8-16(p-p)}$ | typ. | 1,5 | V |

**Chrominance output signal** (without burst)

| | | | | |
|---|---|---|---|---|
| D.C. voltage | $V_{6-16}$ | typ. | 7 | V |
| Output signal (colour bars) at nominal saturation (see note 2) and maximum contrast (peak-to-peak value) | $V_{6-16(p-p)}$ | typ. | 0,5 | V |
| Signal-to-noise ratio | S/N | > | 50 | dB |
| Saturation control range | | | +6 to −50 | dB |
| Phase angle compared to burst output at nom. saturation | $\Delta\varphi_B$ | < | ±5° | |
| Phase angle shift during saturation control range +6 to −50 dB | $\Delta\varphi_C$ | < | ±5° | |
| Collector current of output transistor | $I_7$ | < | 20 | mA |

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1) Kept constant by a.c.c. circuit.

2) Nominal saturation is defined as maximum saturation −6 dB.

**CHARACTERISTICS** (continued)

| | | | | |
|---|---|---|---|---|
| Collector voltage of output transistor at $P_{tot\ max}$ = 100 mW | $V_{7-16}$ | $<$ | 20 | V |

**Control voltage amplifier input**

| | | | | |
|---|---|---|---|---|
| Reference voltage | $V_{12-16}$ | typ. | 7 | V |
| Control voltage | $V_{12-15}$ | typ. | $V_{12-16}-1,5$ | V |
| Input impedance | $\|Z_{15-16}\|$ | $>$ | 500 | kΩ |

**Linearization for saturation input**

| | | | | |
|---|---|---|---|---|
| Linear part of control curve | $V_{10-16}$ | | 1,75 to 4 | V |
| Threshold voltage for 50 dB suppression | $V_{10-16}$ | $>$<br>typ. | 1,6<br>1,75 | V<br>V |
| Adjustment voltage behaviour for higher chrominance output voltage | | positive-going | | |
| Input impedance | $\|Z_{9-16}\|$ | typ. | 10 | kΩ |

**Colour killer input** at pin 15

| | | | | |
|---|---|---|---|---|
| Input voltage for : colour on | $V_{15-16}$ | $<$ | 5,7 | V |
| for : colour off | $V_{15-16}$ | $>$ | 6,0 | V |
| Signal suppression at colour off | | $>$ | 50 | dB |

**Colour killer output**

| | | | | |
|---|---|---|---|---|
| Switching voltage for : colour on | $V_{11-16}$ | typ. | $V_{1-16}$ | V |
| for : colour off | $V_{11-16}$ | $<$ | 0,5 | V |
| Internal resistance | $R_i$ | typ. | 10 | kΩ |
| Collector current of output transistor | $I_{11}$ | $<$ | 10 | mA |

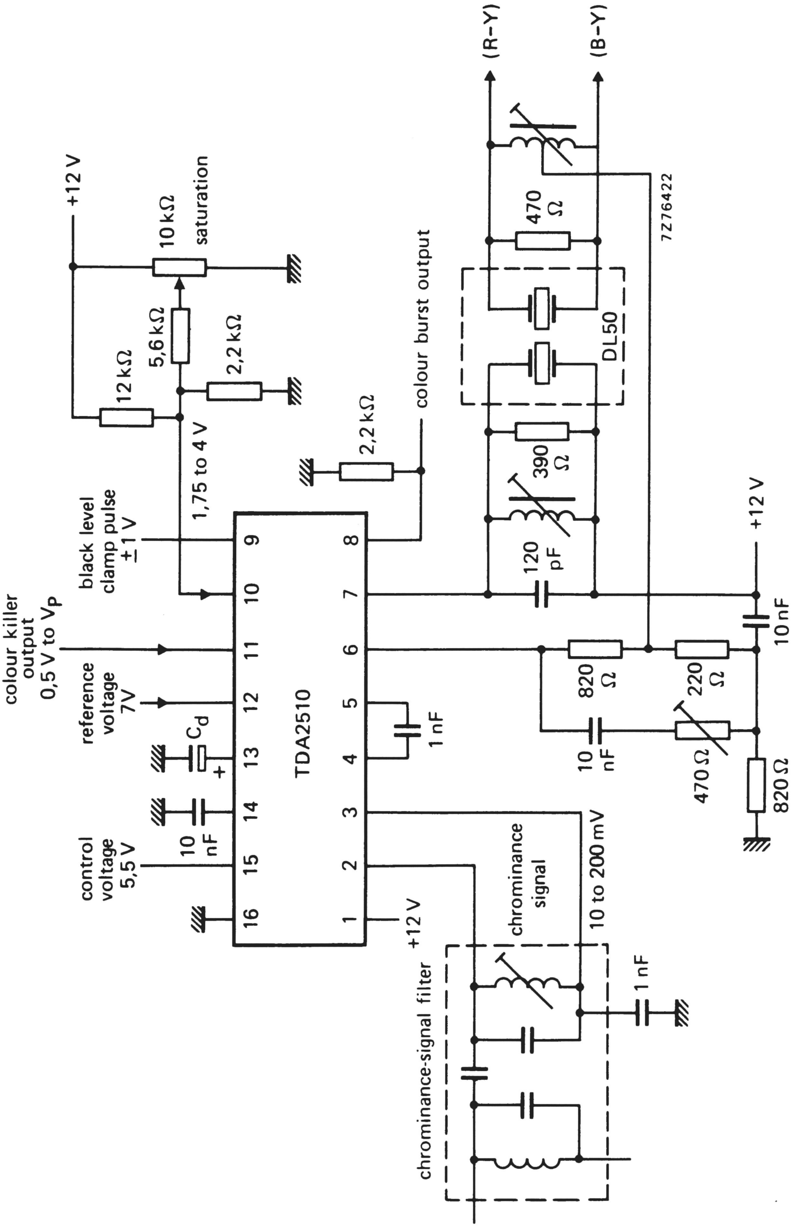
**Burst gating and blanking pulse**

| | | | | |
|---|---|---|---|---|
| Burst gating and blanking pulse (positive or negative) | $\pm V_{9-16}$ | | 1 to 4 | V |
| Input impedance | $\|Z_{9-16}\|$ | typ. | 1 | kΩ |

**Colour killer**

| | | | | |
|---|---|---|---|---|
| Colour unkill delay; depends on $C_d$ (see circuit on page 5) | $t_d$ | typ. | 24 | ms/μF |

## APPLICATION INFORMATION


TDA2510
+12 V
10 kΩ
saturation
5,6 kΩ
2,2 kΩ
12 kΩ
1,75 to 4 V
black level
clamp pulse
±1 V
colour killer
output
0,5 V to V_P
reference
voltage
7V
C_d
+
10
nF
control
voltage
5,5 V
16
15
14
13
12
11
10
9
1
2
3
4
5
6
7
8
+12 V
2,2 kΩ
colour burst output
1 nF
chrominance
signal
10 to 200 mV
chrominance-signal filter
1 nF
(R–Y)
(B–Y)
470 Ω
DL50
390 Ω
120 pF
820 Ω
220 Ω
10 nF
+12 V
10 nF
470 Ω
820 Ω
7Z76422

# COLOUR DEMODULATOR COMBINATION

The TDA2520 is an integrated synchronous demodulator combination for colour television receivers incorporating the following functions :

- 8, 8 MHz oscillator followed by a divider giving two 4, 4 MHz signals used as reference signals
- keyed burst phase detector for optimum noise behaviour
- a stage to obtain chrominance signal control (a.c.c.) and an a.c.c. reference level
- a colour killer and identification signal detector
- two synchronous demodulators for the (B-Y) and (R-Y) signals
- temperature compensated emitter follower outputs
- PAL switch
- PAL flip-flop
- integrated capacitors in the symmetrical demodulators reduce unwanted carrier-signals at the outputs.

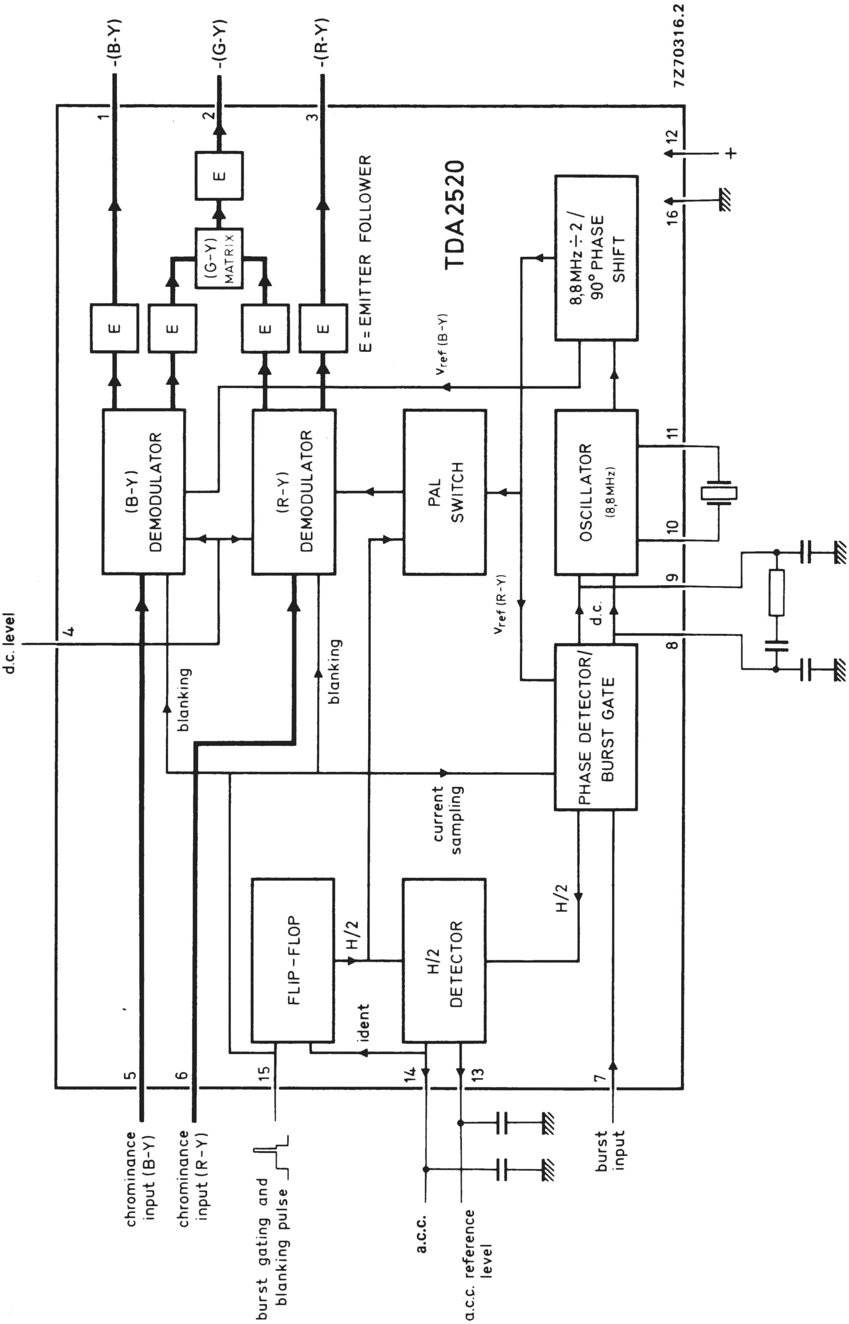
## QUICK REFERENCE DATA

| | | | | | |
|---|---|---|---|---|---|
| Supply voltage | | $V_{12-16}$ | typ. | 12 | V |
| Supply current | | $I_{12}$ | typ. | 40 | mA |
| Colour difference output signals peak-to-peak values | -(R-Y) | $V_{3-16(p-p)}$ | > | 2, 4 | V |
| | -(G-Y) | $V_{2-16(p-p)}$ | > | 1, 35 | V |
| | -(B-Y) | $V_{1-16(p-p)}$ | > | 3 | V |
| Impedance of colour difference signal outputs | | | typ. | 250 | Ω |

**PACKAGE OUTLINES**

TDA2520 : 16-lead DIL ; plastic (SOT-38).
TDA2520Q : 16-lead QIL ; plastic (SOT-58).

## BLOCK DIAGRAM


7Z70316.2
TDA2520
E = EMITTER FOLLOWER
-(B-Y)
-(G-Y)
-(R-Y)
1
2
3
E
(G-Y) MATRIX
(B-Y) DEMODULATOR
(R-Y) DEMODULATOR
PAL SWITCH
OSCILLATOR (8,8 MHz)
8,8 MHz ÷ 2 / 90° PHASE SHIFT
$V_{ref}$ (B-Y)
$V_{ref}$ (R-Y)
PHASE DETECTOR/ BURST GATE
d.c.
d.c. level
4
blanking
current sampling
FLIP-FLOP
H/2
H/2 DETECTOR
ident
12
+
16
11
10
9
8
5
6
15
14
13
7
chrominance input (B-Y)
chrominance input (R-Y)
burst gating and blanking pulse
a.c.c.
a.c.c. reference level
burst input

**RATINGS** Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | | | |
|---|---|---|---|---|---|
| Voltage | | | | | |
| Supply voltage | | $V_{12-16}$ | max. | 14 | V |
| Power dissipation | | | | | |
| Total power dissipation | | $P_{tot}$ | max. | 600 | mW |
| Temperatures | | | | | |
| Storage temperature | | $T_{stg}$ | | -20 to +125 | $^oC$ |
| Operating ambient temperature | | $T_{amb}$ | | -20 to +60 | $^oC$ |

**CHARACTERISTICS** at $V_{12-16} = 12$ V; $T_{amb} = 25\ ^oC$

**Demodulator part**

| | | | | | |
|---|---|---|---|---|---|
| Ratio of demodulated signals | B-Y/R-Y: | $\frac{V_{1-16}}{V_{3-16}}$ | typ. | 1, 78 | |
| | G-Y/R-Y: | $\frac{V_{2-16}}{V_{3-16}}$ | typ. | 0, 85 | 1) |
| | G-Y/R-Y: | $\frac{V_{2-16}}{V_{3-16}}$ | typ. | 0, 17 | 2) |
| Colour difference output signals 3) peak-to-peak values | -(R-Y) | $V_{3-16(p-p)}$ | > | 2, 4 | V |
| | -(G-Y) | $V_{2-16(p-p)}$ | > | 1, 35 | V |
| | -(B-Y) | $V_{1-16(p-p)}$ | > | 3 | V |
| Impedance of colour difference signal outputs | | $\lvert Z_{3-16}\rvert$ | typ. | 250 | Ω |
| | | $\lvert Z_{2-16}\rvert$ | typ. | 250 | Ω |
| | | $\lvert Z_{1-16}\rvert$ | typ. | 250 | Ω |
| H/2 ripple at R-Y output (peak-to-peak value) | | | < | 10 | mV |
| Blanking and keying pulse | | | | | |
| burst keying: active for | | $V_{15-16}$ | > | 7, 5 | V |
| inactive for | | $V_{15-16}$ | < | 6, 5 | V |
| blanking: active for | | $V_{15-16}$ | > | 2 | V |
| inactive for | | $V_{15-16}$ | < | 1 | V |

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1) The demodulators are driven by a chrominance signal of equal amplitude for the (R-Y) and the (B-Y) components. The phase of the (R-Y) chrominance signal equals the phase of the (R-Y) reference signal.
The same holds for the (B-Y) signals.

2) As under note 1, but the phase of the (R-Y) reference signal reversed.

3) The d.c. level of the colour difference outputs can be adjusted from 6 to 10 V at pin 4.

## CHARACTERISTICS (continued)

**Reference part**

| | | | |
|---|---|---|---|
| Colour burst (peak-to-peak value) | $V_{7\text{-}16(p\text{-}p)}$ | typ. | 0, 5 V |
| Phase difference between reference and burst signals for ±400 Hz deviation of crystal frequency | | < | ±5° |
| Overall holding range with typical crystal | $\Delta f$ | typ. | ±500 Hz |
| A.C.C. reference output voltage | $V_{13\text{-}16}$ | typ. | 7 V |
| A.C.C. voltage at 0, 5 V peak-to-peak burst | | | |
| at correct phase | $V_{14\text{-}16}$ | typ. | 5, 5 V |
| with zero burst | $V_{14\text{-}16}$ | typ. | 7, 0 V |
| Oscillator input resistance | $R_{11\text{-}16}$ | typ. | 270 Ω |
| Oscillator input capacitance | $C_{11\text{-}16}$ | see note | |
| Oscillator output resistance | $R_{10\text{-}16}$ | typ. | 200 Ω |

Note : to be established.

# COLOUR DEMODULATOR COMBINATION

The TDA2522 is an integrated synchronous demodulator combination for colour television receivers incorporating the following functions :

- 8, 8 MHz oscillator followed by a divider giving two 4, 4 MHz signals used as reference signals
- keyed burst phase detector for optimum noise behaviour
- a.c.c. detector and amplifier
- a colour killer
- two synchronous demodulators for the (B-Y) and (R-Y) signals
- temperature compensated emitter follower outputs
- PAL switch and PAL flip-flop with internal identification
- integrated capacitors in the symmetrical demodulators reduce unwanted carrier signals at the outputs

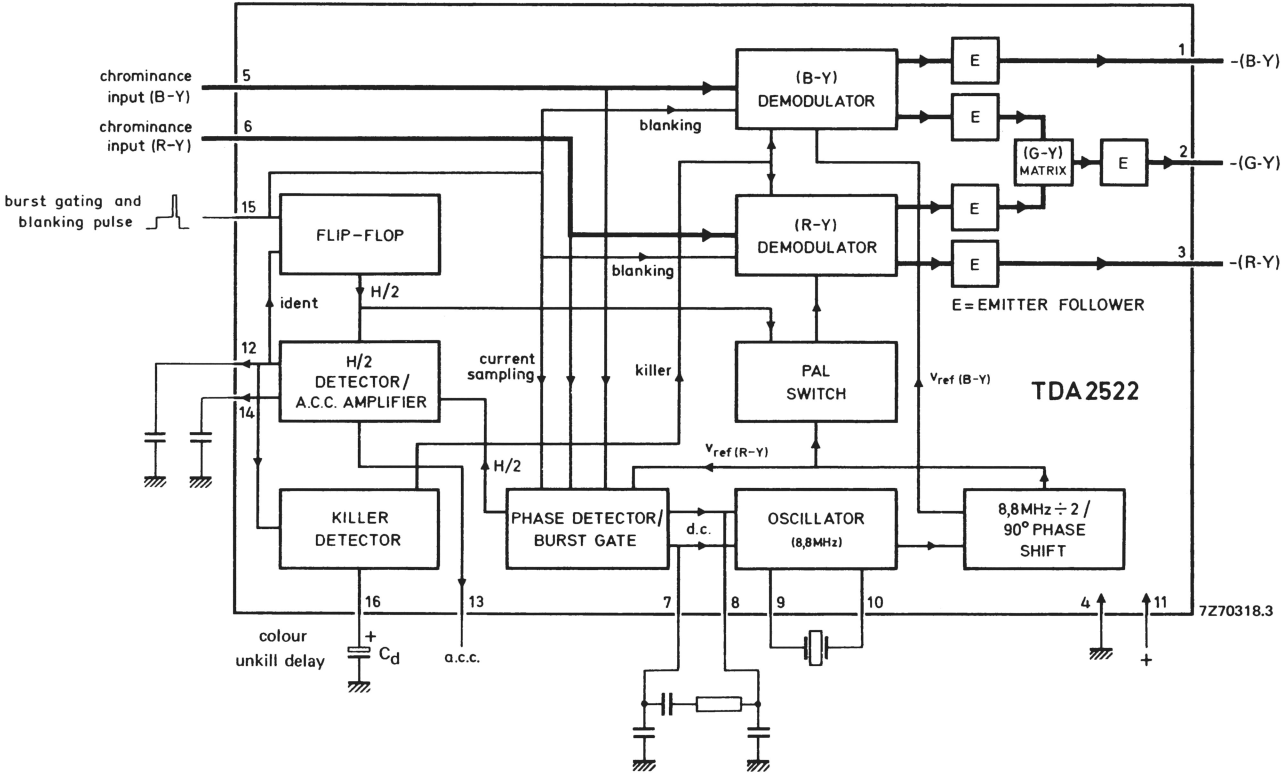
**QUICK REFERENCE DATA**

| | | | | | |
|---|---|---|---|---|---|
| Supply voltage | | $V_{11-4}$ | typ. | 12 | V |
| Supply current | | $I_{11}$ | typ. | 40 | mA |
| Colour difference output signals peak-to-peak values; for the following input signals | −(R-Y) | $V_{3-4(p-p)}$ | > | 2, 4 | V |
| | −(G-Y) | $V_{2-4(p-p)}$ | > | 1, 35 | V |
| | −(B-Y) | $V_{1-4(p-p)}$ | > | 3 | V |
| Chrominance input signal (including burst) peak-to-peak value | R-Y | $V_{6-4(p-p)}$ | | 500 | mV |
| | B-Y | $V_{5-4(p-p)}$ | | 350 | mV |
| Impedance of colour difference signal outputs | | | typ. | 250 | Ω |

**PACKAGE OUTLINES**

TDA2522 : 16-lead DIL ; plastic (SOT-38).
TDA2522Q: 16-lead QIL ; plastic (SOT-58).

## BLOCK DIAGRAM


chrominance input (B-Y)
chrominance input (R-Y)
burst gating and blanking pulse
5
6
15
12
14
16
13
7
8
9
10
4
11
1
2
3
FLIP-FLOP
H/2
ident
H/2 DETECTOR/ A.C.C. AMPLIFIER
KILLER DETECTOR
current sampling
H/2
blanking
blanking
killer
PHASE DETECTOR/ BURST GATE
d.c.
(B-Y) DEMODULATOR
(R-Y) DEMODULATOR
PAL SWITCH
OSCILLATOR (8,8MHz)
8,8MHz ÷ 2 / 90° PHASE SHIFT
V ref (R-Y)
V ref (B-Y)
E
E
E
E
E
(G-Y) MATRIX
E = EMITTER FOLLOWER
TDA2522
-(B-Y)
-(G-Y)
-(R-Y)
colour unkill delay
+
Cd
a.c.c.
+
7Z70318.3

**RATINGS** Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | | |
|---|---|---|---|---|
| Supply voltage | $V_{11-4}$ | max. | 14 | V |
| Total power dissipation | $P_{tot}$ | max. | 600 | mW |
| Storage temperature | $T_{stg}$ | | −20 to +125 | °C |
| Operating ambient temperature | $T_{amb}$ | | −20 to +60 | °C |

**CHARACTERISTICS** at $V_{11-4} = 12$ V; $T_{amb} = 25$ °C

**Demodulator part**

| | | | | | | |
|---|---|---|---|---|---|---|
| Ratio of demodulated signals | B-Y/R-Y : | $\frac{V_{1-4}}{V_{3-4}}$ | typ. | 1,78 | | |
| | G-Y/R-Y : | $\frac{V_{2-4}}{V_{3-4}}$ | typ. | 0,85 | | 1) |
| | G-Y/R-Y : | $\frac{V_{2-4}}{V_{3-4}}$ | typ. | 0,17 | | 2) |
| Colour difference output signals peak-to-peak values: for the following input signals | −(R-Y) | $V_{3-4(p-p)}$ | > | 2,4 | V | |
| | −(G-Y) | $V_{2-4(p-p)}$ | > | 1,35 | V | |
| | −(B-Y) | $V_{1-4(p-p)}$ | > | 3 | V | |
| Chrominance input signal (including burst) peak-to-peak value; note 3 | R-Y | $V_{6-4(p-p)}$ | | 500 | mV | |
| | B-Y | $V_{5-4(p-p)}$ | | 350 | mV | |
| Impedance of colour difference signal outputs | | $\lvert Z_{3-4}\rvert$ | typ. | 250 | Ω | |
| | | $\lvert Z_{2-4}\rvert$ | typ. | 250 | Ω | |
| | | $\lvert Z_{1-4}\rvert$ | typ. | 250 | Ω | |
| H/2 ripple at R-Y output (peak-to-peak value) | | | < | 10 | mV | |
| Blanking and keying pulse burst keying: active for | | $V_{15-4}$ | > | 7,5 | V | |
| inactive for | | $V_{15-4}$ | < | 6,5 | V | |
| blanking: active for | | $V_{15-4}$ | > | 2 | V | |
| inactive for | | $V_{15-4}$ | < | 1 | V | |

---

1) The demodulators are driven by a chrominance signal of equal amplitude for the (R-Y) and the (B-Y) components. The phase of the (R-Y) chrominance signal equals the phase of the (R-Y) reference signal.
The same holds for the (B-Y) signals.

2) As under note 1, but the phase of the (R-Y) reference signal reversed.

3) Colour bar with 75% saturation.

**CHARACTERISTICS** (continued)

**Reference part**

| | | | | | |
|---|---|---|---|---|---|
| Phase difference between reference and burst signals for ±400 Hz deviation of crystal frequency | | < | ±5° | | |
| Overall holding range with typical crystal | Δf | typ. | ±500 | Hz | |
| Burst signal input at keying pulse width of 4 μs (peak-to-peak value) | $V_{5-6(p-p)}$ | typ. | 0,25 | V | 1) |
| Oscillator input resistance | $R_{10-4}$ | typ. | 270 | Ω | |
| Oscillator input capacitance | $C_{10-4}$ | typ. | note 2 | pF | |
| Oscillator output resistance | $R_{9-4}$ | typ. | 200 | Ω | |
| A.C.C. reference voltage | $V_{12-4}$ | typ. | 7 | V | |
| A.C.C. voltage at 0,25 V peak-to-peak burst at correct phase: | $V_{14-4}$ | typ. | 5,5 | V | |
| with zero burst: | $V_{14-4}$ | typ. | 7,0 | V | |
| A.C.C. amplifier output voltage range at $\pm I_{13} < 200\ \mu A$ | $V_{13-4}$ | | 0,5 to 5 | V | |

**Colour killer**

| | | | | | |
|---|---|---|---|---|---|
| Via pin 14 | | | | | |
| Colour off | $V_{14-4}$ | > | 6 | V | |
| Colour on | $V_{14-4}$ | < | 5,6 | V | |
| Alternatively via pin 16 | | | | | |
| Colour off | $V_{16-4}$ | > | 7 | V | |
| Colour on | $V_{16-4}$ | < | 5 | V | |
| Colour unkill delay | $t_d$ | typ. | 20 | ms/μF | 3) |

---

1) The amplitude of the burst is kept constant by a.c.c. action, but depends linearly on the keying pulse width.

2) To be established.

3) The delay depends on the value of $C_d$.

# COLOUR DEMODULATOR COMBINATION

The TDA2523 is an integrated synchronous demodulator combination for colour television receivers incorporating the following functions :

- 8, 8 MHz oscillator followed by a divider giving two 4, 4 MHz signals used as reference signals
- keyed burst phase detector for optimum noise behaviour
- a.c.c. detector and amplifier
- a colour killer
- two synchronous demodulators for the (B-Y) and (R-Y) signals
- temperature compensated emitter follower outputs
- PAL switch and PAL flip-flop with internal identification
- integrated capacitors in the symmetrical demodulators reduce unwanted carrier signals at the outputs

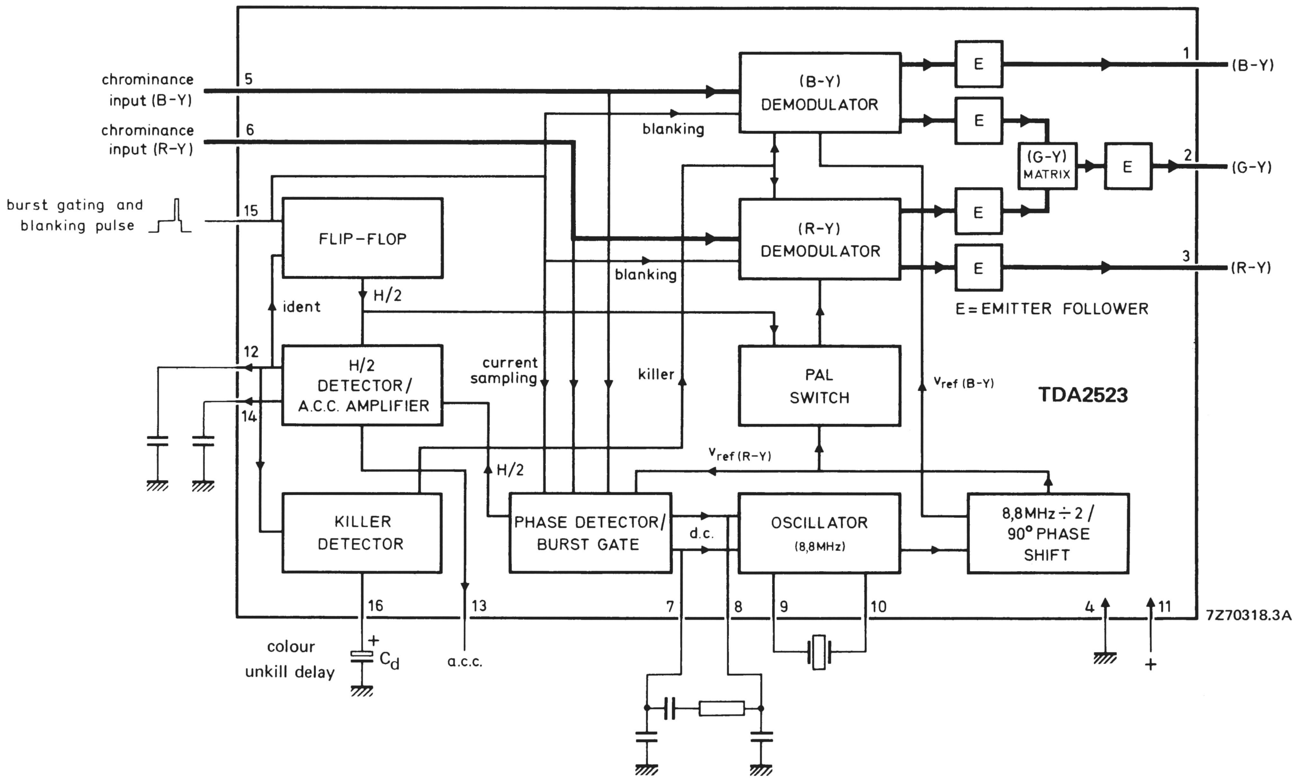
**QUICK REFERENCE DATA**

| | | | | | |
|---|---|---|---|---|---|
| Supply voltage | | $V_{11-4}$ | typ. | 12 | V |
| Supply current | | $I_{11}$ | typ. | 40 | mA |
| Colour difference output signals peak-to-peak values; for the following input signals | (R-Y) | $V_{3-4(p-p)}$ | > | 2, 4 | V |
| | (G-Y) | $V_{2-4(p-p)}$ | > | 1, 35 | V |
| | (B-Y) | $V_{1-4(p-p)}$ | > | 3 | V |
| Chrominance input signal (including burst) peak-to-peak value | R-Y | $V_{6-4(p-p)}$ | | 500 | mV |
| | B-Y | $V_{5-4(p-p)}$ | | 350 | mV |
| Impedance of colour difference signal outputs | | | typ. | 250 | Ω |

**PACKAGE OUTLINES**

TDA2523 : 16-lead DIL ; plastic (SOT-38).
TDA2523Q: 16-lead QIL ; plastic (SOT-58).

## BLOCK DIAGRAM


chrominance input (B-Y)
chrominance input (R-Y)
burst gating and blanking pulse
5
6
15
12
14
16
13
7
8
9
10
4
11
1
2
3
(B-Y)
(G-Y)
(R-Y)
(B-Y) DEMODULATOR
(R-Y) DEMODULATOR
E
E
E
E
E
(G-Y) MATRIX
E = EMITTER FOLLOWER
blanking
blanking
FLIP-FLOP
H/2
ident
H/2 DETECTOR/ A.C.C. AMPLIFIER
current sampling
killer
PAL SWITCH
$V_{ref\,(B-Y)}$
TDA2523
$V_{ref\,(R-Y)}$
H/2
KILLER DETECTOR
PHASE DETECTOR/ BURST GATE
d.c.
OSCILLATOR (8,8MHz)
8,8MHz ÷ 2 / 90° PHASE SHIFT
colour unkill delay
+
$C_d$
a.c.c.
+
7Z70318.3A

**RATINGS** Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | | |
|---|---|---|---|---|
| Supply voltage | $V_{11-4}$ | max. | 14 | V |
| Total power dissipation | $P_{tot}$ | max. | 600 | mW |
| Storage temperature | $T_{stg}$ | | −20 to +125 | °C |
| Operating ambient temperature | $T_{amb}$ | | −20 to +60 | °C |

**CHARACTERISTICS** at $V_{11-4} = 12$ V; $T_{amb} = 25$ °C

**Demodulator part**

| | | | | | | |
|---|---|---|---|---|---|---|
| Ratio of demodulated signals | B-Y/R-Y: | $\frac{V_{1-4}}{V_{3-4}}$ | typ. | 1,78 | | |
| | G-Y/R-Y: | $\frac{V_{2-4}}{V_{3-4}}$ | typ. | 0,85 | | 1) |
| | G-Y/R-Y: | $\frac{V_{2-4}}{V_{3-4}}$ | typ. | 0,17 | | 2) |
| Colour difference output signals peak-to-peak values; for the following input signals | (R-Y) | $V_{3-4(p-p)}$ | > | 2,4 | V | |
| | (G-Y) | $V_{2-4(p-p)}$ | > | 1,35 | V | |
| | (B-Y) | $V_{1-4(p-p)}$ | > | 3 | V | |
| Chrominance input signal (including burst) peak-to-peak value; note 3 | R-Y | $V_{6-4(p-p)}$ | | 500 | mV | |
| | B-Y | $V_{5-4(p-p)}$ | | 350 | mV | |
| Impedance of colour difference signal outputs | | $\lvert Z_{3-4}\rvert$ | typ. | 250 | Ω | |
| | | $\lvert Z_{2-4}\rvert$ | typ. | 250 | Ω | |
| | | $\lvert Z_{1-4}\rvert$ | typ. | 250 | Ω | |
| H/2 ripple at R-Y output (peak-to-peak value) | | | < | 10 | mV | |
| Blanking and keying pulse<br>burst keying: active for | | $V_{15-4}$ | > | 7,5 | V | |
| inactive for | | $V_{15-4}$ | < | 6,5 | V | |
| blanking: active for | | $V_{15-4}$ | > | 2 | V | |
| inactive for | | $V_{15-4}$ | < | 1 | V | |

---

1) The demodulators are driven by a chrominance signal of equal amplitude for the (R-Y) and the (B-Y) components. The phase of the (R-Y) chrominance signal equals the phase of the (R-Y) reference signal.
The same holds for the (B-Y) signals.

2) As under note 1, but the phase of the (R-Y) reference signal reversed.

3) Colour bar with 75% saturation.

## CHARACTERISTICS (continued)

### Reference part

| | | | | | |
|---|---|---|---|---|---|
| Phase difference between reference and burst signals for ±400 Hz deviation of crystal frequency | | < | $\pm 5^{\circ}$ | | |
| Overall holding range with typical crystal | $\Delta f$ | typ. | ±500 | Hz | |
| Burst signal input at keying pulse width of 4 µs (peak-to-peak value) | $V_{5-6(p-p)}$ | typ. | 0, 25 | V | 1) |
| Oscillator input resistance | $R_{10-4}$ | typ. | 270 | Ω | |
| Oscillator input capacitance | $C_{10-4}$ | typ. | note 2 | pF | |
| Oscillator output resistance | $R_{9-4}$ | typ. | 200 | Ω | |
| A.C.C. reference voltage | $V_{12-4}$ | typ. | 7 | V | |
| A.C.C. voltage at 0, 25 V peak-to-peak burst | | | | | |
| at correct phase: | $V_{14-4}$ | typ. | 5, 5 | V | |
| with zero burst: | $V_{14-4}$ | typ. | 7, 0 | V | |
| A.C.C. amplifier output voltage range at $\pm I_{13} < 200\ \mu A$ | $V_{13-4}$ | | 0, 5 to 5 | V | |

### Colour killer

| | | | | | |
|---|---|---|---|---|---|
| Via pin 14 | | | | | |
| Colour off | $V_{14-4}$ | > | 6 | V | |
| Colour on | $V_{14-4}$ | < | 5, 6 | V | |
| Alternatively via pin 16 | | | | | |
| Colour off | $V_{16-4}$ | > | 7 | V | |
| Colour on | $V_{16-4}$ | < | 5 | V | |
| Colour unkill delay | $t_d$ | typ. | 20 | ms/µF | 3) |

---

1) The amplitude of the burst is kept constant by a.c.c. action, but depends linearly on the keying pulse width.

2) To be established.

3) The delay depends on the value of $C_d$.

# COLOUR DEMODULATOR COMBINATION

The TDA2524 is an integrated synchronous demodulator combination for PAL colour television receivers incorporating the following functions:

- Two synchronous demodulators for the (B-Y) and (R-Y) signals.
- 8,8 MHz oscillator followed by a divider giving two 4,4 MHz signals used as reference signals.
- A colour killer and identification signal detector.
- A.C.C. detection by peak value rectification.
- Colour unkill delay.
- (G-Y) signal matrix.
- Integrated capacitors to reduce unwanted carrier signals at the outputs.
- PAL flip-flop and PAL switch.
- Flyback blanking in the synchronous demodulators.

## QUICK REFERENCE DATA

| | | | | |
|---|---|---|---|---|
| Supply voltage | $V_P = V_{11\text{-}4}$ | typ. | 12 | V |
| Supply current | $I_P = I_{11}$ | typ. | 42 | mA |
| Colour difference output signals; peak-to-peak values | | | | |
| (B-Y) signal | $V_{1\text{-}4(p\text{-}p)}$ | $<$ | 1,9 | V |
| (G-Y) signal | $V_{2\text{-}4(p\text{-}p)}$ | $<$ | 0,9 | V |
| (R-Y) signal | $V_{3\text{-}4(p\text{-}p)}$ | $<$ | 1,5 | V |
| Output impedance of colour difference signal outputs | $\lvert Z_{1,2,3\text{-}4} \rvert$ | typ. | 250 | Ω |

## PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).

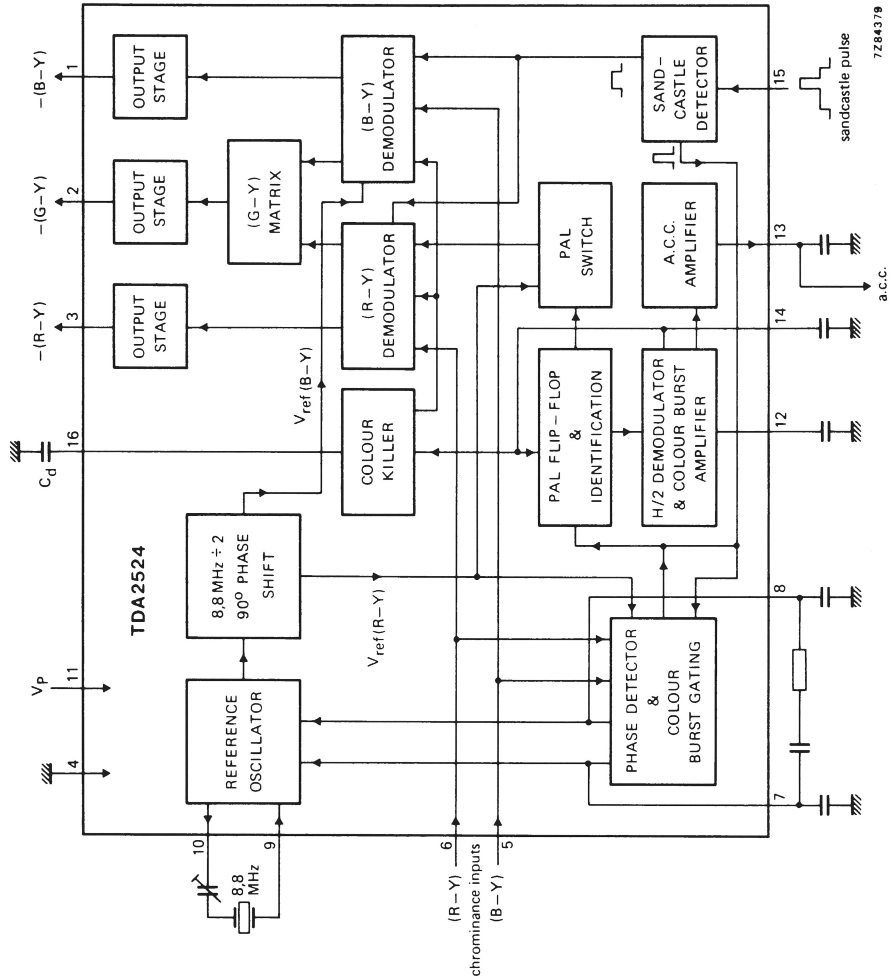

TDA2524
OUTPUT STAGE
OUTPUT STAGE
OUTPUT STAGE
(G−Y) MATRIX
(B−Y) DEMODULATOR
(R−Y) DEMODULATOR
COLOUR KILLER
8,8 MHz ÷ 2 90° PHASE SHIFT
REFERENCE OSCILLATOR
SAND-CASTLE DETECTOR
PAL SWITCH
A.C.C. AMPLIFIER
PAL FLIP−FLOP & IDENTIFICATION
H/2 DEMODULATOR & COLOUR BURST AMPLIFIER
PHASE DETECTOR & COLOUR BURST GATING
−(B−Y) 1
−(G−Y) 2
−(R−Y) 3
Cd 16
VP 11
4
Vref (B−Y)
Vref (R−Y)
10
9
8,8 MHz
6
5
(R−Y) chrominance inputs (B−Y)
15
sandcastle pulse
13
a.c.c.
14
12
8
7
7Z84379

Fig. 1 Block diagram.

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | | |
|---|---|---|---|---|
| Supply voltage | $V_P = V_{11\text{-}4}$ | max. | 14 | V |
| Voltages with respect to pin 4 | | | | |
| pins 1, 2, 3 | $V_{1,2,3\text{-}4}$ | max. | $V_P$ | V |
| pin 13 | $V_{13\text{-}4}$ | min. | 0 | V |
| pin 15 | $V_{15\text{-}4}$ | | 0 to $V_P$ | V |
| pin 16 | $V_{16\text{-}4}$ | | 0 to $V_P$ | V |
| Currents at: | | | | |
| pins 1, 2, 3 | $-I_{1,2,3}$ | max. | 5 | mA |
| pin 9 | $\pm I_9$ | max. | 2 | mA |
| pin 10 | $-I_{10}$ | max. | 5 | mA |
| pin 13 | $I_{13}$ | max. | 2 | mA |
| pin 14 | $\pm I_{14}$ | max. | 2 | mA |
| Total power dissipation | $P_{tot}$ | max. | 800 | mW |
| Storage temperature | $T_{stg}$ | | −20 to + 125 | °C |
| Operating ambient temperature | $T_{amb}$ | | −20 to + 70 | °C |

## CHARACTERISTICS

| | | | | |
|---|---|---|---|---|
| Supply voltage range | $V_P = V_{11\text{-}4}$ | | 10,8 to 13,2 | V |

The following characteristics are measured at $V_P = 12$ V; $T_{amb} = 25$ °C; unless otherwise specified

| | | | | |
|---|---|---|---|---|
| Supply current | $I_P = I_{11}$ | typ. | 42 | mA |

**Demodulator part**

| | | | | |
|---|---|---|---|---|
| Input resistance | $R_{5,6\text{-}4}$ | $>$ | 1 | kΩ |
| Input capacitance | $C_{5,6\text{-}4}$ | $<$ | 10 | pF |
| (R-Y) signal gain | $G_{(R\text{-}Y)}$ | typ. | 2,57 | |
| Ratio of demodulated signals at $V_{5\text{-}4} = V_{6\text{-}4}$ | $\dfrac{V_{(B\text{-}Y)}}{V_{(R\text{-}Y)}}$ | typ. | 1,78 | |

Matrix for the (G-Y) signal $V_{(G\text{-}Y)} = -0{,}51\,V_{(R\text{-}Y)} - 0{,}19\,V_{(B\text{-}Y)}$

**Colour difference outputs**

| | | | | |
|---|---|---|---|---|
| D.C. output voltage | $V_{1,2,3,4}$ | typ. | 5,6 | V |
| Peak-to-peak output voltages | | | | |
| (B-Y) signal | $V_{1\text{-}4(p\text{-}p)}$ | $<$ | 1,9 | V |
| (G-Y) signal | $V_{2\text{-}4(p\text{-}p)}$ | $<$ | 0,9 | V |
| (R-Y) signal | $V_{3\text{-}4(p\text{-}p)}$ | $<$ | 1,5 | V |
| Output impedance | $\lvert Z_{1,2,3\text{-}4}\rvert$ | typ. | 250 | Ω |
| Residual 4,4 MHz signal (peak-to-peak value) | $V_{1,2,3\text{-}4(p\text{-}p)}$ | $<$ | 30 | mV |
| H/2 ripple at (R-Y) output (peak-to-peak value) | $V_{3\text{-}4(p\text{-}p)}$ | $<$ | 10 | mV |
| Blanking level | $V_{15\text{-}4}$ | | 1 to 2 | V |

## CHARACTERISTICS (continued)

| | | | |
|---|---|---|---|
| **Reference oscillator** | | | |
| Input resistance | $R_{9\text{-}4}$ | typ. | 270 Ω |
| Output resistance | $R_{10\text{-}4}$ | typ. | 200 Ω |
| Gain | $G_{10\text{-}9}$ | > | 2,5 |
| Catching range; depends on RC-circuitry between pins 7 and 8; at R = 680 Ω and C = 15 μF | Δf | > | 500 Hz |
| Phase shift between the reference and burst signals at Δf = ± 400 Hz | $\varphi$ | typ. | ± 5° |
| **A.C.C. part** | | | |
| Reference voltage | $V_{12\text{-}4}$ | typ. | 7 V |
| Voltage with respect to pin 14 | | | |
| with colour burst signal $V_{5\text{-}6(p\text{-}p)} = 0{,}19$ V | $V_{12\text{-}14}$ | typ. | 1,5 V |
| without colour burst signal | $V_{12\text{-}14}$ | typ. | 0 V |
| Identification ON | $V_{14\text{-}12}$ | | 0,2 to 0,6 V |
| A.C.C. range dependent on $V_{14\text{-}4}$ | $V_{13\text{-}4}$ | | 0,5 to 3,0 V |
| Output current | $-I_{13}$ | | 15 to 50 μA |
| Colour burst keying at | $V_{15\text{-}4}$ | | 6,5 to 7,5 V |
| Colour killer voltages | | | |
| colour OFF at | $V_{12\text{-}14}$ | typ. | 0,5 V |
| or at | $V_{16\text{-}4}$ | > | 5,5 V |
| colour ON at | $V_{12\text{-}14}$ | typ. | 1,5 V |
| or at | $V_{16\text{-}4}$ | < | 4,0 V |
| Colour unkill delay; depends on $C_d$ (Fig. 1) | $t_d$ | typ. | 24 ms/μF |

# COLOUR DEMODULATOR COMBINATION

The TDA2525 is an integrated synchronous demodulator combination for PAL colour television receivers incorporating the following functions:

- Two synchronous demodulators for the (B-Y) and (R-Y) signals.
- 8,8 MHz oscillator followed by a divider giving two 4,4 MHz signals used as reference signals.
- A colour killer and identification signal detector.
- A.C.C. detection by peak value rectification.
- Colour unkill delay.
- (G-Y) signal matrix.
- Integrated capacitors to reduce unwanted carrier signals at the outputs.
- PAL flip-flop and PAL switch.
- Flyback blanking in the synchronous demodulators.

## QUICK REFERENCE DATA

| | | | | |
|---|---|---|---|---|
| Supply voltage | $V_P = V_{11\text{-}4}$ | typ. | 12 | V |
| Supply current | $I_P = I_{11}$ | typ. | 42 | mA |
| Colour difference output signals; peak-to-peak values | | | | |
| (B-Y) signal | $V_{1\text{-}4(p\text{-}p)}$ | < | 2,4 | V |
| (G-Y) signal | $V_{2\text{-}4(p\text{-}p)}$ | < | 1,35 | V |
| (R-Y) signal | $V_{3\text{-}4(p\text{-}p)}$ | < | 3,0 | V |
| Output impedance of colour difference signal outputs | $\lvert Z_{1,2,3\text{-}4}\rvert$ | typ. | 250 | Ω |

## PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).

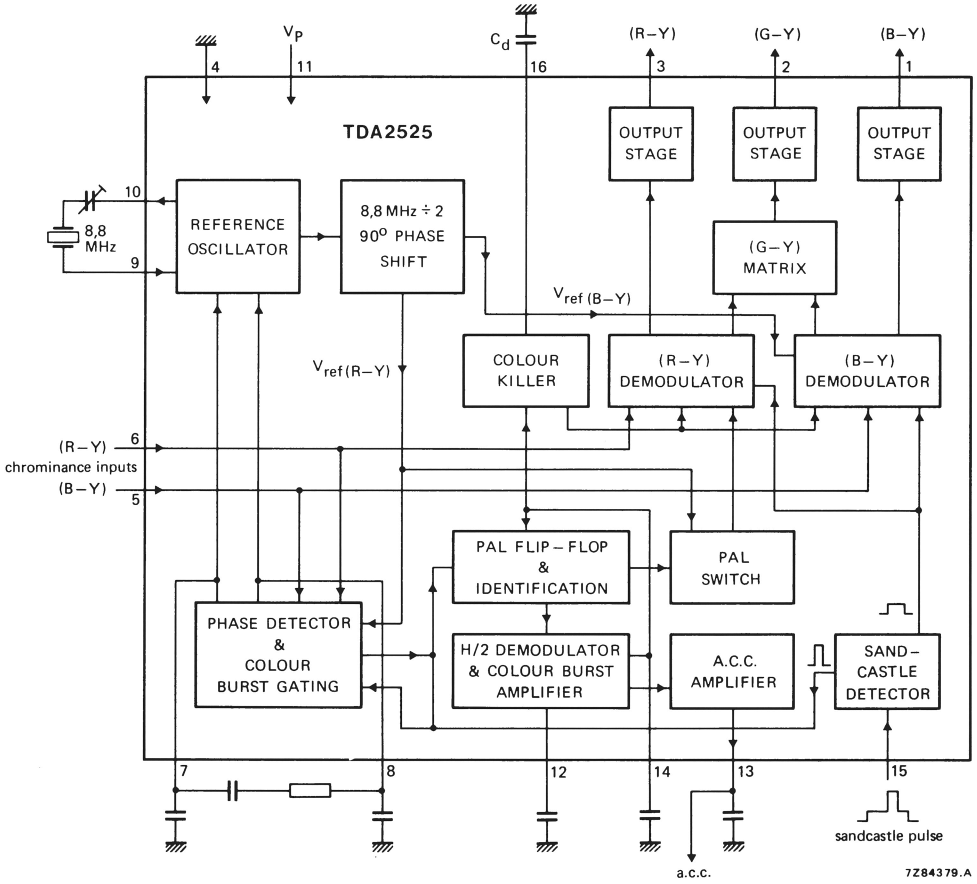

TDA2525
4
$V_P$
11
$C_d$
16
(R−Y)
3
(G−Y)
2
(B−Y)
1
OUTPUT STAGE
OUTPUT STAGE
OUTPUT STAGE
(G−Y) MATRIX
10
9
8,8 MHz
REFERENCE OSCILLATOR
8,8 MHz ÷ 2 90° PHASE SHIFT
$V_{ref\,(B-Y)}$
$V_{ref\,(R-Y)}$
COLOUR KILLER
(R−Y) DEMODULATOR
(B−Y) DEMODULATOR
(R−Y)
6
chrominance inputs
(B−Y)
5
PAL FLIP−FLOP & IDENTIFICATION
PAL SWITCH
PHASE DETECTOR & COLOUR BURST GATING
H/2 DEMODULATOR & COLOUR BURST AMPLIFIER
A.C.C. AMPLIFIER
SAND-CASTLE DETECTOR
7
8
12
14
13
15
a.c.c.
sandcastle pulse
7Z84379.A

Fig. 1 Block diagram.

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | | |
|---|---|---|---|---|
| Supply voltage | $V_P = V_{11\text{-}4}$ | max. | 14 | V |
| Voltages with respect to pin 4 | | | | |
| pins 1, 2, 3 | $V_{1,2,3\text{-}4}$ | max. | $V_P$ | V |
| pin 15 | $V_{15\text{-}4}$ | | 0 to $V_P$ | V |
| Currents at: | | | | |
| pins 1, 2, 3 | $-I_{1,2,3}$ | max. | 5 | mA |
| pin 9 | $\pm I_9$ | max. | 2 | mA |
| pin 10 | $-I_{10}$ | max. | 5 | mA |
| pin 13 | $I_{13}$ | max. | 2 | mA |
| pin 14 | $\pm I_{14}$ | max. | 2 | mA |
| Total power dissipation | $P_{tot}$ | max. | 800 | mW |
| Storage temperature | $T_{stg}$ | | −20 to + 125 | °C |
| Operating ambient temperature | $T_{amb}$ | | −20 to + 70 | °C |

## CHARACTERISTICS

| | | | | |
|---|---|---|---|---|
| Supply voltage range | $V_P = V_{11\text{-}4}$ | | 10,8 to 13,2 | V |

The following characteristics are measured at $V_P = 12$ V; $T_{amb} = 25$ °C; unless otherwise specified.

| | | | | |
|---|---|---|---|---|
| Supply current | $I_P = I_{11}$ | typ. | 42 | mA |

### Demodulator part

| | | | | |
|---|---|---|---|---|
| Input resistance | $R_{5,6\text{-}4}$ | > | 1 | kΩ |
| Input capacitance | $C_{5,6\text{-}4}$ | < | 10 | pF |
| (R-Y) signal gain | $G_{(R\text{-}Y)}$ | typ. | 4,5 | |
| Ratio of demodulated signals at $V_{5\text{-}4} = V_{6\text{-}4}$ | $\frac{V_{(B\text{-}Y)}}{V_{(R\text{-}Y)}}$ | typ. | 1,78 | |

Matrix for the (G-Y) signal $V_{(G\text{-}Y)} = -0{,}51\ V_{(R\text{-}Y)} - 0{,}19\ V_{(B\text{-}Y)}$

### Colour difference outputs

| | | | | |
|---|---|---|---|---|
| D.C. output voltage | $V_{1,2,3,4}$ | typ. | 5,6 | V |
| Peak-to-peak output voltages | | | | |
| (B-Y) signal | $V_{1\text{-}4(p\text{-}p)}$ | < | 2,4 | V |
| (G-Y) signal | $V_{2\text{-}4(p\text{-}p)}$ | < | 1,35 | V |
| (R-Y) signal | $V_{3\text{-}4(p\text{-}p)}$ | < | 3,0 | V |
| Output impedance | $\lvert Z_{1,2,3\text{-}4}\rvert$ | typ. | 250 | Ω |
| Residual 4,4 MHz signal (peak-to-peak value) | $V_{1,2,3\text{-}4(p\text{-}p)}$ | < | 50 | mV |
| H/2 ripple at (R-Y) output (peak-to-peak value) | $V_{3\text{-}4(p\text{-}p)}$ | < | 10 | mV |
| Blanking level | $V_{15\text{-}4}$ | | 1 to 2 | V |

## CHARACTERISTICS (continued)

### Reference oscillator

| | | | | |
|---|---|---|---|---|
| Input resistance | $R_{9\text{-}4}$ | typ. | 270 | Ω |
| Output resistance | $R_{10\text{-}4}$ | typ. | 200 | Ω |
| Gain | $G_{10\text{-}9}$ | $>$ | 2,5 | |
| Catching range; depends on RC-circuitry between pins 7 and 8; at R = 680 Ω and C = 15 μF | $\Delta f$ | $>$ | 500 | Hz |
| Phase shift between the reference and burst signals at $\Delta f = \pm 400$ Hz | $\varphi$ | typ. | $\pm 5^{\circ}$ | |

### A.C.C. part

| | | | | |
|---|---|---|---|---|
| Reference voltage | $V_{12\text{-}4}$ | typ. | 7 | V |
| Voltage with respect to pin 14 | | | | |
| with colour burst signal $V_{5\text{-}6(p\text{-}p)} = 0{,}225$ V | $-V_{12\text{-}14}$ | typ. | 1,5 | V |
| without colour burst signal | $V_{12\text{-}14}$ | typ. | 0 | V |
| Identification ON | $V_{14\text{-}12}$ | | 0,2 to 0,6 | V |
| A.C.C. range dependent on $V_{14\text{-}4}$ | $V_{13\text{-}4}$ | | 0,5 to 3,0 | V |
| Output current | $-I_{13}$ | | 15 to 50 | μA |
| Colour burst keying at | $V_{15\text{-}4}$ | | 6,5 to 7,5 | V |
| Colour killer voltages | | | | |
| colour OFF at | $V_{12\text{-}14}$ | typ. | 0,5 | V |
| or at | $V_{16\text{-}4}$ | $>$ | 6,0 | V |
| colour ON at | $V_{12\text{-}14}$ | typ. | 1,5 | V |
| or at | $V_{16\text{-}4}$ | $<$ | 4,0 | V |
| Colour unkill delay; depends on $C_d$ (Fig. 1) | $t_d$ | typ. | 24 | ms/μF |

# RGB MATRIX PREAMPLIFIER

The TDA2530 is an integrated RGB matrix preamplifier for colour television receivers, incorporating a matrix preamplifier for RGB cathode drive of the picture tube with clamping circuits. The three channels have the same layout to ensure identical frequency behaviour.

This integrated circuit has been designed to be driven from the TDA2522 synchronous demodulator and oscillator IC.

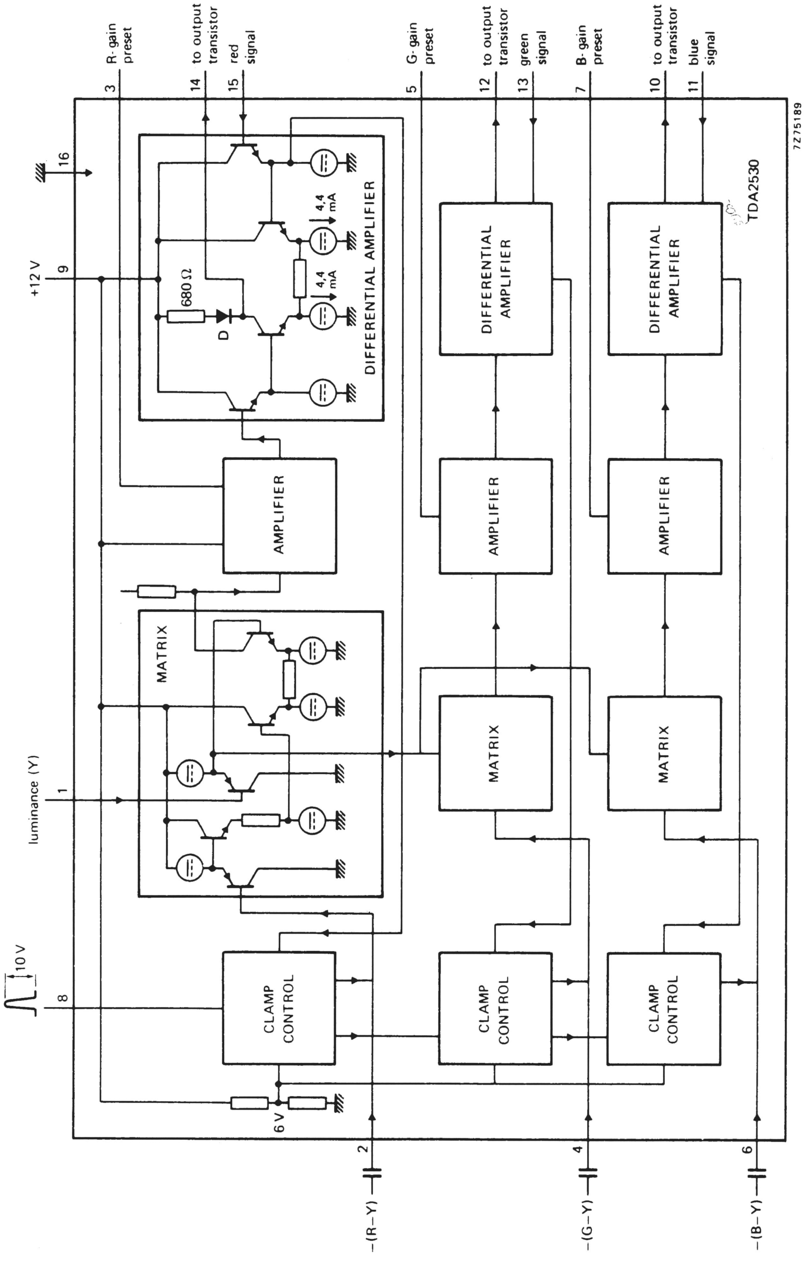
## QUICK REFERENCE DATA

| | | | |
|---|---|---|---|
| Supply voltage | $V_{9-16}$ | typ. | 12 V |
| Operating ambient temperature range | $T_{amb}$ | | −20 to +60 °C |
| Luminance input resistance | $R_{1-16}$ | > | 100 kΩ |
| Input current of colour difference inputs | $I_2, I_4, I_6$ | typ. | 2 µA |
| during clamping | $I_2, I_4, I_6$ | | −0,2 to +0,2 mA |
| Clamping pulse input current | $-I_8$ | < | 20 µA |
| Gain of RGB preamplifiers | G | typ. | 0 dB |
| Gain d.c. adjustment range | ΔG | typ. | ±3 dB |
| Gain of error amplifier (conductance) | | typ. | 20 mA/V |
| Input current of feedback inputs | $I_{11}, I_{13}, I_{15}$ | typ. | 2 µA |
| Output current swing | $I_{10}, I_{12}, I_{14}$ | | −4,4 to +4,4 mA |

**PACKAGE OUTLINES**

TDA2530 : 16-lead DIL; plastic (SOT-38).
TDA2530Q : 16-lead QIL; plastic (SOT-58).

## BLOCK DIAGRAM


R-gain preset
to output transistor
red signal
G-gain preset
to output transistor
green signal
B-gain preset
to output transistor
blue signal
3
14
15
5
12
13
7
10
11
16
9
+12 V
1
luminance (Y)
8
10 V
7Z75189
TDA2530
680 Ω
D
4,4 mA
4,4 mA
DIFFERENTIAL AMPLIFIER
DIFFERENTIAL AMPLIFIER
DIFFERENTIAL AMPLIFIER
AMPLIFIER
AMPLIFIER
AMPLIFIER
MATRIX
MATRIX
MATRIX
CLAMP CONTROL
CLAMP CONTROL
CLAMP CONTROL
6 V
2
4
6
−(R−Y)
−(G−Y)
−(B−Y)

**RATINGS** Limiting values in accordance with the Absolute Maximum System (IEC134)

Voltages

| | | | |
|---|---|---|---|
| Supply voltage (pin 9) | $V_P$ ($V_{9-16}$) | max. | 15 V |
| Pin 1 | $V_{1-16}$ | | 0 to $V_P$ |
| Pins 3, 5 and 7 | $V_{3;5;7-16}$ | | 0 to $V_P$ |
| Pins 2, 4 and 6 | $V_{2;4;6-16}$ | | 0 to $V_P$ |
| Pin 8 | $V_{8-16}$ | max. | $V_P$ |
| Pin 10 | $V_{10-16}$ | | $V_{11-16}$ to $V_P + 3$ V |
| Pin 12 | $V_{12-16}$ | | $V_{13-16}$ to $V_P + 3$ V |
| Pin 14 | $V_{14-16}$ | | $V_{15-16}$ to $V_P + 3$ V |
| Pins 11, 13 and 15 | $V_{11;13;15-16}$ | | 0, 3 $V_P$ to $V_P$ |

Current

| | | | |
|---|---|---|---|
| Pin 8 | $-I_8$ | max. | 1 mA |

Power dissipation

| | | | |
|---|---|---|---|
| Total power dissipation | $P_{tot}$ | max. | 1 W |

Temperatures

| | | | |
|---|---|---|---|
| Storage temperature | $T_{stg}$ | | −20 to +125 °C |
| Operating ambient temperature | $T_{amb}$ | | −20 to +60 °C |

**CHARACTERISTICS** at $V_P = 12$ V; $V_{1-16} = 1,5$ V; $T_{amb} = 25$ °C; measured in circuit on page 5.

| | | | |
|---|---|---|---|
| Current consumption | $I_9$ | typ. | 50 mA |
| **Luminance input** | | | |
| Black level | $V_{1-16}$ | typ. | 1, 5 V |
| Black-to-white input voltage (peak-to-peak value) | $V_{1-16(p-p)}$ | typ. | 1, 0 V |
| Input resistance | $R_{1-16}$ | > | 100 kΩ |
| **Colour difference input** | | | |
| Input signals (peak-to-peak values) R-Y 1) | $V_{2-16(p-p)}$ | typ. | 1, 4 V |
| G-Y 1) | $V_{4-16(p-p)}$ | typ. | 0, 82 V |
| B-Y 1) | $V_{6-16(p-p)}$ | typ. | 1, 78 V |
| Input currents (source resistance 300 Ω max.) | $I_2, I_4, I_6$ | typ.<br>< | 2 μA<br>4 μA |
| Input currents during clamping | $I_2, I_4, I_6$ | | −0, 2 to +0, 2 mA |

---

1) This prescribed order is not mandatory, as all three channels are identical.

## CHARACTERISTICS (continued)

### Clamp pulse input for d.c. feedback

| | | | | | |
|---|---|---|---|---|---|
| Input voltage for clamping: on level | $V_{8-16}$ | | 6, 5 to 12 | V | |
| off level | $V_{8-16}$ | | 0 to 5, 5 | V | 1) |
| Input current for clamping: on level | $I_8$ | < | 1 | µA | |
| off level | $-I_8$ | < | 20 | µA | |

### Feedback input

| | | | | | |
|---|---|---|---|---|---|
| D.C. level during clamping | $V_{11;13;15-16}$ | typ. | 0, 5 $V_P$ | | |

### Gain adjustment for colour drive

| | | | | | |
|---|---|---|---|---|---|
| Adjustment voltage range | $V_{3;5;7-16}$ | | 0 to 10 | V | |
| Adjustment voltage for nominal gain | $V_{3;5;7-16}$ | typ. | 5 | V | |
| Nominal gain between colour difference inputs, luminance input and colour feedback inputs (pins 11, 13 and 15) | G | typ. | 0 | dB | 2) |
| Adjustment range of nominal gain at $\Delta V_{3;5;7-16} = \pm 5$ V | $\Delta G$ | > | ±3 | dB | |

### Differential amplifier

| | | | | | |
|---|---|---|---|---|---|
| Input current of feedback inputs | $I_{11}, I_{13}, I_{15}$ | typ. | 2 | µA | |
| Gain of error amplifier (conductance) | | typ. | 20 | mA/V | |
| Output current swing | $I_{10}, I_{12}, I_{14}$ | | −4, 4 to +4, 4 | mA | |
| Integrated load resistance | $R_{10;12;14-9}$ | typ. | 680 | Ω | 3) |
| Output bias voltage (see application information) | $V_{10;12;14-16}$ | typ. | 8 | V | 3) |

## APPLICATION INFORMATION (see circuit on page 5)

Clamping level ($V_{cl}$) of video output stages, with set clamping level potentiometers in their mid-positions:

$$V_{cl} = V_P \left(1 + \frac{R1}{R2} - \frac{R1}{R3}\right)$$

Gain of video output stages: $G = 1 + \frac{R1}{R2} + \frac{R1}{R3} + \frac{R1}{R4}$

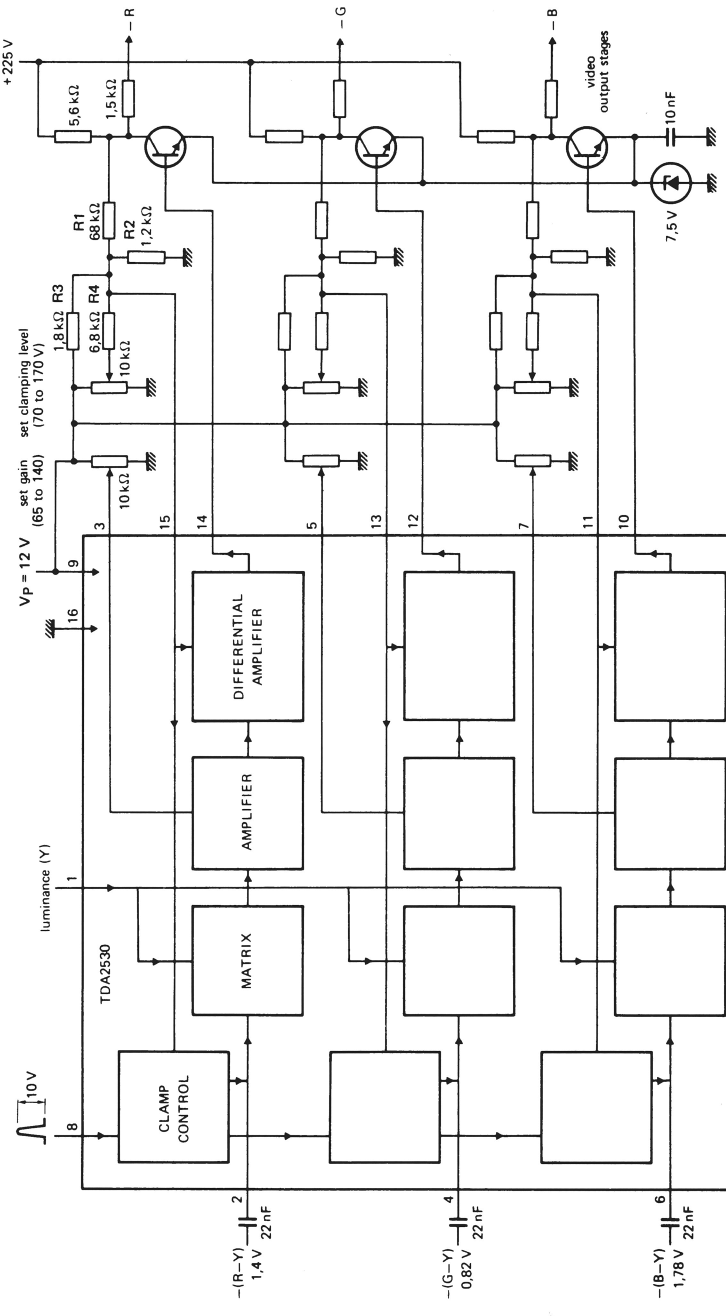
---

1) Switching from clamping on to off occurs at about 6 V.

2) Error signal is assumed to be negligible.

3) The fact that the load resistors have series diodes (D; see block diagram on page 2), means that the resistors can be ignored when $V_{10;12;14} \geq V_P$.
In that case, external load resistors must be chosen such that the nominal current will be 4, 4 mA.

## APPLICATION INFORMATION


+225 V
5,6 kΩ
1,5 kΩ
−R
−G
−B
video output stages
10 nF
7,5 V
R1 68 kΩ
R2 1,2 kΩ
R3 1,8 kΩ
R4 6,8 kΩ
10 kΩ
set clamping level (70 to 170 V)
set gain (65 to 140)
10 kΩ
$V_P$ = 12 V
9
16
3
15
14
5
13
12
7
11
10
7Z75190
DIFFERENTIAL AMPLIFIER
AMPLIFIER
MATRIX
CLAMP CONTROL
TDA2530
luminance (Y)
1
8
10 V
−(R−Y) 1,4 V
2
22 nF
−(G−Y) 0,82 V
4
22 nF
−(B−Y) 1,78 V
6
22 nF

# RGB MATRIX PREAMPLIFIER

The TDA2532 is an integrated matrix preamplifier for use in conjunction with discrete video amplifiers to provide RGB drive to the cathodes of a colour television picture tube. The integrated circuit incorporates:

- matrix circuits;
- gain control stages, operated by d.c. setting;
- preamplifiers with feedback and integral black-level clamps;
- facilities for video blanking during data display.

The three channels have the same layout to ensure identical frequency behaviour. The integrated circuit has been designed to be driven by the integrated colour demodulator combination type TDA2522.

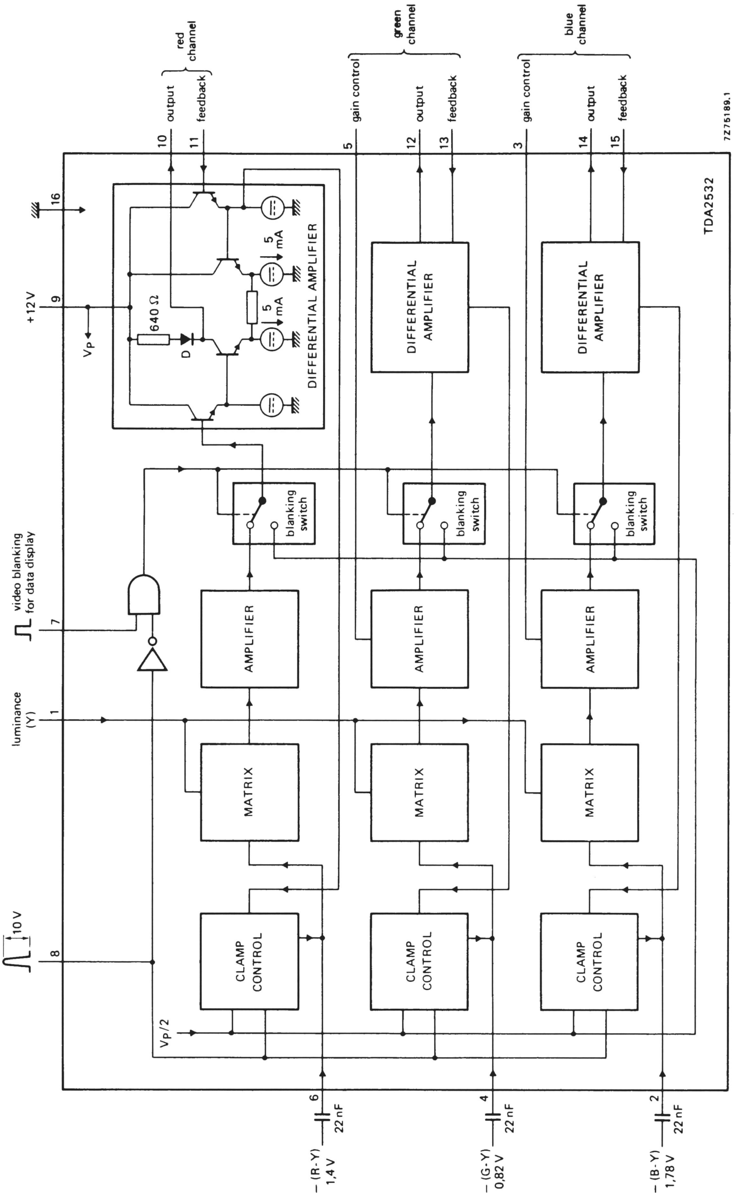
## QUICK REFERENCE DATA

| | | | | |
|---|---|---|---|---|
| Supply voltage | $V_{9\text{-}16}$ | typ. | 12 | V |
| Operating ambient temperature range | $T_{amb}$ | | −25 to + 60 | °C |
| Luminance input resistance | $R_{1\text{-}16}$ | > | 100 | kΩ |
| Input current of colour difference inputs | $I_2, I_4, I_6$ | typ. | 1 | μA |
| Clamping pulse input current | $-I_8$ | < | 60 | μA |
| Gain of RGB preamplifiers | G | typ. | 0 | dB |
| Gain d.c. adjustment range | ΔG | > | ± 40 | % |
| Gain of error amplifier (transconductance) | | typ. | 20 | mA/V |
| Output current swing | $I_{10}, I_{12}, I_{14}$ | typ. | ± 3,5 | mA |

## PACKAGE OUTLINES

TDA2532: 16-lead DIL; plastic (SOT-38).
TDA2532Q: 16-lead QIL; plastic (SOT-58).

## BLOCK DIAGRAM


red channel
output
feedback
10
11
green channel
gain control
output
feedback
5
12
13
blue channel
gain control
output
feedback
3
14
15
7Z75189.1
TDA2532
16
+12 V
9
$V_P$
640 Ω
D
5 mA
5 mA
DIFFERENTIAL AMPLIFIER
DIFFERENTIAL AMPLIFIER
DIFFERENTIAL AMPLIFIER
blanking switch
blanking switch
blanking switch
video blanking for data display
7
AMPLIFIER
AMPLIFIER
AMPLIFIER
luminance (Y)
1
MATRIX
MATRIX
MATRIX
10 V
8
CLAMP CONTROL
CLAMP CONTROL
CLAMP CONTROL
$V_P/2$
6
22 nF
– (R-Y) 1,4 V
4
22 nF
– (G-Y) 0,82 V
2
22 nF
– (B-Y) 1,78 V

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | |
|---|---|---|---|
| Supply voltage (pin 9) | $V_P$ ($V_{9\text{-}16}$) | max. | 13,2 V |
| Pin 1 | $V_{1\text{-}16}$ | | 0 to $V_P$ |
| Pins 3, 5 | $V_{3;\,5\text{-}16}$ | | 0 to $V_P$ |
| Pins 2, 4 and 6 | $V_{2;\,4;\,6\text{-}16}$ | | 0 to $V_P$ |
| Pin 7 | $V_{7\text{-}16}$ | | −0,5 V to $V_P$ |
| Pin 8 | $V_{8\text{-}16}$ | max. | $V_P$ |
| Pin 10 | $V_{10\text{-}16}$ | | $V_{11\text{-}16}$ to $V_P + 3$ V |
| Pin 12 | $V_{12\text{-}16}$ | | $V_{13\text{-}16}$ to $V_P + 3$ V |
| Pin 14 | $V_{14\text{-}16}$ | | $V_{15\text{-}16}$ to $V_P + 3$ V |
| Pins 11, 13 and 15 | $V_{11;\,13;\,15\text{-}16}$ | | 0,3 $V_P$ to $V_P$ |
| Pin 8 | $-I_8$ | max. | 1 mA |
| Total power dissipation | $P_{tot}$ | max. | 1,1 W |
| Storage temperature | $T_{stg}$ | | −25 to + 125 °C |
| Operating ambient temperature | $T_{amb}$ | | −25 to + 60 °C |

## CHARACTERISTICS

**At $V_P = 12$ V; $V_{1\text{-}16} = 1{,}5$ V; $T_{amb} = 25$ °C; measured in circuit on page 6.**

| | | | |
|---|---|---|---|
| Current consumption | $I_9$ | typ. | 60 mA |

**Luminance input**

| | | | |
|---|---|---|---|
| Black level | $V_{1\text{-}16}$ | typ. | 1,5 V |
| Black-to-white input voltage (peak-to-peak value) | $V_{1\text{-}16\,(p\text{-}p)}$ | typ. | 1,0 V |
| Input resistance | $R_{1\text{-}16}$ | > | 100 kΩ |

**Colour difference input**

| | | | | |
|---|---|---|---|---|
| Input signals (peak-to-peak values)<br>for 100% saturated colour bars | R-Y | $V_{6\text{-}16\,(p\text{-}p)}$ | typ. | 1,4 V |
| | G-Y | $V_{4\text{-}16\,(p\text{-}p)}$ | typ. | 0,82 V |
| | B-Y | $V_{2\text{-}16\,(p\text{-}p)}$ | typ. | 1,78 V |
| Input currents (source resistance 300 Ω max.) | | $I_2, I_4, I_6$ | typ. | 1 µA |
| | | | < | 3 µA |

## CHARACTERISTICS (continued)

| | | | | |
|---|---|---|---|---|
| **Clamp pulse input** | | | | |
| Input voltage for clamping | | | | |
| on level | $V_{8\text{-}16}$ | | 7,5 to 12 | V |
| off level | $V_{8\text{-}16}$ | | 0 to 6,5 | V* |
| Input voltage to enable video blanking input | $V_{8\text{-}16}$ | < | 1 | V |
| Input voltage to disable video blanking input | $V_{8\text{-}16}$ | | 2 to 12 | V |
| Input current for clamping | | | | |
| on level | $I_8$ | < | 1 | μA |
| off level | $-I_8$ | < | 60 | μA |
| Clamp pulse duration | $t_{clamp}$ | > | 3,5 | μs |
| **Video blanking input** | | | | |
| Input voltage for blanking | | | | |
| on level | $V_{7\text{-}16}$ | > | 1,5 | V |
| off level | $V_{7\text{-}16}$ | < | 0,5 | V |
| **Feedback input** | | | | |
| D.C. level during clamping | $V_{11;\,13;\,15\text{-}16}$ | | 6 to 6,2 | V |
| **Gain adjustment for colour drive** | | | | |
| Adjustment voltage range | $V_{3;\,5\text{-}16}$ | | 0 to 10 | V |
| Adjustment voltage for nominal gain | $V_{3;\,5\text{-}16}$ | typ. | 5 | V |
| Nominal gain between colour difference inputs, luminance input and colour feedback inputs (pins 11, 13 and 15) | G | typ. | 0 | dB** |
| Adjustment range of nominal gain at $\Delta V_{3;\,5\text{-}16} = \pm 5$ V | ΔG | > | ± 40 | % |
| **Differential amplifier** | | | | |
| Gain of error amplifier (transconductance) | | typ. | 20 | mA/V |
| Output current swing | $I_{10}, I_{12}, I_{14}$ | ⩾ | ± 3,5 | mA |
| Integrated load resistance | $R_{10;\,12;\,14\text{-}9}$ | typ. | 640 | Ω▲ |
| Output bias voltage (see application information) | $V_{10;\,12;\,14\text{-}16}$ | typ. | 8 | V▲ |

---

* Switching from clamping on to off occurs at about 7 V.

** Error signal is assumed to be negligible.

▲ The fact that the load resistors have series diodes (D; see block diagram on page 2), means that the resistors can be ignored when $V_{10;\,12;\,14} \geqslant V_P$. In that case, external load resistors must be chosen such that the nominal current will be 3,5 mA.

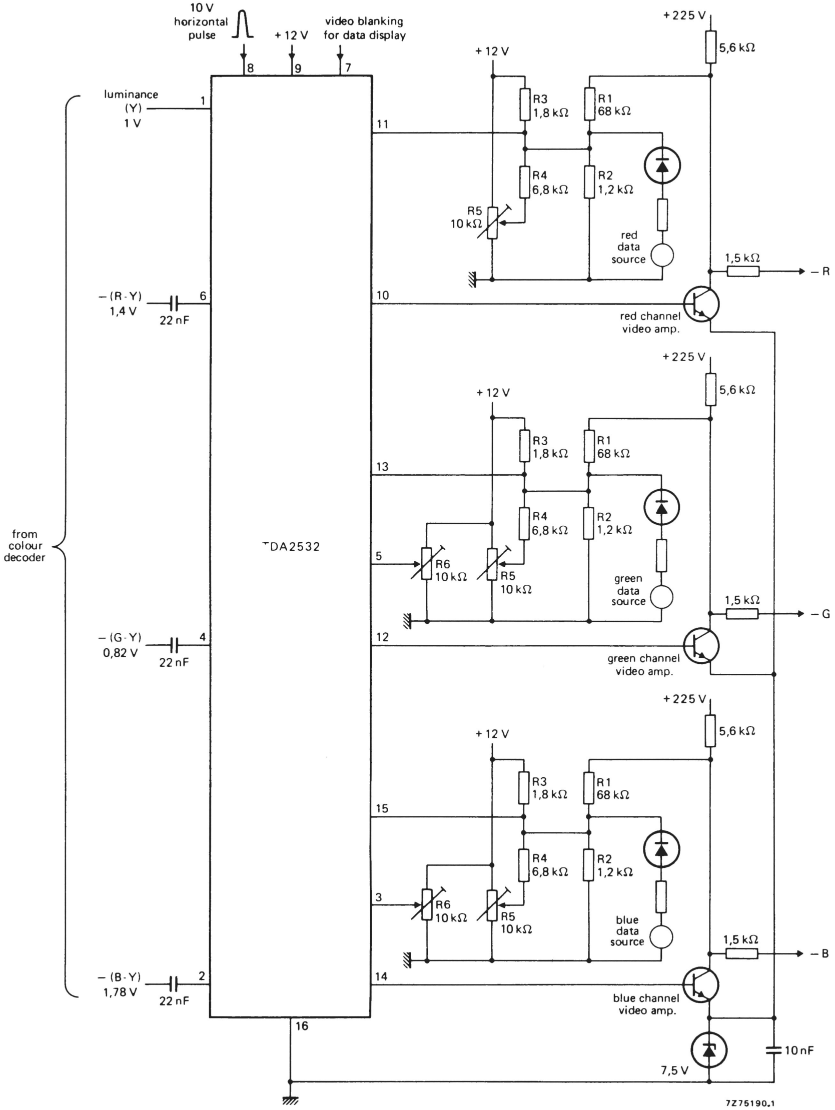
## APPLICATION INFORMATION (see circuit on page 6)

Clamping level ($V_{cl}$) of video output stages, with set clamping level potentiometers in their mid-positions:

$$V_{cl} = 0{,}5\ V_P \left(1 + \frac{R1}{R2} - \frac{R1}{R3}\right).$$

Gain of video output stages: $G = 1 + \frac{R1}{R2} + \frac{R1}{R3} + \frac{R1}{R4 + 0{,}25\ R5}$.

## APPLICATION INFORMATION


10 V
horizontal
pulse
+ 12 V
video blanking
for data display
8
9
7
luminance
(Y)
1 V
1
−(R-Y)
1,4 V
22 nF
6
from
colour
decoder
TDA2532
−(G-Y)
0,82 V
22 nF
4
−(B-Y)
1,78 V
22 nF
2
16
11
10
13
5
12
15
3
14
+12 V
R3
1,8 kΩ
R1
68 kΩ
R4
6,8 kΩ
R2
1,2 kΩ
R5
10 kΩ
R6
10 kΩ
red
data
source
green
data
source
blue
data
source
+225 V
5,6 kΩ
1,5 kΩ
−R
−G
−B
red channel
video amp.
green channel
video amp.
blue channel
video amp.
7,5 V
10 nF
7Z75190.1

R5 = clamping level adjustment (70 V to 170 V); R6 = gain adjustment (65 to 140).

# TELEVISION I.F. AMPLIFIER AND DEMODULATOR

The TDA2540 is an i.f. amplifier and demodulator circuit for colour and black and white television receivers using n-p-n tuners.
It incorporates the following functions:

- gain-controlled wide-band amplifier, providing complete i.f. gain
- synchronous demodulator
- white spot inverter
- video preamplifier with noise protection
- a.f.c. circuit which can be switched on/off by a d.c. level, e.g. during tuning
- a.g.c. circuit with noise gating
- tuner a.g.c. output (n-p-n tuners)
- VCR switch, which switches off the video output; e.g. for insertion of a VCR playback signal

## QUICK REFERENCE DATA

| | | | | |
|---|---|---|---|---|
| Supply voltage | $V_{11\text{-}13}$ | typ. | 12 | V |
| Supply current | $I_{11}$ | typ. | 50 | mA |
| I.F. input voltage at f = 38,9 MHz (r.m.s. value) | $V_{1\text{-}16\,(rms)}$ | typ. | 100 | $\mu$V |
| Video output voltage (white at 10% of top sync) | $V_{12(p\text{-}p)}$ | typ. | 2,7 | V |
| I.F. voltage gain control range | $G_v$ | typ. | 64 | dB |
| Signal-to-noise ratio at $V_i$ = 10 mV | S/N | typ. | 58 | dB |
| A.F.C. output voltage swing for $\Delta f$ = 100 kHz | $\Delta V_{5\text{-}13}$ | typ. | 10 | V |

## PACKAGE OUTLINES

TDA2540 : 16-lead DIL; plastic (SOT-38).
TDA2540Q: 16-lead QIL; plastic (SOT-58).

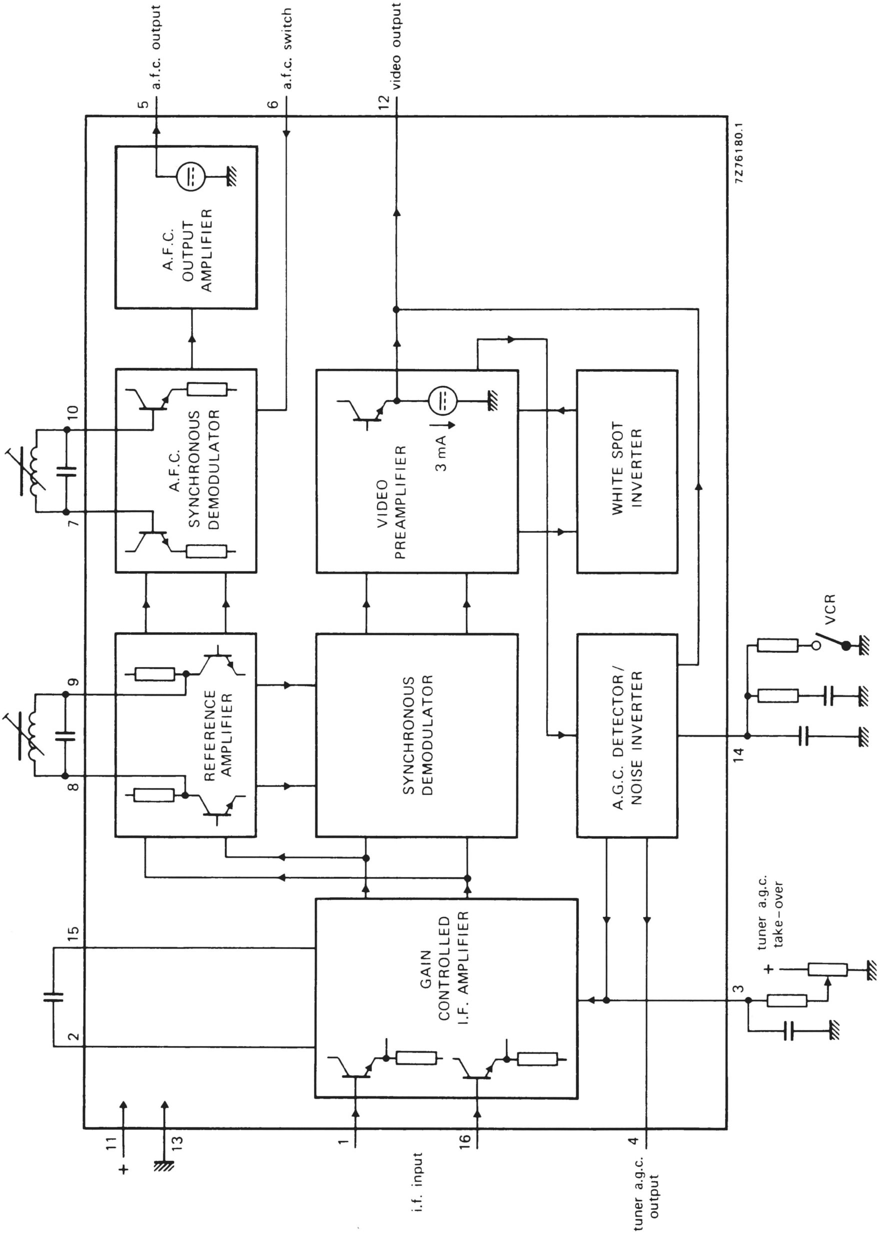

5 a.f.c. output
6 a.f.c. switch
12 video output
7Z76180.1
A.F.C. OUTPUT AMPLIFIER
A.F.C. SYNCHRONOUS DEMODULATOR
VIDEO PREAMPLIFIER
3 mA
WHITE SPOT INVERTER
10
7
9
8
REFERENCE AMPLIFIER
SYNCHRONOUS DEMODULATOR
A.G.C. DETECTOR / NOISE INVERTER
VCR
14
15
2
GAIN CONTROLLED I.F. AMPLIFIER
3
tuner a.g.c. take-over
+
11
+
13
1
16
i.f. input
4
tuner a.g.c. output

Fig. 1 Block diagram.

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | |
|---|---|---|---|
| Supply voltage | $V_{11\text{-}13}$ | max. | 13,2 V |
| Tuner a.g.c. voltage | $V_{4\text{-}13}$ | max. | 12 V |
| Total power dissipation | $P_{tot}$ | max. | 900 mW |
| Storage temperature | $T_{stg}$ | | −55 to + 125 °C |
| Operating ambient temperature | $T_{amb}$ | | −25 to + 60 °C |

## CHARACTERISTICS (measured in Fig. 5)

| | | | |
|---|---|---|---|
| Supply voltage range | $V_{11\text{-}13}$ | typ.<br> | 12 V<br>10,2 to 13,2 V |

The following characteristics are measured at $T_{amb}$ = 25 °C; $V_{11\text{-}13}$ = 12 V; f = 38,9 MHz

| | | | |
|---|---|---|---|
| I.F. input voltage for onset of a.g.c. (r.m.s. value) | $V_{1\text{-}16(rms)}$ | typ.<br>< | 100 µV<br>150 µV |
| Differential input impedance | $\lvert Z_{1\text{-}16} \rvert$ | typ. | 2 kΩ in parallel with 2 pF |
| Zero-signal output level | $V_{12\text{-}13}$ | typ. | 6 ± 0,3 V* |
| Top sync output level | $V_{12\text{-}13}$ | typ.<br> | 3,07 V<br>2,9 to 3,2 V |
| I.F. voltage gain control range | $G_v$ | typ. | 64 dB |
| Bandwidth of video amplifier (3 dB) | B | typ. | 6 MHz |
| Signal-to-noise ratio at $V_i$ = 10 mV | S/N | typ. | 58 dB** |
| Differential gain | dG | typ.<br>< | 4 %<br>10 % |
| Differential phase | dφ | typ.<br>< | 2°<br>10° |

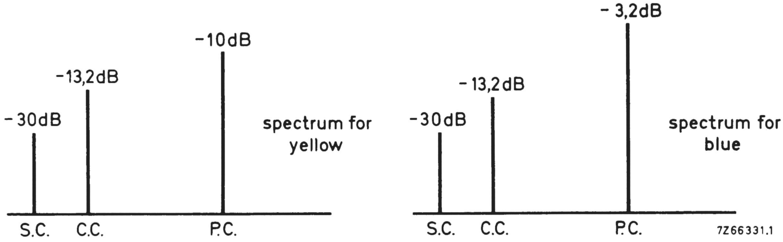
---

* So-called 'projected zero point', e.g. with switched demodulator.

$$** \ S/N = \frac{V_o \text{ black-to-white}}{V_{n(rms)} \text{ at } B = 5 \text{ MHz}}.$$

**CHARACTERISTICS** (continued)

| | | |
|---|---|---|
| Intermodulation at 1,1 MHz: blue* | > | 46 dB |
| | typ. | 60 dB |
| yellow* | > | 46 dB |
| | typ. | 50 dB |
| at 3,3 MHz** | > | 46 dB |
| | typ. | 54 dB |



S.C.: sound carrier level
C.C.: chrominance carrier level
P.C.: picture carrier level

} with respect to top sync level

Fig. 2 Input conditions for intermodulation measurements; standard colour bar with 75% contrast.

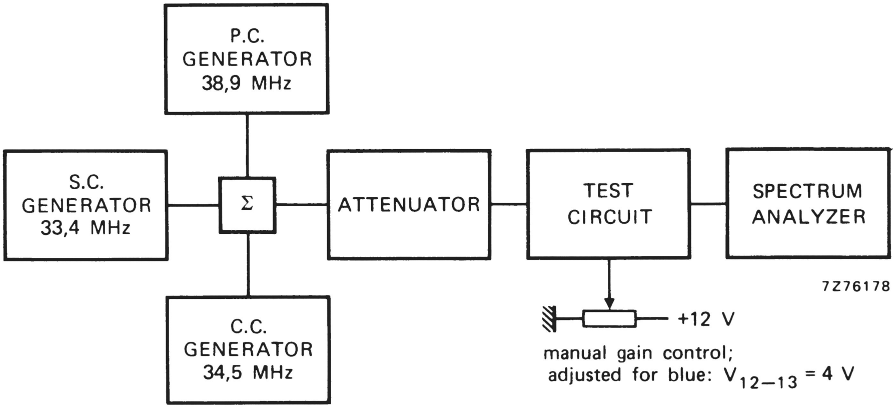

P.C. GENERATOR 38,9 MHz
S.C. GENERATOR 33,4 MHz
Σ
ATTENUATOR
TEST CIRCUIT
SPECTRUM ANALYZER
C.C. GENERATOR 34,5 MHz
7Z76178
+12 V
manual gain control;
adjusted for blue: $V_{12-13} = 4$ V

Fig. 3 Test set-up for intermodulation.

* $20 \log \dfrac{V_o \text{ at } 4{,}4 \text{ MHz}}{V_o \text{ at } 1{,}1 \text{ MHz}} + 3{,}6$ dB. ** $20 \log \dfrac{V_o \text{ at } 4{,}4 \text{ MHz}}{V_o \text{ at } 3{,}3 \text{ MHz}}$.

| | | | | |
|---|---|---|---|---|
| Carrier signal at video output | | typ.<br>< | 4<br>30 | mV<br>mV |
| 2nd harmonic of carrier at video output | | typ.<br>< | 20<br>30 | mV<br>mV |
| White spot inverter threshold level (Fig. 4) | | typ. | 6,6 | V |
| White spot insertion level (Fig. 4) | | typ. | 4,7 | V |
| Noise inverter threshold level (Fig. 4) | | typ. | 1,8 | V |
| Noise insertion level (Fig. 4) | | typ. | 3,8 | V |
| External video switch (VCR) switches off the output at: | $V_{14-13}$ | < | 1,1 | V |

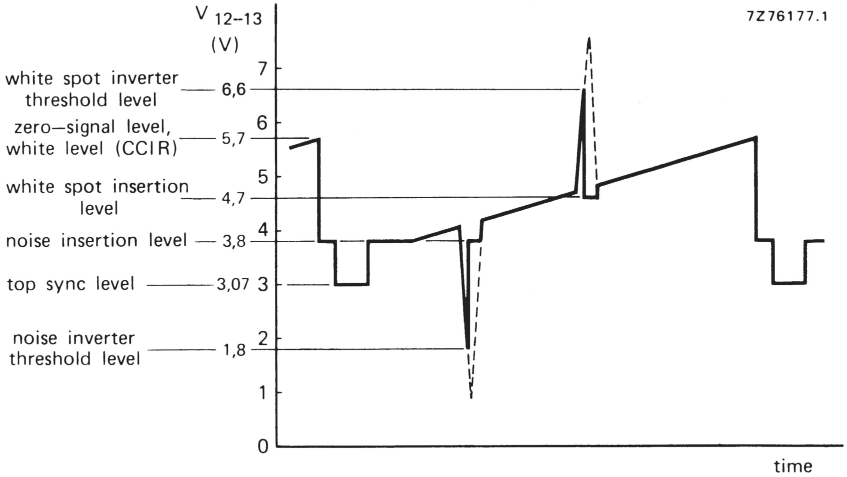


Fig. 4 Video output waveform showing white spot and noise inverter threshold levels.

| | | | | |
|---|---|---|---|---|
| Tuner a.g.c. output current range | $I_4$ | | 10 to 0 | mA |
| Tuner a.g.c. output voltage at $I_4$ = 10 mA | $V_{4-13}$ | < | 0,3 | V |
| Tuner a.g.c. output leakage current $V_{14-13}$ = 5 V; $V_{4-13}$ = 12 V | $I_4$ | < | 15 | μA |
| Maximum a.f.c. output voltage swing | $\Delta V_{5-13}$ | ><br>typ. | 10<br>11 | V<br>V |
| Detuning for a.f.c. output voltage swing of 10 V | $\Delta f$ | typ.<br>< | 100<br>200 | kHz<br>kHz |
| A.F.C. zero-signal output voltage (minimum gain) | $V_{5-13}$ | typ. | 6<br>4 to 8 | V<br>V |
| A.F.C. switches on at: | $V_{6-13}$ | > | 3,2 | V |
| A.F.C. switches off at: | $V_{6-13}$ | < | 1,5 | V |

## APPLICATION INFORMATION

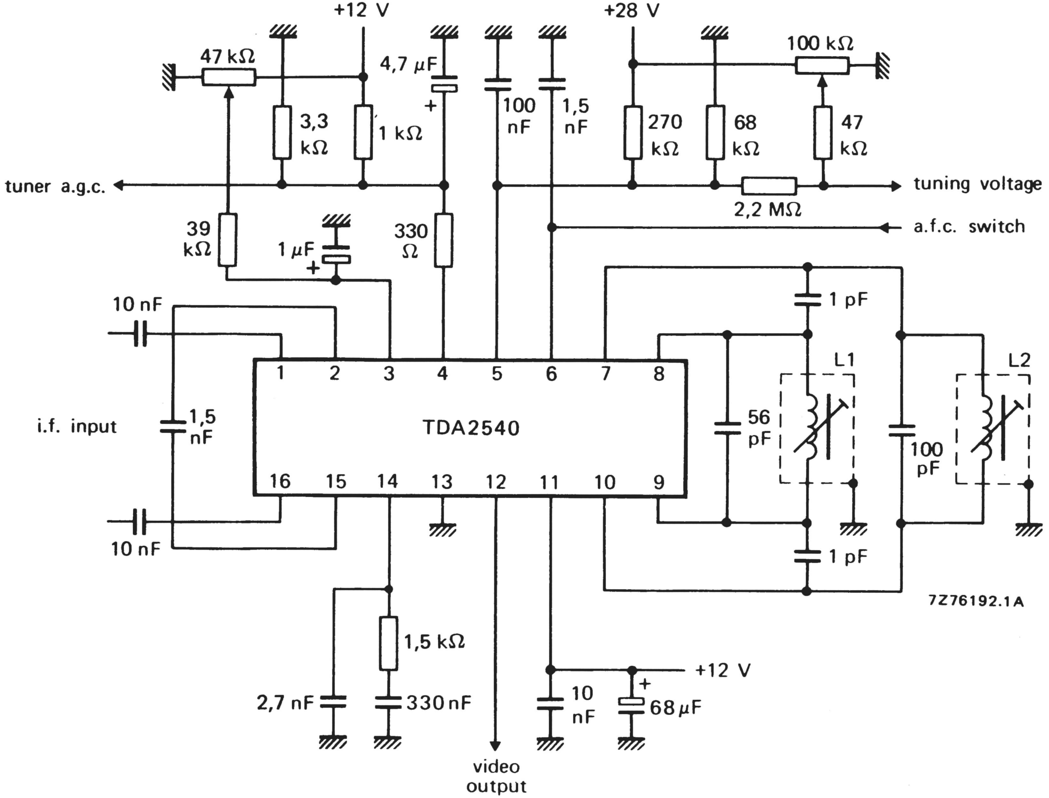
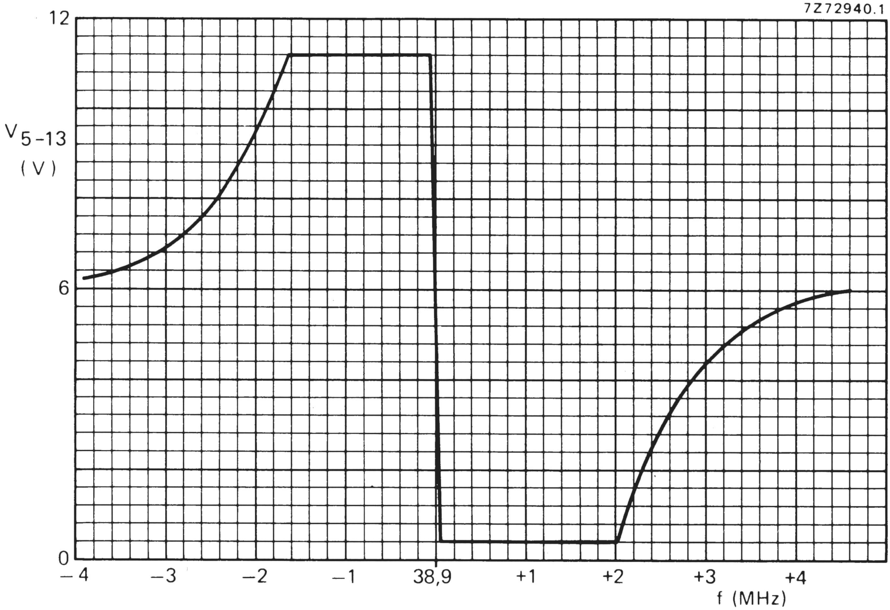

+12 V
47 kΩ
3,3 kΩ
1 kΩ
4,7 μF
+
100 nF
1,5 nF
+28 V
270 kΩ
68 kΩ
100 kΩ
47 kΩ
tuner a.g.c.
tuning voltage
2,2 MΩ
a.f.c. switch
39 kΩ
1 μF
+
330 Ω
10 nF
1,5 nF
10 nF
i.f. input
TDA2540
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
1 pF
56 pF
L1
100 pF
L2
1 pF
7Z76192.1A
1,5 kΩ
2,7 nF
330 nF
10 nF
68 μF
+
+12 V
video output

Fig. 5 Typical application circuit diagram; Q of L1 and L2 ≈ 80; f = 38,9 MHz.



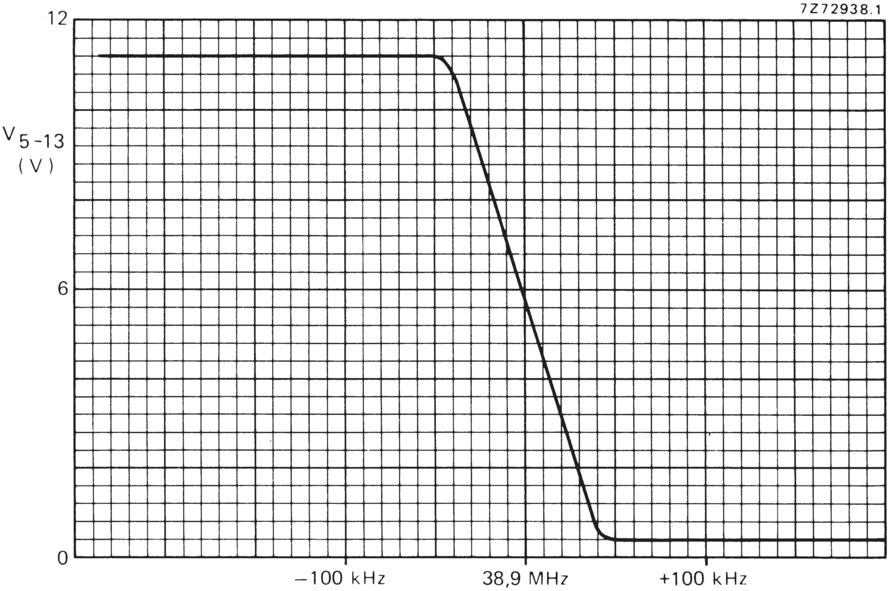


Fig. 6 A.F.C. output voltage ($V_{5-13}$) as a function of the frequency.

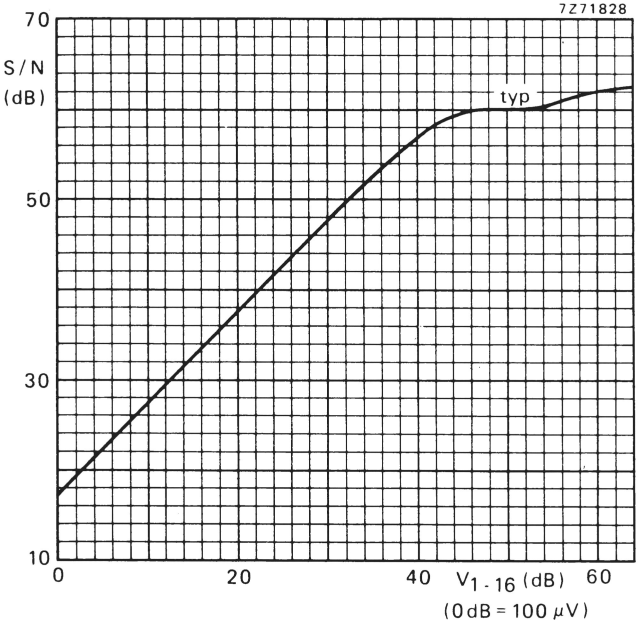


Fig. 7 Signal-to-noise ratio as a function of the input voltage ($V_{1-16}$).

# TELEVISION I.F. AMPLIFIER AND DEMODULATOR

The TDA2541 is an i.f. amplifier and demodulator circuit for colour and black and white television receivers using p-n-p tuners.
It incorporates the following functions:

- gain-controlled wide-band amplifier, providing complete i.f. gain
- synchronous demodulator
- white spot inverter
- video preamplifier with noise protection
- a.f.c. circuit which can be switched on/off by a d.c. level, e.g. during tuning
- a.g.c. circuit with noise gating
- tuner a.g.c. output (p-n-p tuners)
- VCR switch, which switches off the video output; e.g. for insertion of a VCR playback signal.

## QUICK REFERENCE DATA

| | | | | |
|---|---|---|---|---|
| Supply voltage | $V_{11\text{-}13}$ | typ. | 12 | V |
| Supply current | $I_{11}$ | typ. | 50 | mA |
| I.F. input voltage at f = 38,9 MHz (r.m.s. value) | $V_{1\text{-}16(rms)}$ | typ. | 100 | $\mu$V |
| Video output voltage (white at 10% of top sync) | $V_{12(p\text{-}p)}$ | typ. | 2,7 | V |
| I.F. voltage gain control range | $G_v$ | typ. | 64 | dB |
| Signal-to-noise ratio at $V_i$ = 10 mV | S/N | typ. | 58 | dB |
| A.F.C. output voltage swing for $\Delta f$ = 100 kHz | $\Delta V_{5\text{-}13}$ | typ. | 10 | V |

## PACKAGE OUTLINES

TDA2541 : 16-lead DIL; plastic (SOT-38).
TDA2541Q: 16-lead QIL; plastic (SOT-58).

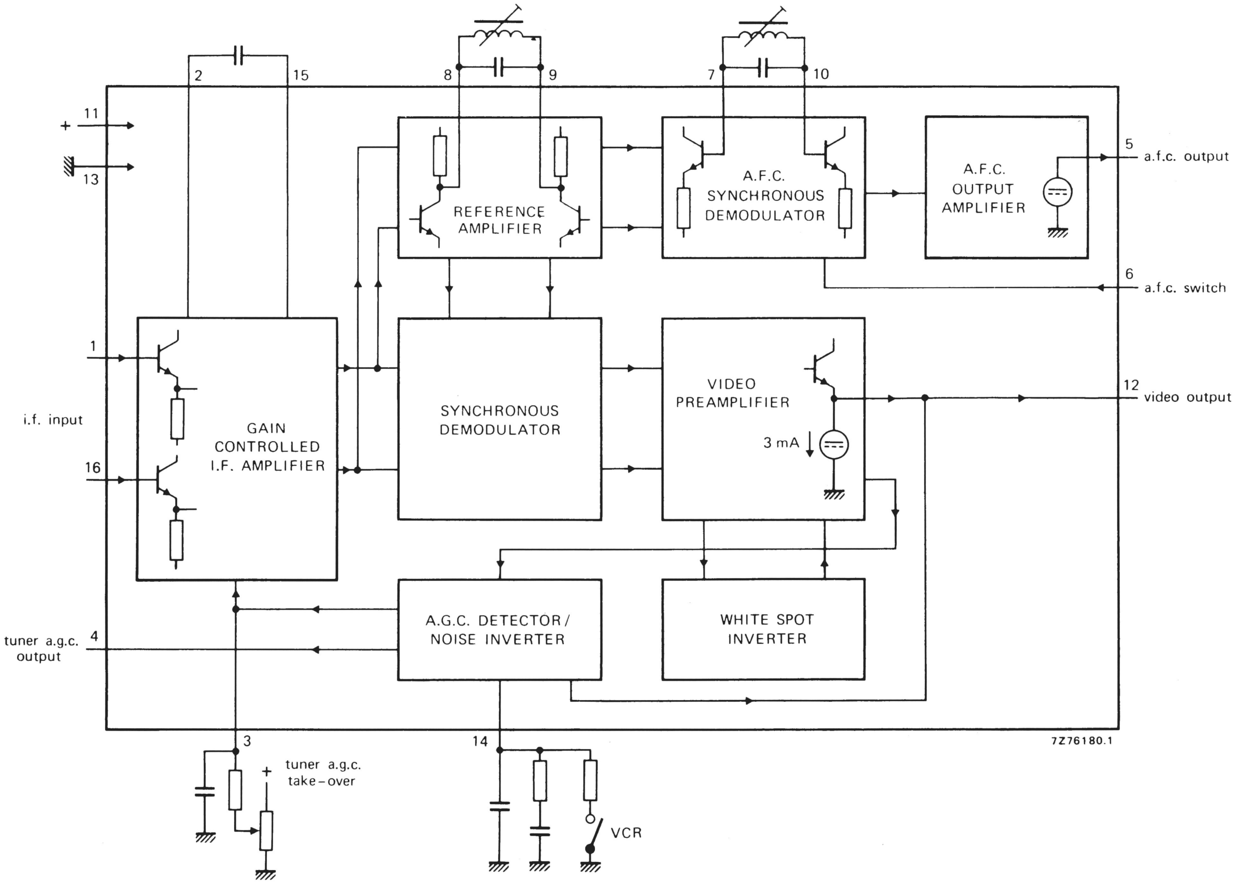

2
15
8
9
7
10
11
13
+
REFERENCE AMPLIFIER
A.F.C. SYNCHRONOUS DEMODULATOR
A.F.C. OUTPUT AMPLIFIER
5
a.f.c. output
6
a.f.c. switch
1
i.f. input
16
GAIN CONTROLLED I.F. AMPLIFIER
SYNCHRONOUS DEMODULATOR
VIDEO PREAMPLIFIER
3 mA
12
video output
tuner a.g.c. output
4
A.G.C. DETECTOR / NOISE INVERTER
WHITE SPOT INVERTER
7Z76180.1
3
tuner a.g.c. take–over
14
VCR

Fig. 1 Block diagram.

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | | |
|---|---|---|---|---|
| Supply voltage | $V_{11\text{-}13}$ | max. | 13,2 | V |
| Tuner a.g.c. voltage | $V_{4\text{-}13}$ | max. | 12 | V |
| Total power dissipation | $P_{tot}$ | max. | 900 | mW |
| Storage temperature | $T_{stg}$ | −55 to + 125 | | °C |
| Operating ambient temperature | $T_{amb}$ | −25 to + 60 | | °C |

**CHARACTERISTICS** (measured in Fig. 5)

| | | | | |
|---|---|---|---|---|
| Supply voltage range | $V_{11\text{-}13}$ | typ. | 12 | V |
| | | | 10,2 to 13,2 | V |

The following characteristics are measured at $T_{amb}$ = 25 °C; $V_{11\text{-}13}$ = 12 V; f = 38,9 MHz

| | | | | |
|---|---|---|---|---|
| I.F. input voltage for onset of a.g.c. (r.m.s. value) | $V_{1\text{-}16(rms)}$ | typ. | 100 | μV |
| | | < | 150 | μV |
| Differential input impedance | $\lvert Z_{1\text{-}16} \rvert$ | typ. | 2 kΩ in parallel with 2 pF | |
| Zero-signal output level | $V_{12\text{-}13}$ | typ. | 6 ± 0,3 | V* |
| Top sync output level | $V_{12\text{-}13}$ | typ. | 3,07 | V |
| | | | 2,9 to 3,2 | V |
| I.F. voltage gain control range | $G_v$ | typ. | 64 | dB |
| Bandwidth of video amplifier (3 dB) | B | typ. | 6 | MHz |
| Signal-to-noise ratio at $V_i$ = 10 mV | S/N | typ. | 58 | dB** |
| Differential gain | dG | typ. | 4 | % |
| | | < | 10 | % |
| Differential phase | dφ | typ. | 2° | |
| | | < | 10° | |

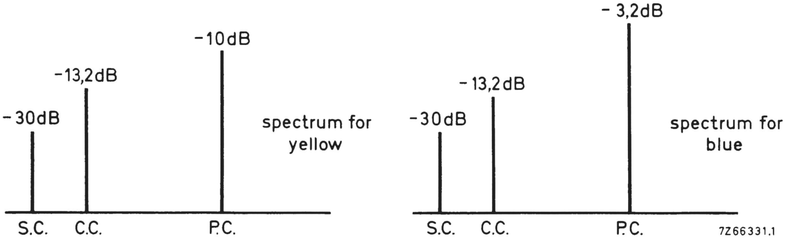
---

* So-called 'projected zero point', e.g. with switched demodulator.

**
$$S/N = \frac{V_o \text{ black-to-white}}{V_{n(rms)} \text{ at } B = 5 \text{ MHz}}.$$

**CHARACTERISTICS** (continued)

| | | |
|---|---|---|
| Intermodulation at 1,1 MHz: blue* | > | 46 dB |
| | typ. | 60 dB |
| yellow* | > | 46 dB |
| | typ. | 50 dB |
| at 3,3 MHz** | > | 46 dB |
| | typ. | 54 dB |



S.C. : sound carrier level
C.C. : chrominance carrier level
P.C. : picture carrier level
} with respect to top sync level

Fig. 2 Input conditions for intermodulation measurements; standard colour bar with 75% contrast.

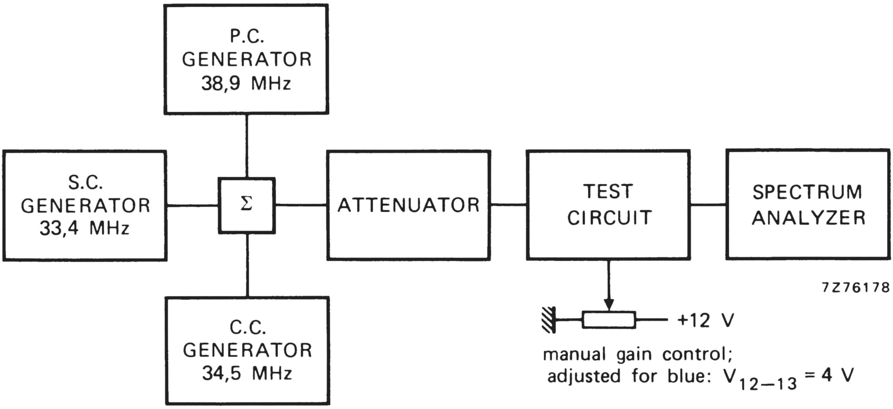

P.C. GENERATOR 38,9 MHz
S.C. GENERATOR 33,4 MHz
Σ
C.C. GENERATOR 34,5 MHz
ATTENUATOR
TEST CIRCUIT
SPECTRUM ANALYZER
7Z76178
+12 V
manual gain control;
adjusted for blue: $V_{12-13} = 4$ V

Fig. 3 Test set-up for intermodulation.

* $20 \log \dfrac{V_o \text{ at } 4{,}4 \text{ MHz}}{V_o \text{ at } 1{,}1 \text{ MHz}} + 3{,}6$ dB.

** $20 \log \dfrac{V_o \text{ at } 4{,}4 \text{ MHz}}{V_o \text{ at } 3{,}3 \text{ MHz}}$.

| | | | | |
|---|---|---|---|---|
| Carrier signal at video output | | typ.<br><| 4<br>30 | mV<br>mV |
| 2nd harmonic of carrier at video output | | typ.<br>< | 20<br>30 | mV<br>mV |
| White spot inverter threshold level (Fig. 4) | | typ. | 6,6 | V |
| White spot insertion level (Fig. 4) | | typ. | 4,7 | V |
| Noise inverter threshold level (Fig. 4) | | typ. | 1,8 | V |
| Noise insertion level (Fig. 4) | | typ. | 3,8 | V |
| External video switch (VCR) switches off the output at: | $V_{14-13}$ | < | 1,1 | V |

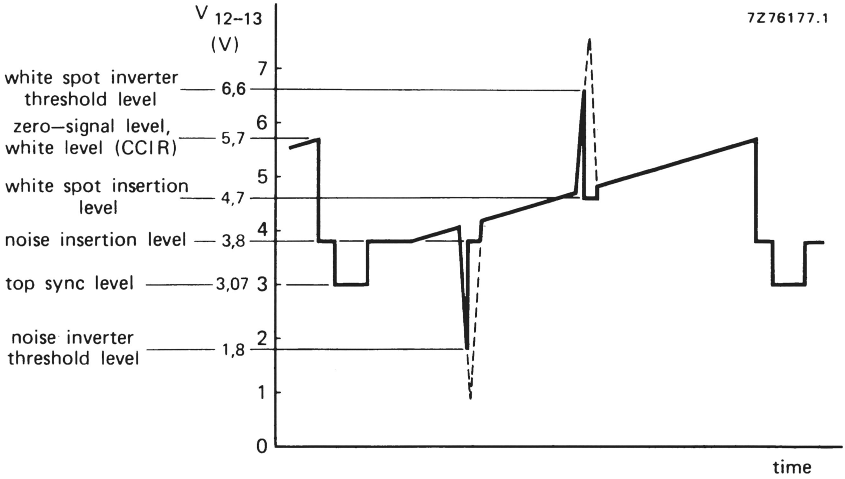


Fig. 4 Video output waveform showing white spot and noise inverter threshold levels.

| | | | | |
|---|---|---|---|---|
| Tuner a.g.c. output current range | $I_4$ | | 0 to 10 | mA |
| Tuner a.g.c. output voltage at $I_4$ = 10 mA | $V_{4-13}$ | < | 0,3 | V |
| Tuner a.g.c. output leakage current $V_{14-13}$ = 11 V; $V_{4-13}$ = 12 V | $I_4$ | < | 15 | µA |
| Maximum a.f.c. output voltage swing | $\Delta V_{5-13}$ | ><br>typ. | 10<br>11 | V<br>V |
| Detuning for a.f.c. output voltage swing of 10 V | $\Delta f$ | typ.<br>< | 100<br>200 | kHz<br>kHz |
| A.F.C. zero-signal output voltage (minimum gain) | $V_{5-13}$ | typ. | 6<br>4 to 8 | V<br>V |
| A.F.C. switches on at: | $V_{6-13}$ | > | 3,2 | V |
| A.F.C. switches off at: | $V_{6-13}$ | < | 1,5 | V |

## APPLICATION INFORMATION

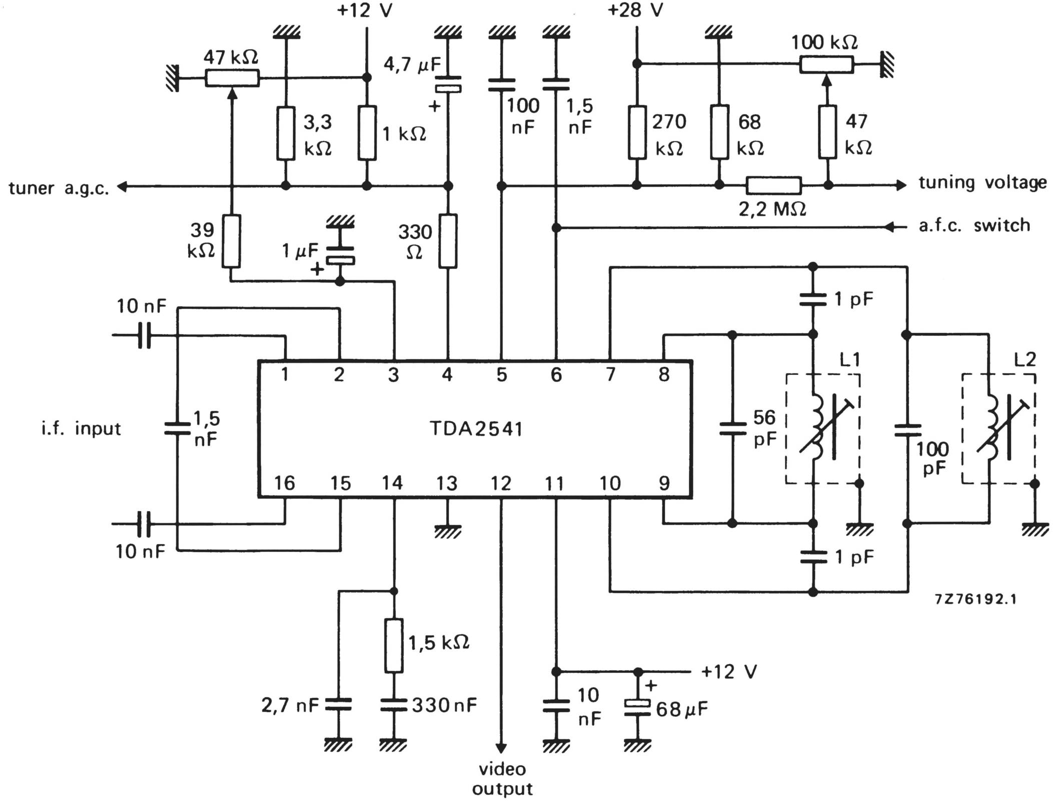
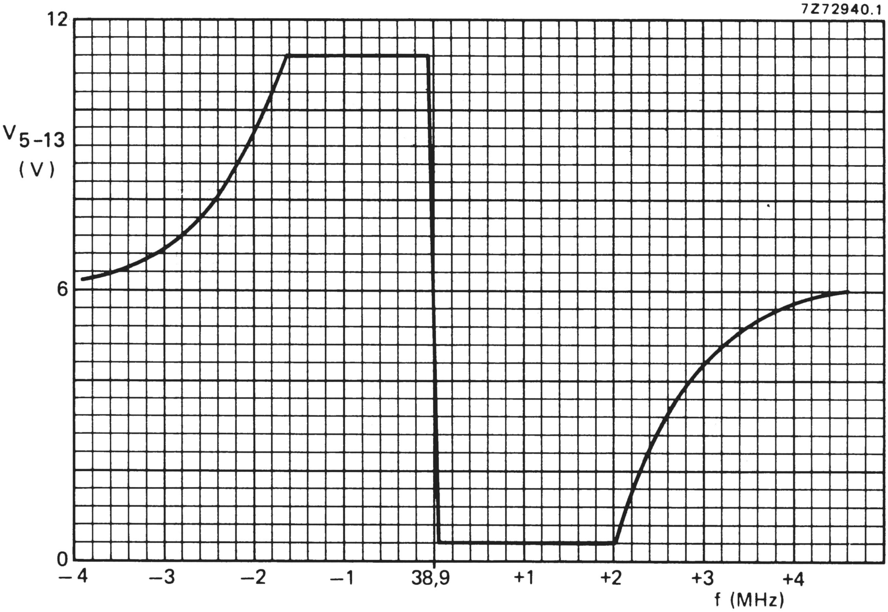

+12 V
47 kΩ
3,3 kΩ
1 kΩ
4,7 μF
+
100 nF
1,5 nF
+28 V
270 kΩ
68 kΩ
100 kΩ
47 kΩ
tuner a.g.c.
tuning voltage
2,2 MΩ
a.f.c. switch
39 kΩ
1 μF
+
330 Ω
10 nF
1,5 nF
i.f. input
10 nF
1
2
3
4
5
6
7
8
TDA2541
16
15
14
13
12
11
10
9
1 pF
56 pF
L1
100 pF
L2
1 pF
7Z76192.1
1,5 kΩ
2,7 nF
330 nF
video output
10 nF
+
68 μF
+12 V

Fig. 5 Typical application circuit diagram; Q of L1 and L2 ≈ 80; $f_o = 38,9$ MHz.



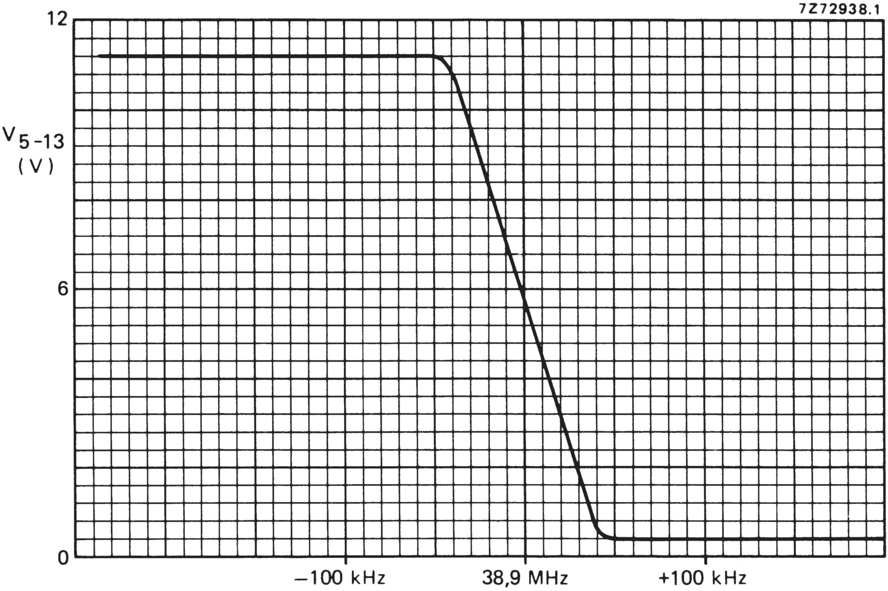


Fig. 6 A.F.C. output voltage ($V_{5-13}$) as a function of the frequency.

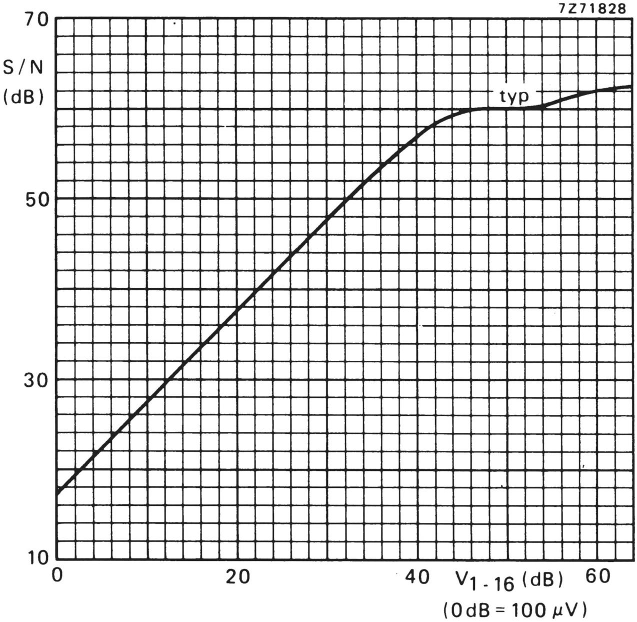


Fig. 7 Signal-to-noise ratio as a function of the input voltage ($V_{1\text{-}16}$).

# TELEVISION I.F. AMPLIFIER AND DEMODULATOR

The TDA2542 is an i.f. amplifier and demodulator circuit for E and L standards in colour and black and white television receivers using p-n-p tuners.
It incorporates the following functions:

- gain-controlled wide-band amplifier, providing complete i.f. gain
- synchronous demodulator
- video preamplifier
- a.f.c. circuit which can be switched on/off by a d.c. level, e.g. during tuning
- a.g.c. circuit
- tuner a.g.c. output (p-n-p tuners)

## QUICK REFERENCE DATA

| | | | | |
|---|---|---|---|---|
| Supply voltage | $V_{11\text{-}13}$ | typ. | 12 | V |
| Supply current | $I_{11}$ | typ. | 50 | mA |
| I.F. input voltage at f = 32,7 MHz (r.m.s. value) | $V_{1\text{-}16(rms)}$ | typ. | 100 | μV |
| Video output voltage (peak-to-peak value) | $V_{12(p\text{-}p)}$ | typ. | 3 | V |
| I.F. voltage gain control range | $G_v$ | typ. | 64 | dB |
| Signal-to-noise ratio at $V_i$ = 10 mV | S/N | typ. | 58 | dB |
| A.F.C. output voltage swing for Δf = 100 kHz | $\Delta V_{5\text{-}13}$ | typ. | 10 | V |

## PACKAGE OUTLINES

TDA2542 : 16-lead DIL; plastic (SOT-38).
TDA2542Q: 16-lead QIL; plastic (SOT-58).

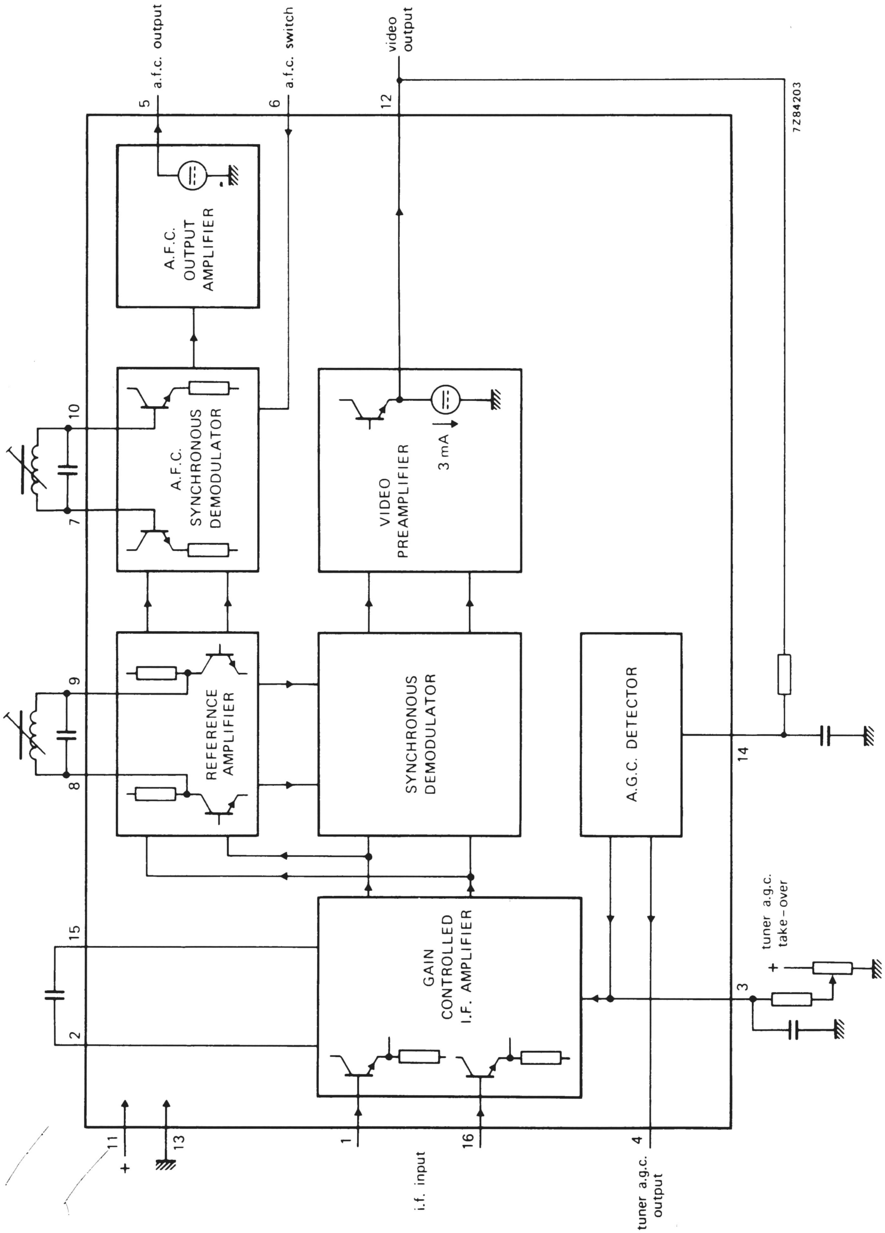

a.f.c. output
5
a.f.c. switch
6
video output
12
7Z84203
A.F.C. OUTPUT AMPLIFIER
A.F.C. SYNCHRONOUS DEMODULATOR
10
7
VIDEO PREAMPLIFIER
3 mA
REFERENCE AMPLIFIER
9
8
SYNCHRONOUS DEMODULATOR
A.G.C. DETECTOR
14
GAIN CONTROLLED I.F. AMPLIFIER
15
2
3
tuner a.g.c. take-over
+
11
+
13
1
16
i.f. input
4
tuner a.g.c. output

Fig. 1 Block diagram.

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | | |
|---|---|---|---|---|
| Supply voltage | $V_{11\text{-}13}$ | max. | 13,8 | V |
| Tuner a.g.c. voltage | $V_{4\text{-}13}$ | max. | 12 | V |
| Total power dissipation | $P_{tot}$ | max. | 900 | mW |
| Storage temperature | $T_{stg}$ | | −55 to + 125 | °C |
| Operating ambient temperature | $T_{amb}$ | | −25 to + 60 | °C |

## CHARACTERISTICS (measured in Fig. 2)

| | | | | |
|---|---|---|---|---|
| Supply voltage range | $V_{11\text{-}13}$ | typ.<br>10,2 to | 12<br>13,8 | V<br>V |

The following characteristics are measured at $T_{amb} = 25\ ^{o}C$; $V_{11\text{-}13} = 12$ V; f = 32,7 MHz

| | | | | |
|---|---|---|---|---|
| I.F. input voltage for onset of a.g.c. (r.m.s. value) | $V_{1\text{-}16(rms)}$ | typ.<br>$<$ | 100<br>150 | $\mu$V<br>$\mu$V |
| Differential input impedance | $\lvert Z_{1\text{-}16} \rvert$ | typ. | 2 kΩ in parallel with 2 pF | |
| Zero-signal output level | $V_{12\text{-}13}$ | typ. | 2,9 | V |
| Maximum video output voltage (peak-to-peak value) | $V_{12(p\text{-}p)}$ | $>$ | 4 | V |
| Video output voltage variation at 50 dB input voltage variation | $\Delta V_{12\text{-}13}$ | $<$ | 0,5 | dB |
| I.F. voltage gain control range | $G_v$ | typ. | 64 | dB |
| Bandwidth of video amplifier (3 dB) | B | typ. | 6 | MHz |
| Signal-to-noise ratio at $V_i = 10$ mV | S/N | typ. | 58 | dB* |
| Differential gain | dG | typ.<br>$<$ | 4<br>10 | %<br>% |
| Differential phase | $d\varphi$ | typ.<br>$<$ | 2°<br>10° | |

---

$$* \ S/N = \frac{V_o \text{ black-to-white}}{V_{n(rms)} \text{ at } B = 5 \text{ MHz}}.$$

**CHARACTERISTICS** (continued)

| | | | |
|---|---|---|---|
| Carrier signal at video output | | typ.<br>$<$ | 4 mV<br>30 mV |
| 2nd harmonic of carrier at video output | | typ.<br>$<$ | 20 mV<br>30 mV |
| Tuner a.g.c. output current range | $I_4$ | | 0 to 10 mA |
| Tuner a.g.c. output voltage at $I_4$ = 10 mA | $V_{4\text{-}13}$ | $<$ | 0,3 V |
| Tuner a.g.c. output leakage current $V_{14\text{-}13}$ = 3 V; $V_{4\text{-}13}$ = 12 V | $I_4$ | $<$ | 15 μA |
| Maximum a.f.c. output voltage swing | $\Delta V_{5\text{-}13}$ | $>$<br>typ. | 10 V<br>11 V |
| Detuning for a.f.c. output voltage swing of 10 V | $\Delta f$ | typ.<br>$<$ | 100 kHz<br>200 kHz |
| A.F.C. switches on at: | $V_{6\text{-}13}$ | $>$ | 3,2 V |
| A.F.C. switches off at: | $V_{6\text{-}13}$ | $<$ | 1,5 V |
| A.G.C. detector reference voltage | $V_{14\text{-}13}$ | typ. | 3,9 V |

## APPLICATION INFORMATION

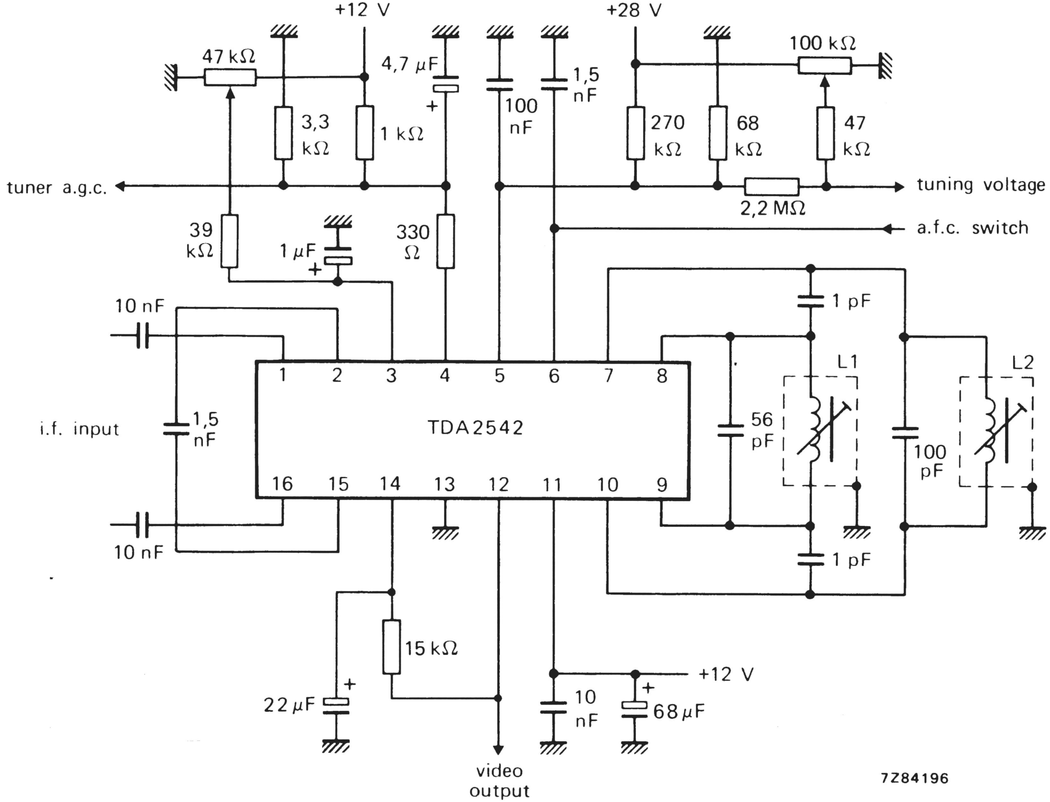
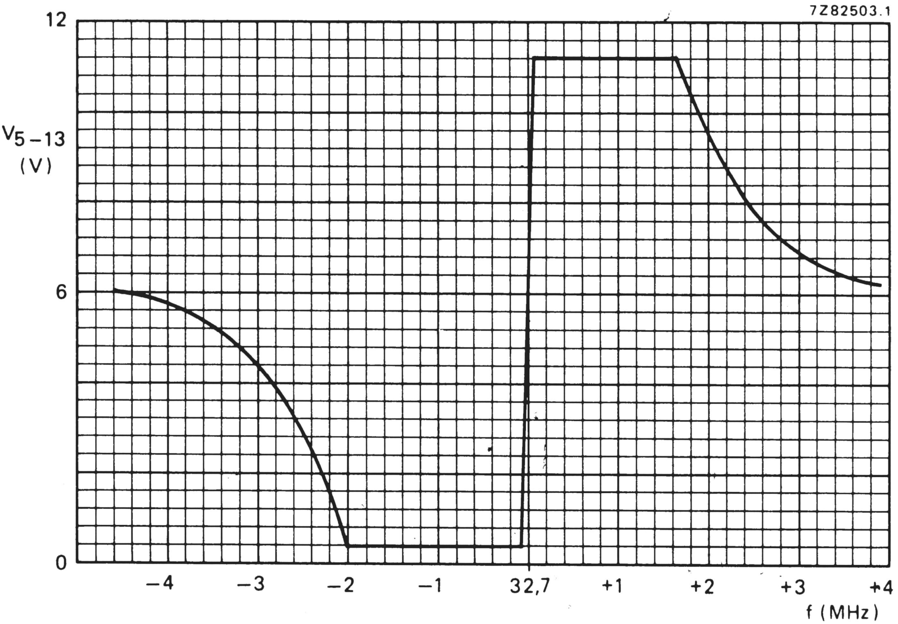

+12 V
47 kΩ
3,3 kΩ
1 kΩ
4,7 μF
+
100 nF
1,5 nF
+28 V
270 kΩ
68 kΩ
100 kΩ
47 kΩ
tuner a.g.c.
tuning voltage
2,2 MΩ
a.f.c. switch
39 kΩ
1 μF
+
330 Ω
10 nF
1,5 nF
10 nF
i.f. input
1
2
3
4
5
6
7
8
TDA2542
16
15
14
13
12
11
10
9
1 pF
L1
56 pF
100 pF
L2
1 pF
15 kΩ
22 μF
+
10 nF
68 μF
+
+12 V
video output
7Z84196

Fig. 2 Typical application circuit diagram; Q of L1 and L2 ≈ 80; f = 32,7 MHz.



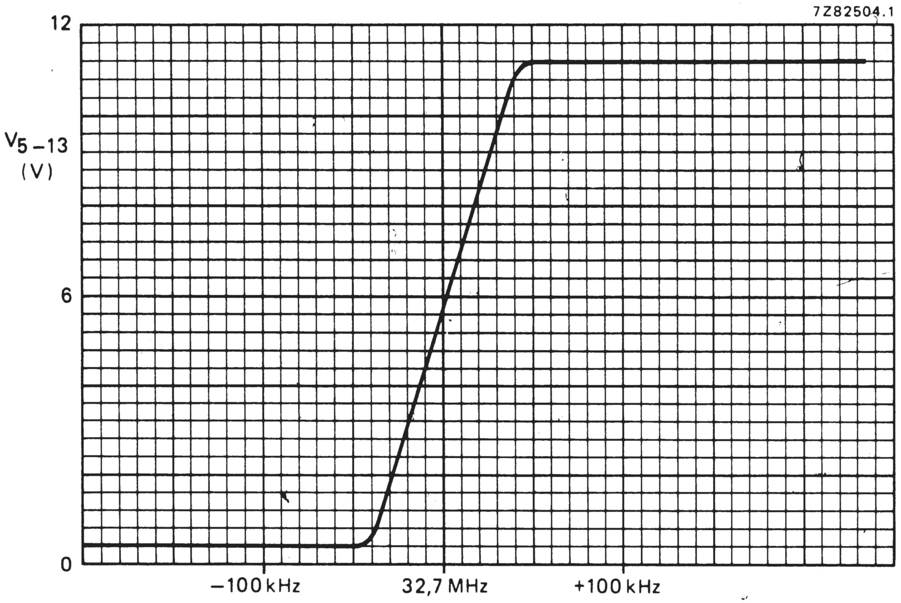


Fig. 3 A.F.C. output voltage ($V_{5\text{-}13}$) as a function of the frequency.

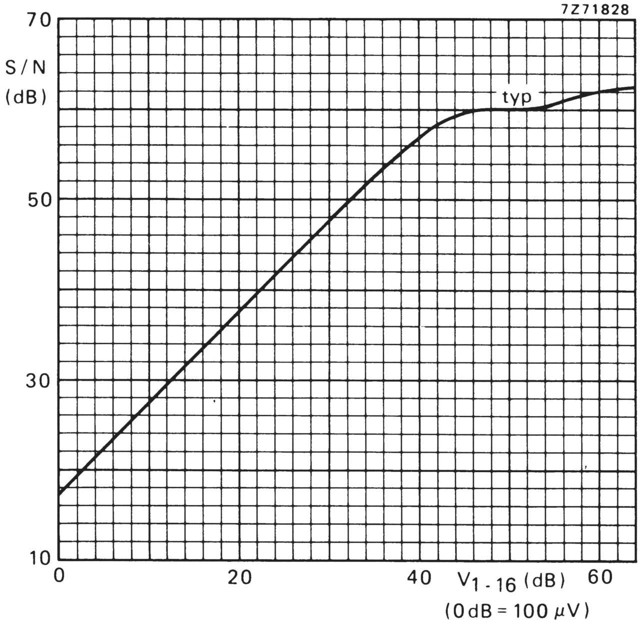


Fig. 4 Signal-to-noise ratio as a function of the input voltage ($V_{1-16}$).

DEVELOPMENT SAMPLE DATA
This information is derived from development samples made available for evaluation. It does not necessarily imply that the device will go into regular production.

# AM SOUND I.F. CIRCUIT FOR FRENCH STANDARD

## GENERAL DESCRIPTION

The TDA2543 is a monolithic integrated AM sound i.f. circuit in television receivers for the French standards L and L′.

The circuit incorporates the following functions:

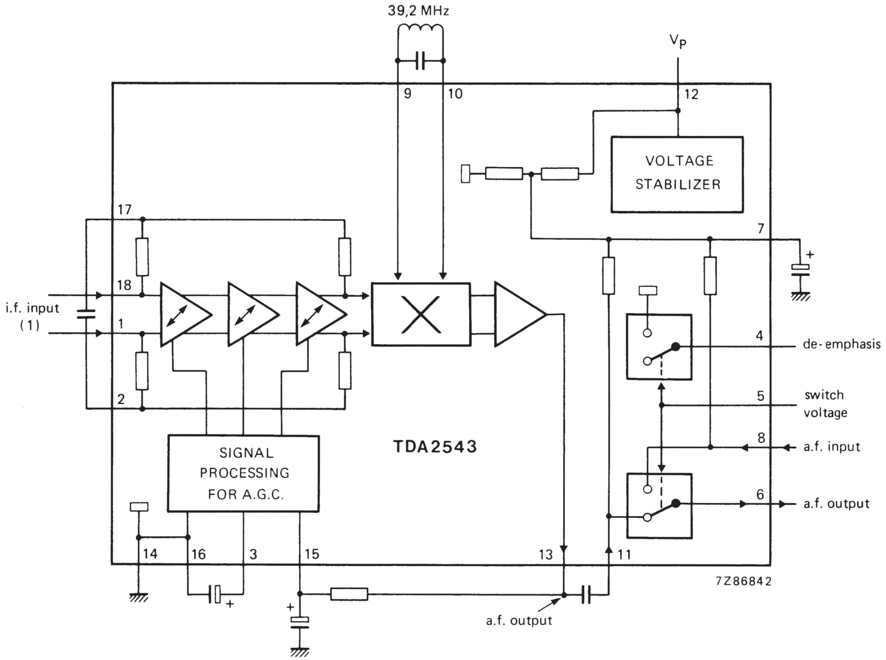
- 3-stage gain controlled i.f. amplifier, providing complete i.f. gain
- Synchronous AM demodulator
- A.G.C. circuit
- Audio input circuit with two external audio inputs and switching facilities to provide for either the demodulated i.f. or an external signal output
- Demodulated i.f. output is available from the input of the switching circuit

## QUICK REFERENCE DATA

| | | | | |
|---|---|---|---|---|
| Supply voltage (pin 12) | $V_{12\text{-}14} = V_P$ | typ. | 12 | V |
| Minimum i.f. vision carrier input voltage (r.m.s. value) for an output signal $V_{13\text{-}14(rms)} = 480$ mV | $V_{VC1\text{-}18(rms)}$ | max. | 30 | μV |
| I.F. control range | $\Delta G_v$ | min. | 60 | dB |
| A.F. output voltage (r.m.s. value) | $V_{13\text{-}14(rms)}$ | typ. | 680 | mV |
| Distortion at $V_{VC1\text{-}18(rms)} = 5$ mV | $d_{tot}$ | max. | 1 | % |
| Signal-to-weighted-noise ratio according to CCIR 468 | S + N/N | min. | 50 | dB |
| Maximum signal amplitude for the a.f. switch (r.m.s. value) | $V_{8;11\text{-}14(rms)}$ | min. | 2 | V |

## PACKAGE OUTLINE

18-lead DIL; plastic (SOT-102CS).


39,2 MHz
$V_P$
9
10
12
VOLTAGE STABILIZER
17
7
+
18
i.f. input
(1)
1
4
de-emphasis
5
switch voltage
2
8
a.f. input
SIGNAL PROCESSING FOR A.G.C.
TDA2543
6
a.f. output
14
16
3
15
13
11
7Z86842
+
+
a.f. output

(1) I.F. signal: vision carrier (V.C.) and sound carrier (S.C.).

Fig. 1 Block diagram.

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | | |
|---|---|---|---|---|
| Supply voltage range (pin 12) | $V_{12\text{-}14} = V_P$ | max. | 13,2 | V |
| Switch voltage (pin 5) | $V_{5\text{-}14}$ | max. | $V_P$ | V |
| Current at pin 4 | $I_4$ | max. | 5 | mA |
| | $-I_4$ | short-circuit proof | | |
| Storage temperature range | $T_{stg}$ | −25 to +150 | | °C |
| Operating ambient temperature range | $T_{amb}$ | −20 to +70 | | °C |

## CHARACTERISTICS

$V_P$ = 12 V; $T_{amb}$ = 25 °C; input signal (vision carrier V.C.) with $f_{VC}$ = 39,2 MHz; sound carrier (S.C.) modulated with $f_m$ = 1 kHz and m = 0,8; measured in Fig. 2; unless otherwise specified

| parameter | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| **Supply** | | | | | |
| Supply voltage range (pin 12) | $V_P$ | 10,8 | – | 13,2 | V |
| Supply current (pin 12) | $I_P$ | – | 50 | – | mA |
| **I.F. input** (pins 1 and 18) | | | | | |
| Minimum i.f. vision carrier input voltage (r.m.s. value) for an output signal $V_{13\text{-}14(rms)}$ = 480 mV | $V_{VC1\text{-}18(rms)}$ | – | – | 30 | μV |
| Maximum i.f. vision carrier input voltage (r.m.s. value) | $V_{VC1\text{-}18(rms)}$ | – | 50 | – | mV |
| Input resistance | $R_{1\text{-}18}$ | – | 2 | – | kΩ |
| Input capacitance | $C_{1\text{-}18}$ | – | 2 | – | pF |
| I.F. control range (–3 dB) | $\Delta G_v$ | 60 | – | – | dB |
| **A.F. output** (pin 13) | | | | | |
| A.F. output voltage (r.m.s. value) at $V_{VC1\text{-}18(rms)}$ = 5 mV | $V_{13\text{-}14(rms)}$ | – | 680 | – | mV |
| Output resistance | $R_{13\text{-}14}$ | – | 100 | – | Ω |
| Distortion at $V_{VC1\text{-}18(rms)}$ = 5 mV | $d_{tot}$ | – | – | 1 | % |
| Signal-to-weighted-noise ratio at a.f. output (pin 13) according to CCIR 468 at $V_{VC1\text{-}18(rms)}$ = 5 mV | S + N/N | 50 | – | – | dB |
| **A.F. switch** (pins 8, 11 and 6) | | | | | |
| Maximum input voltage (r.m.s. value) | $V_{8\text{-}14(rms)}$<br>$V_{11\text{-}14(rms)}$ | 2<br>2 | –<br>– | –<br>– | V<br>V |
| Voltage gain | $G_v$ | – | 0 ± 1 | – | dB |
| Amplitude frequency response (–3 dB) | f | 20 | – | 20 000 | Hz |
| Crosstalk between the non-switched input and the output | $\alpha$ | 60 | – | – | dB |
| Input resistance | $R_{8;\,11\text{-}14}$ | 10 | – | – | kΩ |
| Output resistance | $R_{6\text{-}14}$ | – | 400 | – | Ω |
| **De-emphasis switch** (pin 4) | | | | | |
| Input resistance for: | | | | | |
| ON ($V_{5\text{-}14} > 3$ V) | $R_{4\text{-}14}$ | – | – | 200 | Ω |
| OFF ($V_{5\text{-}14} < 1$ V) | $R_{4\text{-}14}$ | 100 | – | – | kΩ |
| **Switch voltage** (pin 5) | | | | | |
| A.F. switch ON (pin 8 switched) | $V_{5\text{-}14}$ | 3 | – | $V_P$ | V |
| A.F. switch OFF (pin 11 switched) | $V_{5\text{-}14}$ | 0 | – | 1 | V |

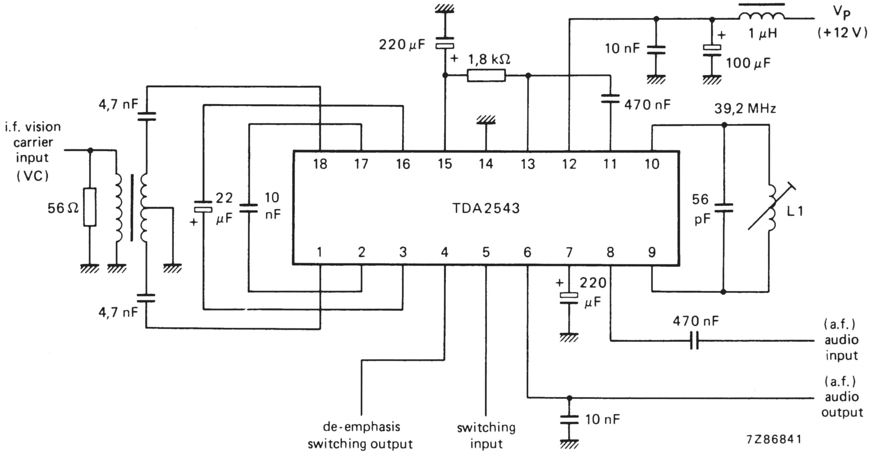

220 µF
+
1,8 kΩ
10 nF
+
1 µH
100 µF
VP
(+12 V)
4,7 nF
470 nF
39,2 MHz
i.f. vision
carrier
input
(VC)
18
17
16
15
14
13
12
11
10
56 Ω
22
µF
+
10
nF
TDA2543
56
pF
L1
1
2
3
4
5
6
7
8
9
4,7 nF
+
220
µF
470 nF
(a.f.)
audio
input
(a.f.)
audio
output
10 nF
de-emphasis
switching output
switching
input
7Z86841

Fig. 2 Measuring circuit; L1 adjusted to minimum distortion at the a.f. output.

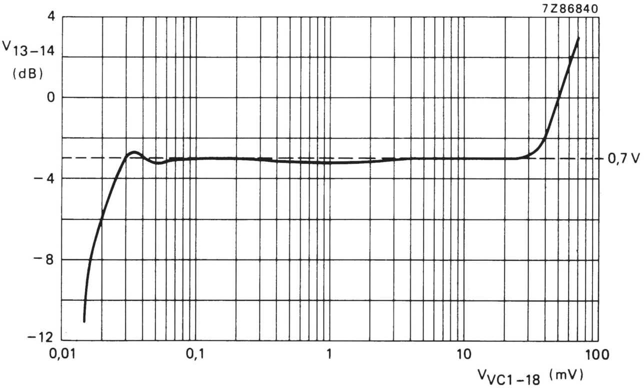


Fig. 3 Control curve of the i.f. amplifier; the r.m.s. a.f. output voltage at pin 13 ($V_{13\text{-}14(rms)}$) as a function of the r.m.s. i.f. vision carrier input voltage ($V_{VC1\text{-}18(rms)}$) at $f_m$ = 1 kHz and m = 0,8.

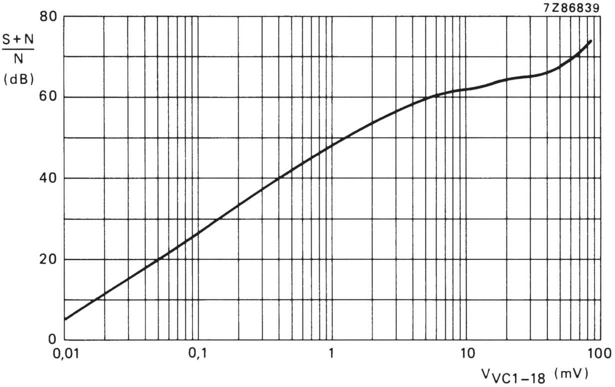


Fig. 4 Signal-to-weighted-noise ratio (S + N/N) at the output (pin 13) as a function of the r.m.s. i.f. vision carrier input voltage ($V_{VC1\text{-}18(rms)}$).

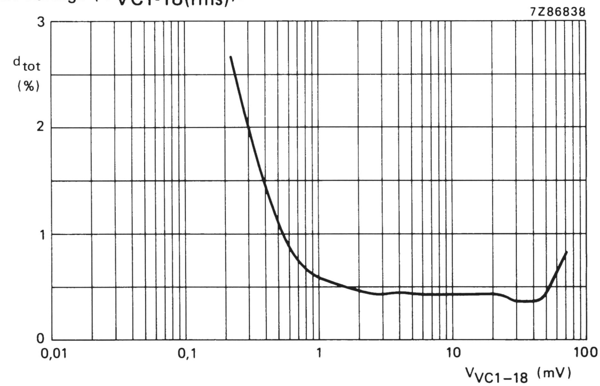


Fig. 5 Distortion ($d_{tot}$) at the output (pin 13) as a function of the r.m.s. i.f. vision carrier input voltage ($V_{VC1\text{-}18(rms)}$) at $f_m$ = 1 kHz and m = 0,8.

DEVELOPMENT SAMPLE DATA

# TELEVISION I.F. AMPLIFIER AND DEMODULATOR

The TDA2544 is an i.f. amplifier and demodulator circuit for colour and black and white television receivers.
It incorporates the following functions:

- gain-controlled wide-band amplifier, providing complete i.f. gain
- low-level synchronous demodulator
- white spot inverter
- video preamplifier with noise protection
- a.f.c. circuit with balanced output
- a.g.c. circuit with noise gating
- tuner a.g.c. output for control of MOS tuners
- external video switch

## QUICK REFERENCE DATA

| | | | | |
|---|---|---|---|---|
| Supply voltage | $V_{11\text{-}13}$ | typ. | 12 | V |
| Supply current | $I_{11}$ | typ. | 50 | mA |
| I.F. input sensitivity at f = 45,75 MHz (r.m.s. value) | $V_{1\text{-}16(rms)}$ | typ. | 150 | $\mu$V |
| Video output voltage (white at 12,5% of top sync) | $V_{12(p\text{-}p)}$ | typ. | 2,6 | V |
| I.F. voltage gain control range | $G_v$ | typ. | 63 | dB |
| Signal-to-noise ratio $V_i$ = 10 mV | S/N | typ. | 58 | dB |
| A.F.C. sensitivity | | typ. | 80 | mV/kHz |

## PACKAGE OUTLINES

TDA2544 16-lead DIL; plastic (SOT-38).
TDA2544Q: 16-lead QIL; plastic (SOT-58).

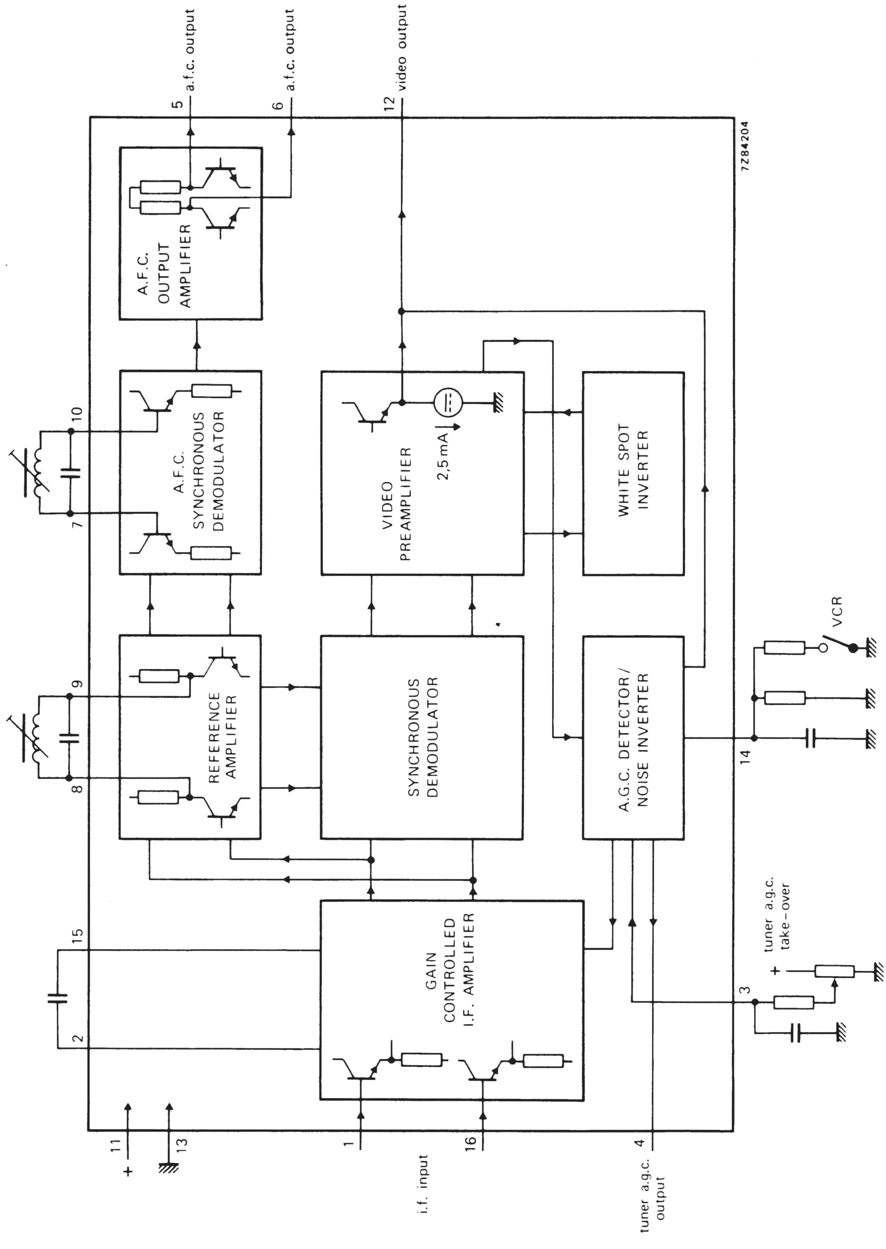

5
a.f.c. output
6
a.f.c. output
12
video output
7Z84204
A.F.C.
OUTPUT
AMPLIFIER
A.F.C.
SYNCHRONOUS
DEMODULATOR
10
7
VIDEO
PREAMPLIFIER
2,5 mA
WHITE SPOT
INVERTER
9
8
REFERENCE
AMPLIFIER
SYNCHRONOUS
DEMODULATOR
A.G.C. DETECTOR/
NOISE INVERTER
VCR
14
15
2
GAIN
CONTROLLED
I.F. AMPLIFIER
tuner a.g.c.
take-over
+
3
11
+
13
1
16
i.f. input
4
tuner a.g.c.
output

Fig. 1 Block diagram.

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | | |
|---|---|---|---|---|
| Supply voltage | $V_{11\text{-}13}$ | max. | 13,8 | V |
| Tuner a.g.c. voltage | $V_{4\text{-}13}$ | max. | 12 | V |
| Total power dissipation | $P_{tot}$ | max. | 1,2 | W |
| Storage temperature | $T_{stg}$ | | −55 to + 125 | °C |
| Operating ambient temperature | $T_{amb}$ | | −25 to + 65 | °C |

## CHARACTERISTICS (measured in Fig. 5)

| | | | | |
|---|---|---|---|---|
| Supply voltage range | $V_{11\text{-}13}$ | typ.<br> | 12<br>10,2 to 13,8 | V<br>V |

The following characteristics are measured at $T_{amb}$ = 25 °C; $V_{11\text{-}13}$ = 12 V

| | | | | |
|---|---|---|---|---|
| I.F. input voltage for onset of a.g.c. (r.m.s. value) at f = 45,75 MHz | $V_{1\text{-}16(rms)}$ | typ. | 150 | $\mu$V |
| Differential input impedance | $\lvert Z_{1\text{-}16} \rvert$ | typ. | 3 kΩ in parallel with 2 pF | |
| Zero-signal output level | $V_{12\text{-}13}$ | typ. | 5,5 | V* |
| Top sync output level | $V_{12\text{-}13}$ | typ. | 2,5 | V |
| I.F. voltage gain control range | $G_v$ | typ. | 63 | dB |
| Bandwidth of video amplifier (3 dB) | B | typ. | 6 | MHz |
| Signal-to-noise ratio at $V_i$ = 10 mV | S/N | typ. | 58 | dB** |
| Differential gain | dG | typ.<br>< | 4<br>10 | %<br>% |
| Differential phase | d$\varphi$ | typ.<br>< | 2°<br>10° | |

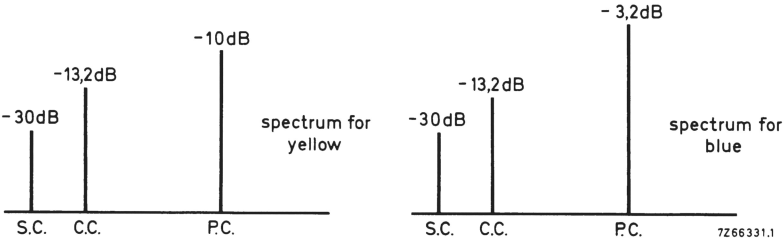
---

* So-called 'projected zero point', e.g. with switched demodulator.

** $$S/N = \frac{V_o \text{ black-to-white}}{V_{n(rms)} \text{ at } B = 5 \text{ MHz}}.$$

**CHARACTERISTICS** (continued)

| | | |
|---|---|---|
| Intermodulation at 0,9 MHz: blue* | typ. | 50 dB |
| yellow* | typ. | 46 dB |
| at 2,6 MHz** | typ. | 49 dB |



S.C. : sound carrier level
C.C. : chrominance carrier level
P.C. : picture carrier level
} with respect to top sync level

Fig. 2 Input conditions for intermodulation measurements; standard colour bar with 75% contrast.

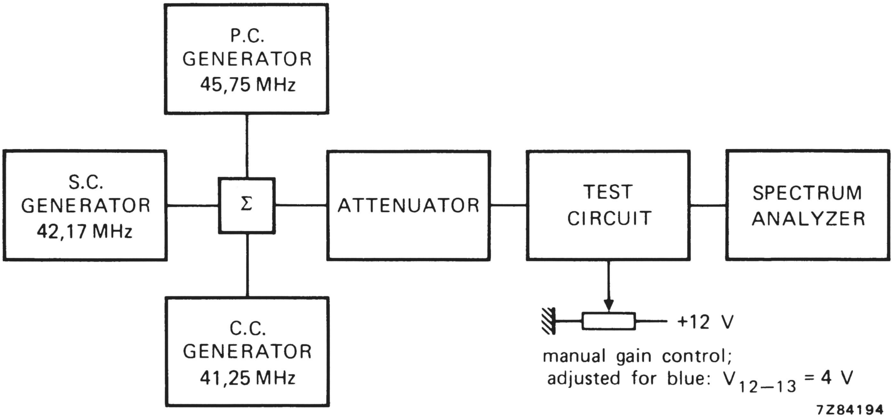

P.C. GENERATOR 45,75 MHz
S.C. GENERATOR 42,17 MHz
Σ
C.C. GENERATOR 41,25 MHz
ATTENUATOR
TEST CIRCUIT
SPECTRUM ANALYZER
+12 V
manual gain control;
adjusted for blue: $V_{12-13}$ = 4 V
7Z84194

Fig. 3 Test set-up for intermodulation.

---

* $20 \log \frac{V_o \text{ at } 3,6 \text{ MHz}}{V_o \text{ at } 0,9 \text{ MHz}} + 3,6 \text{ dB}.$ ** $20 \log \frac{V_o \text{ at } 3,6 \text{ MHz}}{V_o \text{ at } 2,6 \text{ MHz}}.$

| | | | | |
|---|---|---|---|---|
| Carrier signal at video output | | < | 30 | mV |
| 2nd harmonic of carrier at video output | | < | 30 | mV |
| White spot inverter threshold level (Fig. 4) | | typ. | 6,4 | V |
| White spot insertion level (Fig. 4) | | typ. | 4,1 | V |
| Noise inverter threshold level (Fig. 4) | | typ. | 1,6 | V |
| Noise insertion level (Fig. 4) | | typ. | 3,3 | V |
| External video switch (VCR) switches off the output at | $V_{14-13}$ | < | 1,0 | V |

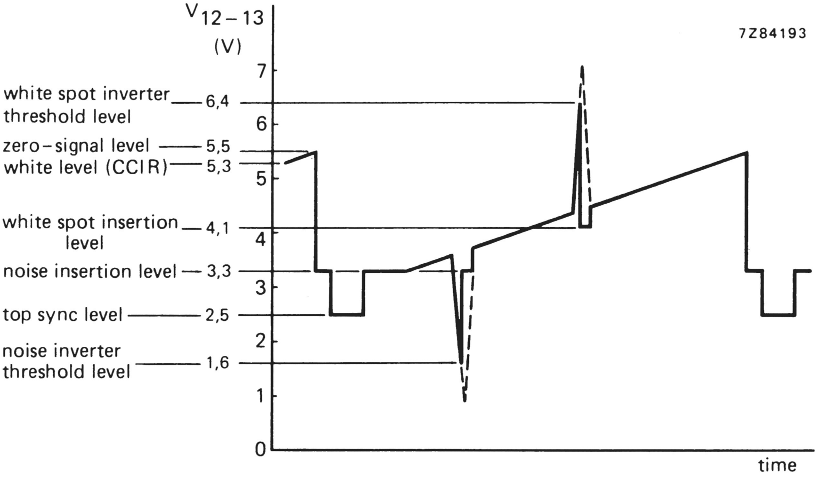


Fig. 4 Video output waveform showing white spot and noise inverter threshold levels.

| | | | | |
|---|---|---|---|---|
| Tuner a.g.c. output current range | $I_4$ | | 0 to 0,3 | mA |
| Tuner a.g.c. output voltage at $I_4 = 0,3$ mA | $V_{4-13}$ | < | 0,3 | V |
| Tuner a.g.c. output leakage current $V_{14-13} = 3$ V; $V_{4-13} = 12$ V | $I_4$ | < | 10 | $\mu$A |
| A.F.C. output voltage (d.c. value) | $V_{5;6-13}$ | typ. | 6,8 | V |
| A.F.C. output offset voltage | $\lvert V_{5-6} \rvert$ | < | 1,5 | V |
| Maximum a.f.c. output voltage | $V_{5;6-13}$ | > | 11,6 | V |
| Minimum a.f.c. output voltage | $V_{5;6-13}$ | < | 2,8 | V |
| A.F.C. sensitivity | | typ. | 80 | mV/kHz |

## APPLICATION INFORMATION

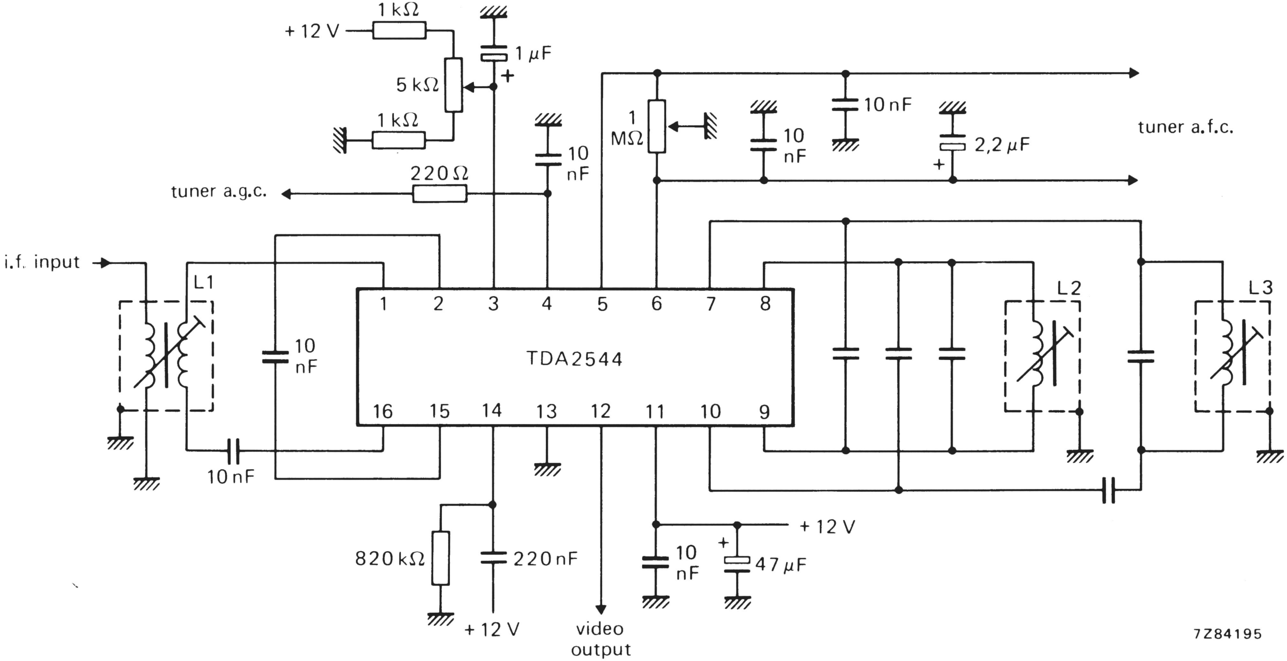

+ 12 V
1 kΩ
5 kΩ
1 kΩ
1 μF
+
10 nF
220 Ω
tuner a.g.c.
1 MΩ
10 nF
10 nF
2,2 μF
+
tuner a.f.c.
i.f. input
L1
10 nF
10 nF
TDA2544
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
L2
L3
820 kΩ
220 nF
+ 12 V
video output
10 nF
47 μF
+
+ 12 V
7Z84195

Fig. 5 Typical application diagram.

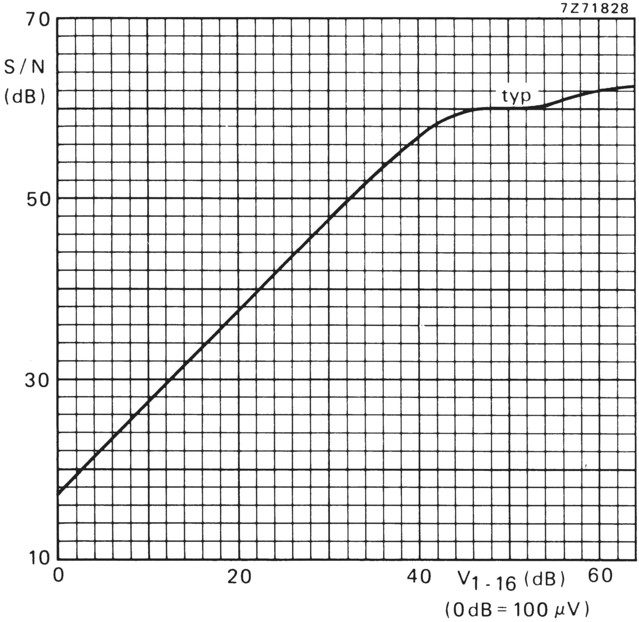


Fig. 6 Signal-to-noise ratio as a function of the input voltage ($V_{1-16}$).

# QUASI-SPLIT-SOUND CIRCUIT

The TDA2545 is a monolithic integrated circuit for quasi-split-sound processing in television receivers.

The circuit incorporates the following functions:

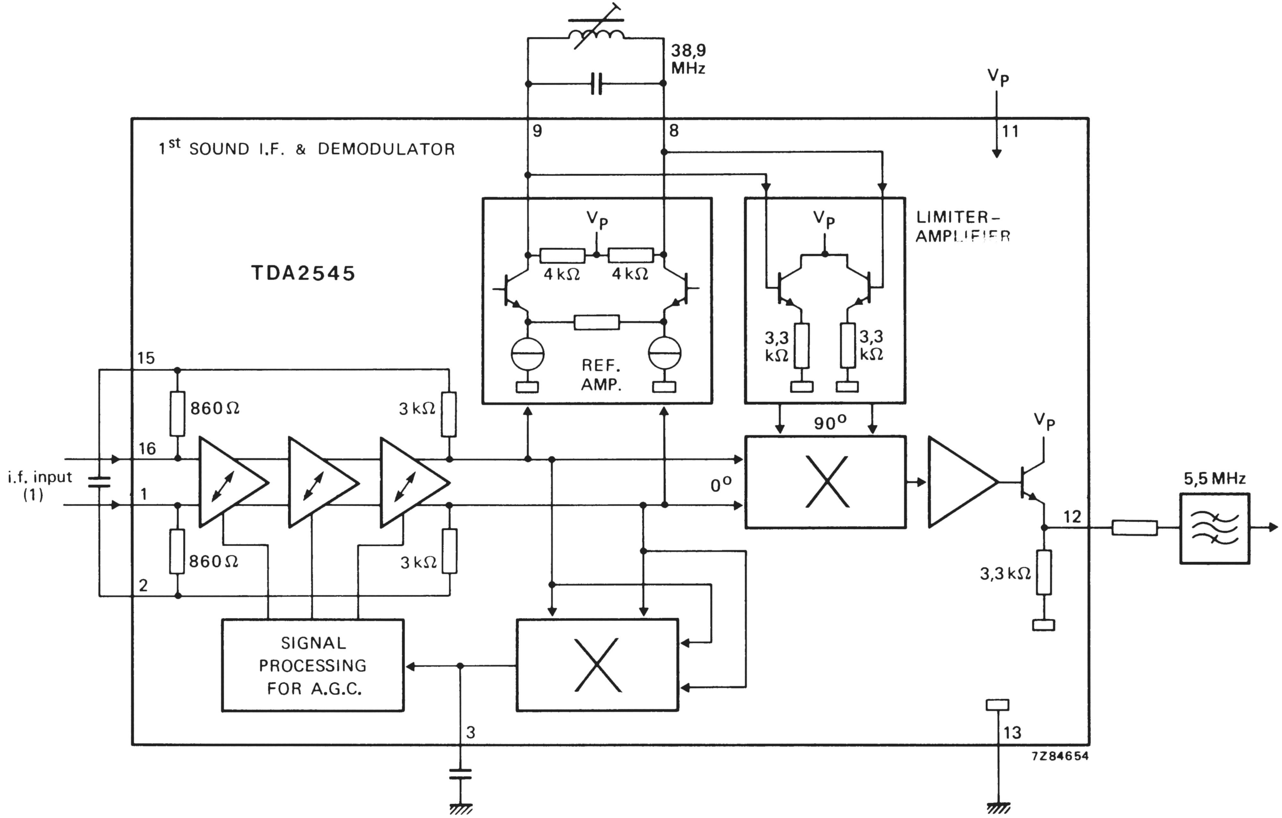
- 3-stage gain controlled i.f. amplifier
- a.g.c. circuit
- reference amplifier with limiter amplifier for vision carrier (V.C.) processing
- linear multiplier for quadrature demodulation

## QUICK REFERENCE DATA

| | | | | |
|---|---|---|---|---|
| Supply voltage | $V_{11\text{-}13} = V_P$ | typ. | 12 | V |
| Minimum i.f. vision carrier input voltage (r.m.s. value) | $V_{VC1\text{-}16\,(rms)}$ | typ. | 30 | μV |
| Output voltage; 5,5 MHz (r.m.s. value) | $V_{12\text{-}13\,(rms)}$ | typ. | 50 | mV |
| I.F. control range | $\Delta G_v$ | > | 60 | dB |
| Signal-to-weighted-noise ratio according to DIN 45 405 | S + W/W | > | 52 | dB |

## PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).


1st SOUND I.F. & DEMODULATOR
TDA2545
38,9 MHz
9
8
VP
11
VP
4 kΩ
4 kΩ
REF. AMP.
VP
LIMITER-AMPLIFIER
3,3 kΩ
3,3 kΩ
90°
0°
15
860 Ω
3 kΩ
16
i.f. input (1)
1
860 Ω
3 kΩ
2
SIGNAL PROCESSING FOR A.G.C.
3
VP
12
3,3 kΩ
5,5 MHz
13
7Z84654

(1) I.F. signal: vision carrier (V.C.) and sound carrier (S.C.).

Fig. 1 Block diagram.

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | | |
|---|---|---|---|---|
| Supply voltage | $V_{11-13} = V_P$ | max. | 13,2 | V |
| Storage temperature range | $T_{stg}$ | | −25 to +125 | °C |
| Operating ambient temperature range | $T_{amb}$ | | −20 to +75 | °C |

## CHARACTERISTICS

$V_P = 12$ V; $T_{amb} = 25$ °C; measured at $f_{VC} = 38,9$ MHz and $f_{SC} = 33,4$ MHz.

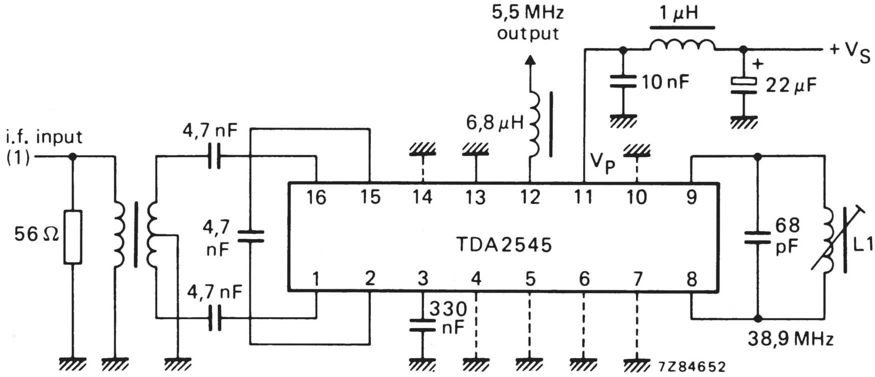
Vision carrier (V.C.) modulated with 2 T/20 T pulses, line-for-line alternating with white bars; modulation depth 100% (proportional to 10% rest-carrier).

Sound carrier (S.C.) modulated with f = 1 kHz and $\Delta f = \pm 50$ kHz.

Vision-to-sound carrier ratio is 13 dB.

For measuring circuit see Fig. 2; unless otherwise specified.

| | | | | |
|---|---|---|---|---|
| Supply voltage range | $V_{11-13} = V_P$ | | 10,8 to 13,2 | V |
| Supply current at $V_{VC1-16(rms)} = 10$ mV | $I_{11} = I_P$ | typ. | 39 | mA |
| Minimum i.f. vision carrier input voltage (r.m.s. value) for a 5,5 MHz output signal $V_{12-13} = 5$ mV | $V_{VC1-16(rms)}$ | < | 100 | µV |
| Maximum input voltage (r.m.s. value) | $V_{VC1-16(rms)}$ | > | 100 | mV |
| Input resistance | $R_{1-16}$ | typ. | 2 | kΩ |
| Input capacitance | $C_{1-16}$ | typ. | 2 | pF |
| I.F. control range | $\Delta G_v$ | > | 60 | dB |
| Signal-to-weighted-noise ratio according to DIN 45 405 measured with TCA420A and $V_{VC1-16(rms)} = 10$ mV | S + W/W | > | 52 | dB |
| Output voltage; 5,5 MHz (r.m.s. value) | | | | |
| at $V_{VC1-16(rms)} = 100$ µV | $V_{12-13(rms)}$ | typ. | 50 | mV |
| at $V_{VC1-16(rms)} = 10$ mV | $V_{12-13(rms)}$ | > | 30 | mV |
| D.C. output voltage | $V_{12-13}$ | typ. | 5,3 | V |
| Allowable load resistance at the output | $R_{12-13}$ | > | 10 | kΩ |
| Control voltage range | $V_{3-13}$ | | 6 to 9 | V |


5,5 MHz output
1 μH
+ V$_S$
10 nF
+
22 μF
6,8 μH
i.f. input (1)
4,7 nF
V$_P$
16
15
14
13
12
11
10
9
56 Ω
4,7 nF
TDA2545
68 pF
L1
1
2
3
4
5
6
7
8
4,7 nF
330 nF
38,9 MHz
7Z84652

(1) I.F. signal: vision carrier (V.C.) and sound carrier (S.C.)

Fig. 2 Measuring circuit for TDA2545.

# QUASI-SPLIT-SOUND CIRCUIT WITH 5,5 MHz DEMODULATION

The TDA2546 is a monolithic integrated circuit for quasi-split-sound processing, including 5,5 MHz demodulation, in television receivers.

The circuit incorporates the following functions:

**1st i.f.** (V.C.: vision carrier plus S.C.: sound carrier)

- 3-stage gain controlled i.f. amplifier
- a.g.c. circuit
- reference amplifier with limiter amplifier for vision carrier (V.C.) processing
- linear multiplier for quadrature demodulation

**2nd i.f.** (5,5 MHz signal)

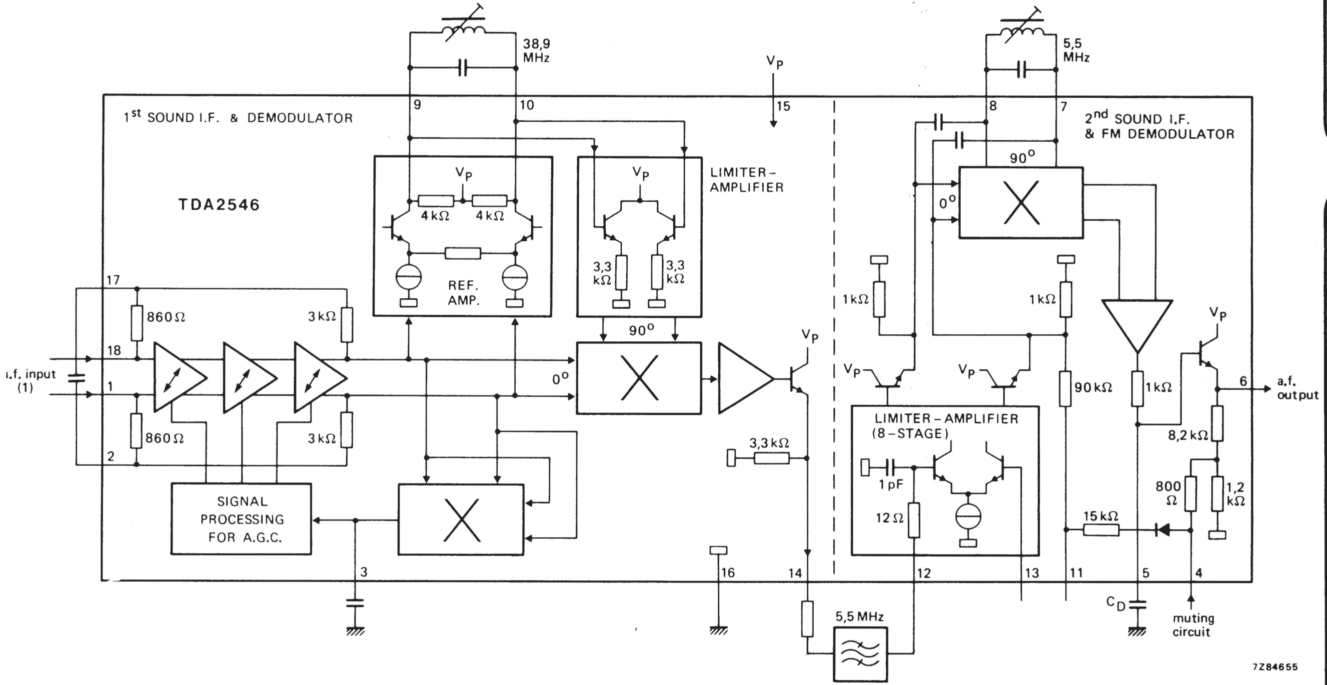
- 8-stage limiter amplifier
- quadrature demodulator
- a.f. amplifier with de-emphasis
- VCR switch

## QUICK REFERENCE DATA

| | | | | |
|---|---|---|---|---|
| Supply voltage | $V_{15\text{-}16} = V_P$ | typ. | 12 | V |
| Minimum i.f. vision carrier input voltage (r.m.s. value) | $V_{VC1\text{-}18(rms)}$ | typ. | 30 | μV |
| Output voltage; 5,5 MHz (r.m.s. value) | $V_{14\text{-}16(rms)}$ | typ. | 50 | mV |
| I.F. control range | $\Delta G_v$ | > | 60 | dB |
| Signal-to-weighted-noise ratio according to DIN 45 405 | S + W/W | > | 50 | dB |
| A.F. output voltage (r.m.s. value) | $V_{o6\text{-}16(rms)}$ | typ. | 1 | V |

## PACKAGE OUTLINE

18-lead DIL; plastic (SOT-102CS).


38,9 MHz
5,5 MHz
VP
9
10
15
8
7
1st SOUND I.F. & DEMODULATOR
2nd SOUND I.F. & FM DEMODULATOR
TDA2546
VP
4 kΩ
4 kΩ
REF. AMP.
VP
3,3 kΩ
3,3 kΩ
LIMITER-AMPLIFIER
90°
0°
90°
0°
17
860 Ω
3 kΩ
18
i.f. input (1)
1
860 Ω
3 kΩ
2
SIGNAL PROCESSING FOR A.G.C.
VP
3,3 kΩ
1 kΩ
1 kΩ
VP
VP
LIMITER-AMPLIFIER (8-STAGE)
1 pF
12 Ω
90 kΩ
1 kΩ
VP
6
a.f. output
8,2 kΩ
800 Ω
1,2 kΩ
15 kΩ
3
16
14
12
13
11
5
4
CD
muting circuit
5,5 MHz
7Z84655

(1) I.F. signal: vision carrier (V.C.) and sound carrier (S.C.)

Fig. 1 Block diagram.

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | | |
|---|---|---|---|---|
| Supply voltage | $V_{15\text{-}16} = V_P$ | max. | 13,2 | V |
| Input current | $I_4$ | max. | 5 | mA |
| Storage temperature range | $T_{stg}$ | | −25 to + 125 | °C |
| Operating ambient temperature range | $T_{amb}$ | | −20 to + 70 | °C |

## CHARACTERISTICS

$V_P = 12$ V; $T_{amb} = 25$ °C; measured at $f_{VC} = 38{,}9$ MHz and $f_{SC} = 33{,}4$ MHz.

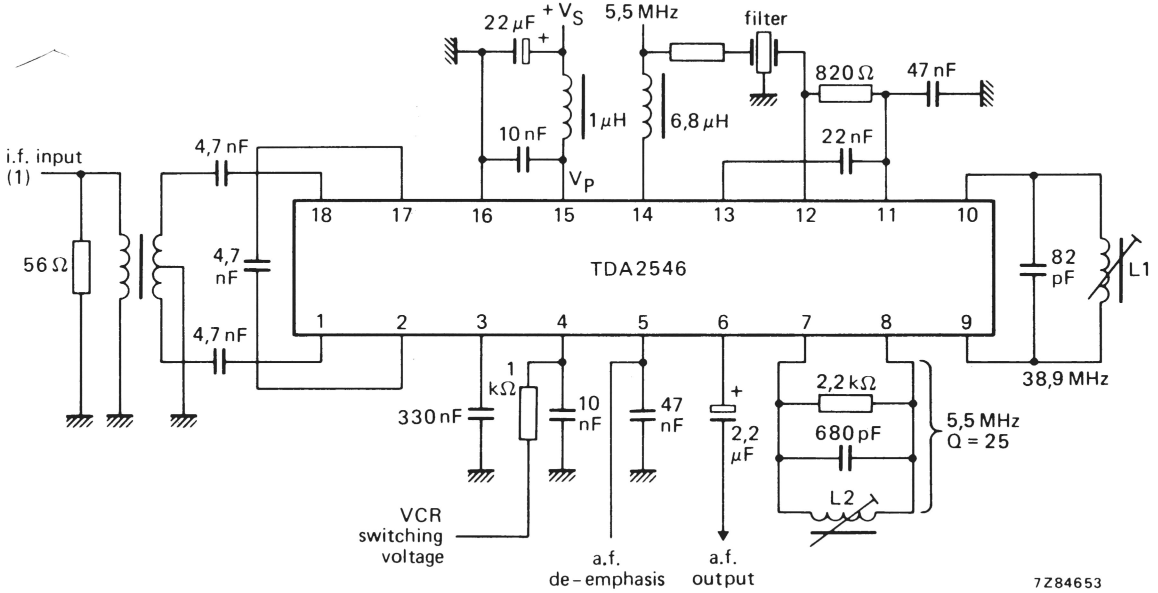
Vision carrier (V.C.) modulated with 2T/20T pulses, line-for-line alternating with white bars; modulation depth 100% (proportional to 10% rest-carrier).

Sound carrier (S.C.) modulated with f = 1 kHz and $\Delta f = \pm 50$ kHz.

Vision-to-sound carrier ratio is 13 dB.

For measuring circuit see Fig. 2; unless otherwise specified.

| | | | | |
|---|---|---|---|---|
| Supply voltage range | $V_{15\text{-}16} = V_P$ | | 10,8 to 13,2 | V |
| Supply current at $V_{VC1\text{-}18(rms)} = 10$ mV | $I_{15} = I_P$ | typ. | 53 | mA |
| Minimum i.f. vision carrier input voltage (r.m.s. value) for $V_{o6\text{-}16(rms)} = 800$ mV | $V_{VC1\text{-}18(rms)}$ | < | 100 | μV |
| Maximum input voltage (r.m.s. value) | $V_{VC1\text{-}18(rms)}$ | > | 100 | mV |
| Input resistance | $R_{1\text{-}18}$ | typ. | 2 | kΩ |
| Input capacitance | $C_{1\text{-}18}$ | typ. | 2 | pF |
| I.F. control range | $\Delta G_v$ | > | 60 | dB |
| Signal-to-weighted-noise ratio according to DIN 45 405 measured with $V_{VC1\text{-}18(rms)} = 10$ mV | S + W/W | > | 50 | dB |
| Output voltage; 5,5 MHz (r.m.s. value) at $V_{VC1\text{-}18(rms)} = 10$ mV | $V_{14\text{-}16(rms)}$ | > | 30 | mV |
| Load resistance (pin 14) | $R_{14\text{-}16}$ | > | 10 | kΩ |
| Control voltage range | $V_{3\text{-}16}$ | | 6 to 9 | V |
| Load resistance (pin 6) | $R_{6\text{-}16}$ | > | 27 | kΩ |
| Internal de-emphasis resistance | $R_{i5\text{-}16}$ | typ. | 1 | kΩ |
| Switching voltage | | | | |
| for mute | $V_{4\text{-}16}$ | > | 4 | V |
| for a.f. on | $V_{4\text{-}16}$ | | 0 to 2,5 | V |
| A.F. output voltage (r.m.s. value) at $V_{VC1\text{-}18(rms)} = 10$ mV | $V_{6\text{-}16(rms)}$ | typ. | 1 | V |


i.f. input
(1)
56 Ω
4,7 nF
4,7
nF
4,7 nF
18
17
16
15
14
13
12
11
10
1
2
3
4
5
6
7
8
9
TDA2546
22 µF
+
+ V_S
10 nF
1 µH
V_P
5,5 MHz
6,8 µH
filter
820 Ω
47 nF
22 nF
82
pF
L1
38,9 MHz
1
kΩ
330 nF
10
nF
47
nF
+
2,2
µF
2,2 kΩ
680 pF
L2
5,5 MHz
Q = 25
VCR
switching
voltage
a.f.
de-emphasis
a.f.
output
7Z84653

(1) I.F. signal: vision carrier (V.C.) and sound carrier (SC).

Fig. 2 Measuring circuit for TDA2546. Coil adjustment procedure: L1 at minimum rest-amplitude modulation, measured at pin 14; L2 at minimum distortion at a.f. output (pin 6).

# TELEVISION I.F. AMPLIFIER AND DEMODULATOR

## GENERAL DESCRIPTION

The TDA2548 is an i.f. amplifier and demodulator circuit for colour and black and white television receivers using p-n-p tuners.
It incorporates the following functions:

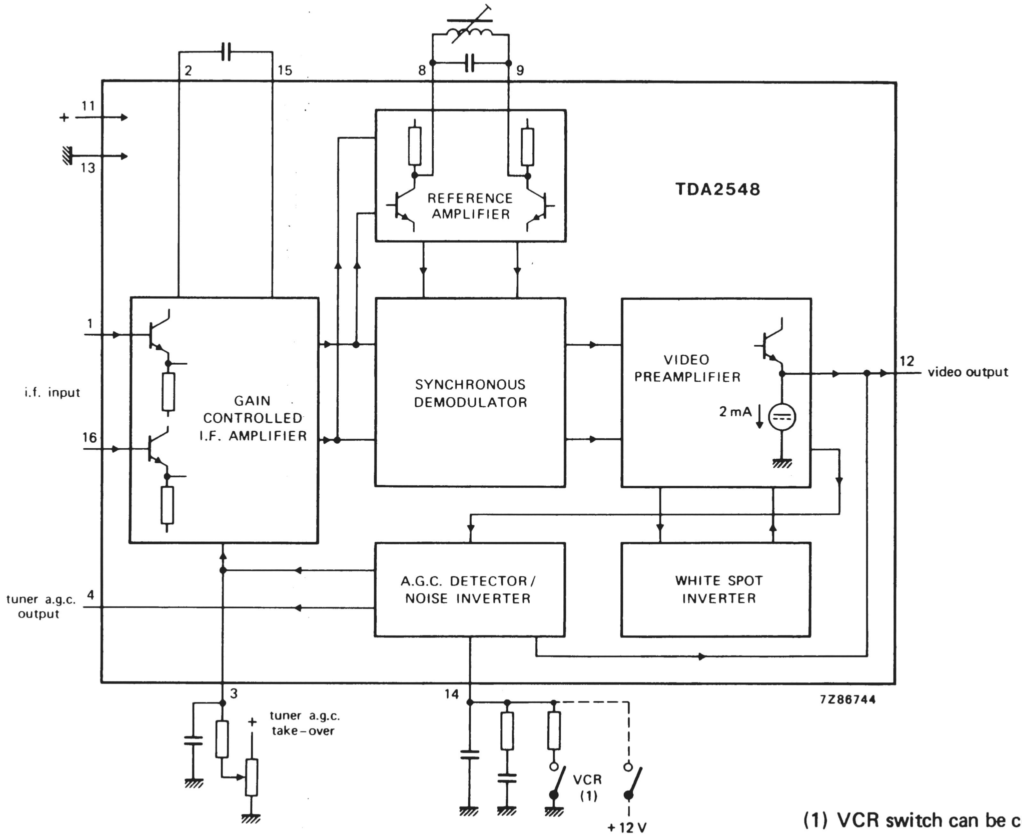
- gain-controlled wide-band amplifier, providing complete i.f. gain
- synchronous demodulator
- white spot inverter
- video preamplifier with noise protection
- a.g.c. circuit with noise gating
- tuner a.g.c. output (p-n-p tuners)
- VCR switch, which switches off the video output; e.g. for insertion of a VCR playback signal.

## QUICK REFERENCE DATA

| | | | | |
|---|---|---|---|---|
| Supply voltage | $V_{11\text{-}13}$ | typ. | 12 | V |
| Supply current | $I_{11}$ | typ. | 50 | mA |
| I.F. input voltage at f = 38,9 MHz (r.m.s. value) | $V_{1\text{-}16(rms)}$ | typ. | 100 | $\mu$V |
| Video output voltage (white at 10% of top sync) | $V_{12(p\text{-}p)}$ | typ. | 2,7 | V |
| I.F. voltage gain control range | $G_v$ | typ. | 64 | dB |
| Signal-to-noise ratio at $V_i$ = 10 mV | S/N | typ. | 58 | dB |

## PACKAGE OUTLINES

TDA2548 : 16-lead DIL; plastic (SOT-38).
TDA2548Q: 16-lead QIL; plastic (SOT-58).


TDA2548
11
+
13
2
15
8
9
1
16
i.f. input
tuner a.g.c.
output
4
GAIN
CONTROLLED
I.F. AMPLIFIER
REFERENCE
AMPLIFIER
SYNCHRONOUS
DEMODULATOR
VIDEO
PREAMPLIFIER
2 mA
12
video output
A.G.C. DETECTOR /
NOISE INVERTER
WHITE SPOT
INVERTER
3
tuner a.g.c.
take-over
+
14
VCR
(1)
+ 12 V
7Z86744

(1) VCR switch can be connected either to ground or to + 12 V.

Fig. 1 Block diagram.

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | | |
|---|---|---|---|---|
| Supply voltage | $V_{11\text{-}13}$ | max. | 13,2 | V |
| Tuner a.g.c. voltage | $V_{4\text{-}13}$ | max. | 12 | V |
| Total power dissipation | $P_{tot}$ | max. | 900 | mW |
| Storage temperature | $T_{stg}$ | | −55 to + 125 | °C |
| Operating ambient temperature | $T_{amb}$ | | −25 to + 60 | °C |

## CHARACTERISTICS (measured in Fig. 5)

| | | | | |
|---|---|---|---|---|
| Supply voltage range | $V_{11\text{-}13}$ | typ. | 12 | V |
| | | | 10,2 to 13,2 | V |

The following characteristics are measured at $T_{amb}$ = 25 °C; $V_{11\text{-}13}$ = 12 V; f = 38,9 MHz

| | | | | |
|---|---|---|---|---|
| I.F. input voltage for onset of a.g.c. (r.m.s. value) | $V_{1\text{-}16(rms)}$ | typ. | 100 | μV |
| | | < | 150 | μV |
| Differential input impedance | $\lvert Z_{1\text{-}16} \rvert$ | typ. | 2 kΩ in parallel with 2 pF | |
| Zero-signal output level | $V_{12\text{-}13}$ | typ. | 6 ± 0,3 | V* |
| Top sync output level | $V_{12\text{-}13}$ | typ. | 3,07 | V |
| | | | 2,9 to 3,2 | V |
| I.F. voltage gain control range | $G_v$ | typ. | 64 | dB |
| Bandwidth of video amplifier (3 dB) | B | typ. | 6 | MHz |
| Signal-to-noise ratio at $V_i$ = 10 mV | S/N | typ. | 58 | dB** |
| Differential gain | dG | typ. | 4 | % |
| | | < | 10 | % |
| Differential phase | dφ | typ. | 2° | |
| | | < | 10° | |

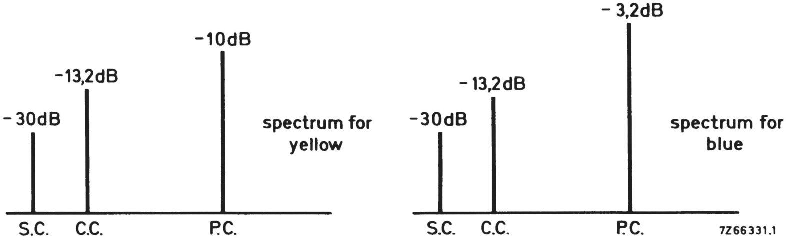
---

* So-called 'projected zero point', e.g. with switched demodulator.

**
$$S/N = \frac{V_o \text{ black-to-white}}{V_{n(rms)} \text{ at } B = 5\text{ MHz}}$$

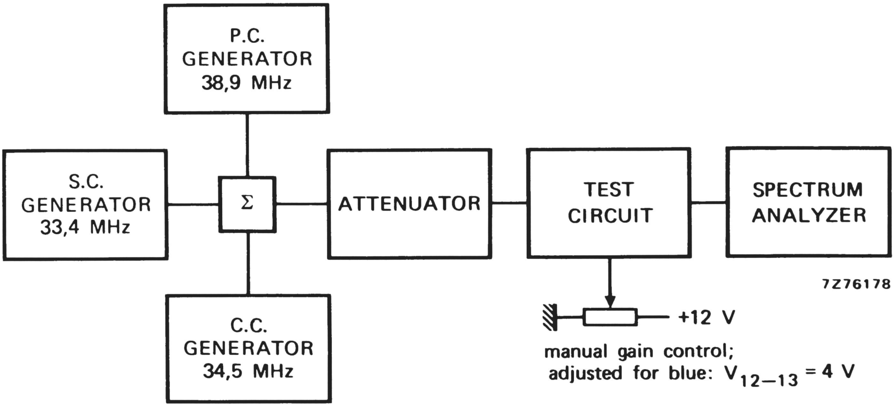
**CHARACTERISTICS** (continued)

| | | | |
|---|---|---|---|
| Intermodulation at 1,1 MHz: blue* | | > | 46 dB |
| | | typ. | 60 dB |
| | yellow* | > | 46 dB |
| | | typ. | 50 dB |
| at 3,3 MHz** | | > | 46 dB |
| | | typ. | 54 dB |



S.C. : sound carrier level
C.C. : chrominance carrier level
P.C. : picture carrier level
with respect to top sync level

Fig. 2 Input conditions for intermodulation measurements; standard colour bar with 75% contrast.


P.C. GENERATOR 38,9 MHz
S.C. GENERATOR 33,4 MHz
Σ
ATTENUATOR
TEST CIRCUIT
SPECTRUM ANALYZER
C.C. GENERATOR 34,5 MHz
7Z76178
+12 V

manual gain control;
adjusted for blue: $V_{12-13} = 4$ V

Fig. 3 Test set-up for intermodulation.

---

* $20 \log \frac{V_o \text{ at } 4,4 \text{ MHz}}{V_o \text{ at } 1,1 \text{ MHz}} + 3,6$ dB.

** $20 \log \frac{V_o \text{ at } 4,4 \text{ MHz}}{V_o \text{ at } 3,3 \text{ MHz}}$

| | | | | |
|---|---|---|---|---|
| Carrier signal at video output | | typ.<br><  | 4<br>30 | mV<br>mV |
| 2nd harmonic of carrier at video output | | typ.<br>< | 20<br>30 | mV<br>mV |
| White spot inverter threshold level (Fig. 4) | | typ. | 6,6 | V |
| White spot insertion level (Fig. 4) | | typ. | 4,7 | V |
| Noise inverter threshold level (Fig. 4) | | typ. | 1,8 | V |
| Noise insertion level (Fig. 4) | | typ. | 3,8 | V |
| External video switch (VCR) switches off the output at: | $V_{14\text{-}13}$ | < | 1,1 | V |

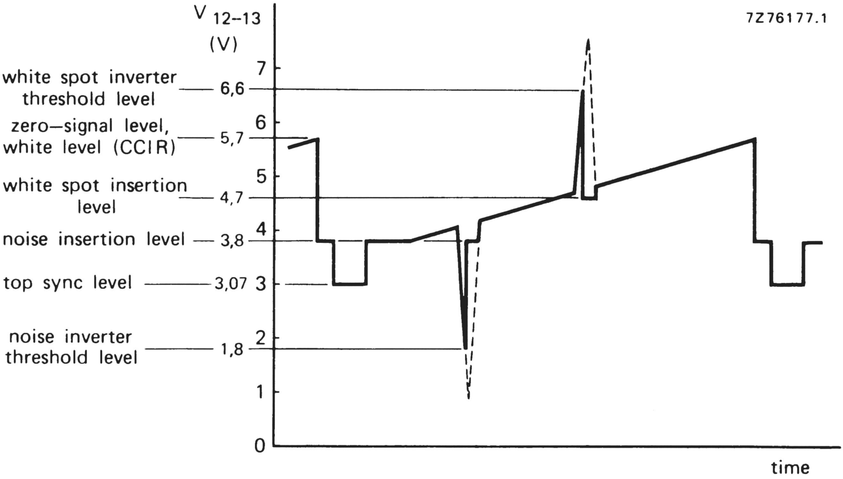


Fig. 4 Video output waveform showing white spot and noise inverter threshold levels.

| | | | | |
|---|---|---|---|---|
| Tuner a.g.c. output current range | $I_4$ | | 0 to 10 | mA |
| Tuner a.g.c. output voltage at $I_4$ = 10 mA | $V_{4\text{-}13}$ | < | 0,3 | V |
| Tuner a.g.c. output leakage current<br>$V_{14\text{-}13}$ = 11 V; $V_{4\text{-}13}$ = 12 V | $I_4$ | < | 15 | $\mu$A |

## APPLICATION INFORMATION

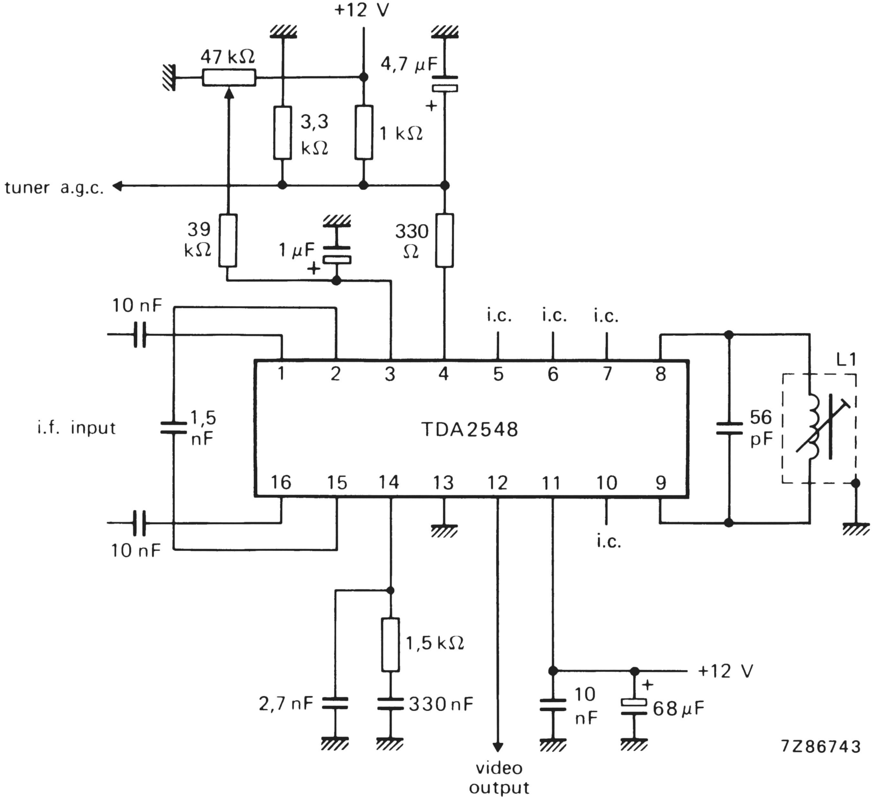

+12 V
47 kΩ
3,3 kΩ
1 kΩ
4,7 μF
+
tuner a.g.c.
39 kΩ
1 μF
+
330 Ω
10 nF
i.c.
i.c.
i.c.
1
2
3
4
5
6
7
8
L1
i.f. input
1,5 nF
TDA2548
56 pF
16
15
14
13
12
11
10
9
10 nF
i.c.
1,5 kΩ
+12 V
2,7 nF
330 nF
10 nF
+
68 μF
7Z86743
video output

Fig. 5 Typical application circuit diagram; Q of L1 ≈ 80; $f_o$ 38,9 MHz.

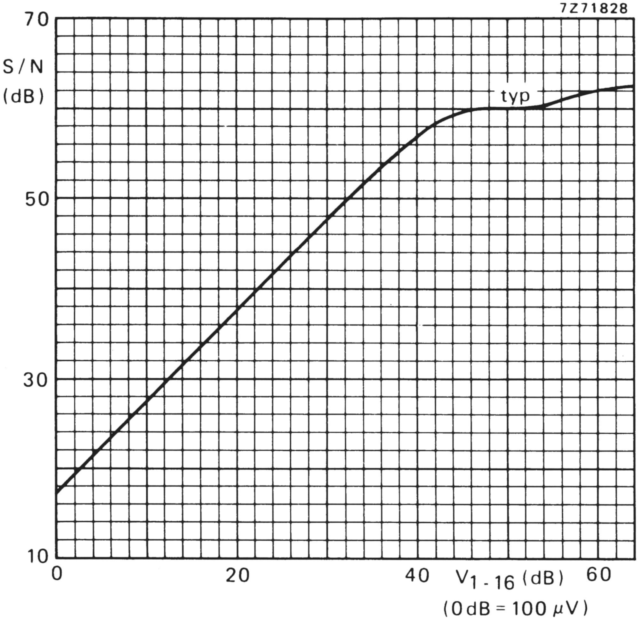


Fig. 6 Signal-to-noise ratio as a function of the input voltage ($V_{1-16}$).

DEVELOPMENT SAMPLE DATA

This information is derived from development samples made available for evaluation. It does not necessarily imply that the device will go into regular production.

# I.F. AMPLIFIER AND DEMODULATOR FOR MULTISTANDARD TV RECEIVERS

The TDA2549 is an i.f. circuit for positive and negative modulation in colour and black and white television receivers. It contains the following functions:

- Gain-controlled wide-band amplifier providing complete i.f. gain
- Synchronous demodulator for positive and negative modulation
- Video preamplifier with noise protection for negative modulation
- Auxiliary video input (1 V) and output (75 Ω)
- Video switch to select between auxiliary video input signal and demodulated video signal
- A.F.C. circuit with on/off switch and inverter switch
- A.G.C. circuit for positive modulation (mean level) and negative modulation (noise gate)
- A tuner a.g.c. output for MOSFET tuners

## QUICK REFERENCE DATA

| | | | | |
|---|---|---|---|---|
| Supply voltage (pins 13 and 21) | $V_{13;21\text{-}3}$ | typ. | 12 | V |
| Supply current (pins 13 and 21) | $I_{13;21}$ | typ. | 80 | mA |
| I.F. input sensitivity (38,9 MHz) (between pins 6 and 7) | $V_{6\text{-}7}$ | typ. | 100 | μV |
| Video output voltage (pin 22) | $V_{22\text{-}3}$ | typ. | 2 | V |
| I.F. voltage gain control range | $G_v$ | typ. | 64 | dB |
| Signal-to-noise ratio at $V_i$ = 10 mV | S/N | typ. | 58 | dB |
| A.F.C. output voltage swing (pin 15) | $V_{15\text{-}3}$ | typ. | 11 | V |
| Tuner a.g.c. output current (pin 10) | $I_{10}$ | min. | 0,3 | mA |
| Video bandwidth | B | typ. | 6 | MHz |
| Auxiliary video input impedance (pin 12) | $\lvert Z_{12\text{-}3}\rvert$ | min. | 10 | kΩ |
| Auxiliary video input voltage (pin 12) | $V_{12\text{-}3}$ | typ. | 1 | V |
| Auxiliary video output impedance (pin 14) | $\lvert Z_{14\text{-}3}\rvert$ | typ. | 7 | Ω |
| Auxiliary video input voltage (pin 14) | $V_{14\text{-}3}$ | typ. | 2 | V |

**A COMPLETE DATA SHEET IS AVAILABLE UPON REQUEST**

# LUMINANCE AND CHROMINANCE CONTROL COMBINATION

The TDA2560 is a monolithic integrated circuit for use in decoding systems of colour television receivers. The circuit consists of a luminance and chrominance amplifier. The luminance amplifier has a low input impedance so that matching of the luminance delay line is very easy.
It also incorporates the following functions:

- d.c. contrast control;
- d.c. brightness control;
- black level clamp;
- blanking;
- additional video output with positive-going sync.

The chrominance amplifier comprises:

- gain controlled amplifier;
- chrominance gain control tracked with contrast control;
- separate d.c. saturation control;
- combined chroma and burst output, burst signal amplitude not affected by contrast and saturation control;
- the delay line can be driven directly by the IC.

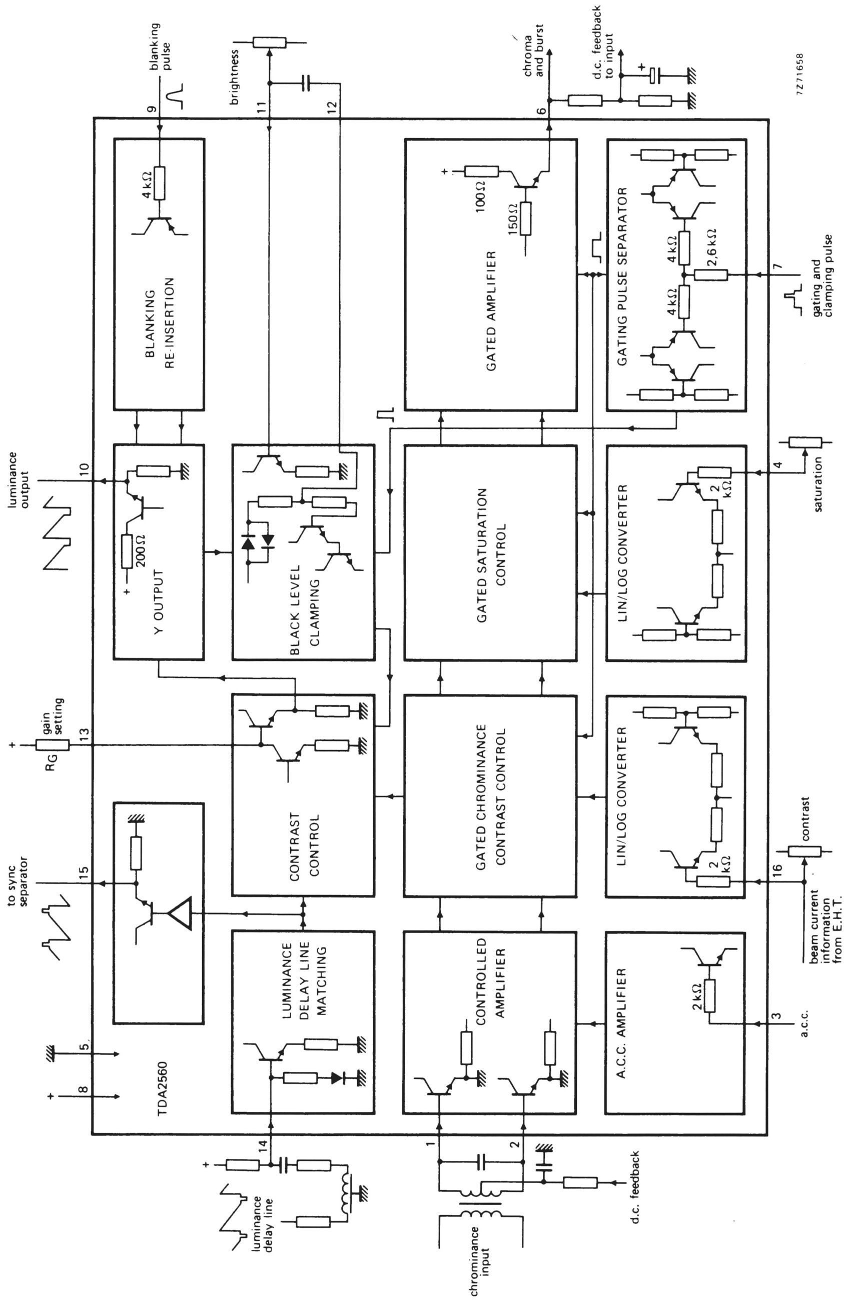
## QUICK REFERENCE DATA

| | | | | |
|---|---|---|---|---|
| Supply voltage | $V_{8-5}$ | typ. | 12 | V |
| Supply current | $I_8$ | typ. | 45 | mA |
| Luminance signal input current (black-to-white value) | $I_{14}$ | typ. | 0,2 | mA |
| Chrominance input signal (peak-to-peak value) | $V_{2-1(p-p)}$ | | 4 to 80 | mV |
| Luminance output signal at nominal contrast (black-to-white value) | $V_{10-5}$ | typ. | 3 | V |
| Chrominance output signal at nominal contrast and saturation and 1,25 V peak-to-peak burst output (peak-to-peak value) | $V_{6-5(p-p)}$ | typ. | 2,5 | V |
| Contrast control range | | > | 20 | dB |
| Saturation control range | | > | 20 | dB |

## PACKAGE OUTLINES

TDA2560 : 16-lead DIL ; plastic (SOT-38).
TDA2560Q: 16-lead QIL ; plastic (SOT-58).

## BLOCK DIAGRAM


blanking pulse
9
brightness
11
12
chroma and burst
6
d.c. feedback to input
+
7Z71658
4 kΩ
BLANKING RE-INSERTION
100Ω
150Ω
GATED AMPLIFIER
4 kΩ
4 kΩ
2,6 kΩ
GATING PULSE SEPARATOR
7
gating and clamping pulse
luminance output
10
+
200Ω
Y OUTPUT
BLACK LEVEL CLAMPING
GATED SATURATION CONTROL
2 kΩ
LIN/LOG CONVERTER
4
saturation
gain setting
RG
+
13
CONTRAST CONTROL
GATED CHROMINANCE CONTRAST CONTROL
LIN/LOG CONVERTER
2 kΩ
16
contrast
beam current information from E.H.T.
to sync separator
15
LUMINANCE DELAY LINE MATCHING
CONTROLLED AMPLIFIER
2 kΩ
A.C.C. AMPLIFIER
3
a.c.c.
5
8
+
TDA2560
14
+
luminance delay line
1
2
chrominance input
d.c. feedback

**RATINGS** Limiting values in accordance with the Absolute Maximum System (IEC134)

| | | | | |
|---|---|---|---|---|
| Voltage | | | | |
| Supply voltage | $V_{8-5}$ | max. | 14 | V |
| Power dissipation | | | | |
| Total power dissipation | $P_{tot}$ | max. | 930 | mW |
| Temperatures | | | | |
| Storage temperature | $T_{stg}$ | | −55 to +125 | °C |
| Operating ambient temperature | $T_{amb}$ | | 0 to +65 | °C |

**CHARACTERISTICS** measured in the circuit on page 7

| | | | | |
|---|---|---|---|---|
| Supply voltage range | $V_{8-5}$ | typ. | 12 | V |
| | | | 10 to 14 | V |
| Supply current | $I_8$ | typ. | 45 | mA 1) |
| Allowable hum on supply line (peak-to-peak value) | $V_{8-5(p-p)}$ | < | 100 | mV |

The following data are measured at $V_{8-5}$ = 12 V; $T_{amb}$ = 25 °C; $R_G$ = 2,7 kΩ

**Luminance amplifier**

| | | | | |
|---|---|---|---|---|
| Input signal current; black-to-white value | $I_{14}$ | typ. | 0,2 | mA |
| Input bias current | $I_{14}$ | typ. | 0,25 | mA |
| Input impedance | $\lvert Z_{14-5}\rvert$ | typ. | 150 | Ω 2) |
| Gain (pin 13) | see note 1 on page 5 | | | |
| Contrast control range | | > | 20 | dB |
| Contrast control voltage range | $V_{16-5}$ (see control curve on page 6) | | | |
| Contrast control current | $I_{16}$ | < | 8 | μA |
| Black level range | $V_{10-5}$ | | 1 to 3 | V |
| Brightness control voltage range | $V_{11-5}$ | typ. | 1 to 3 | V |
| Brightness control current | $I_{11}$ | < | 20 | μA 3) |
| Black level stability when changing temperature | | typ. | 0,1 | mV/°C |
| Black level stability when changing contrast | see page 9 (pin 10) | | | |
| Bandwidth (−3 dB) | B | > | 5 | MHz 4) |

---

1) At a load on pin 6 of 1,5 kΩ, and no load on pins 10 and 15.

2) At an input bias current of 0,25 mA.

3) At $V_{11-5}$ > 4 V.

4) At nominal contrast (max. contrast setting −3 dB).

## CHARACTERISTICS (continued)

| | | | | |
|---|---|---|---|---|
| Output voltage (black-to-white value) | $V_{10-5}$ | typ. | 3 | V |
| Output voltage (additional; positive-going sync) peak-to-peak value | $V_{15-5(p-p)}$ | typ. | 3, 4 | V[1] |
| Black level clamp pulse (see note 2 on page 5) | | | | |
| on level | $V_{7-5}$ | | 7 to $V_{8-5}$ | V |
| off level | $V_{7-5}$ | < | 5 | V |
| Blanking pulse (see note 3 on page 5) | | | | |
| for 0 V on pin 10: on level | $V_{9-5}$ | | 2, 5 to 4, 5 | V |
| off level | $V_{9-5}$ | < | 1, 5 | V |
| for 1, 5 V on pin 10: on level | $V_{9-5}$ | | 6 to $V_{8-5}$ | V |
| off level | $V_{9-5}$ | < | 4, 5 | V |
| **Chrominance amplifier** [2] | | | | |
| Input signal (peak-to-peak value) | $V_{2-1(p-p)}$ | | 4 to 80 | mV |
| Chrominance output signal at nominal contrast and saturation setting (peak-to-peak value) | $V_{6-5(p-p)}$ | typ. | 2 | V[3] |
| Maximum chrominance output signal | $V_{6-5}$ | | 4, 6 | V |
| Bandwidth (−3 dB) | B | typ. | 6 | MHz |
| Ratio of burst and chrominance at nominal contrast and saturation | see notes 4 and 5 on page 5 | | | |
| A.C.C. starting voltage (see note 6 on page 5) | $V_{3-5}$ | typ. | 1, 2 | V |
| A.C.C. range | | > | 30 | dB |
| Tracking between luminance and chrominance with contrast control (10 dB control) | | typ. | ±1 | dB |
| Saturation control range | | > | 20 | dB |
| Saturation control voltage range | $V_{4-5}$ (see control curve on page 6) | | | |
| Gating pulse for chrominance amplifier | | | | |
| on level | $V_{7-5}$ | | 2, 3 to 5 | V |
| off level | $V_{7-5}$ | < | 1 | V |
| width | $t_7$ | > | 8 | μs |
| Signal-to-noise ratio at nominal input voltage | S/N | > | 46 | dB |
| Phase shift between burst and chrominance | | < | $5^{o}$ | |

---

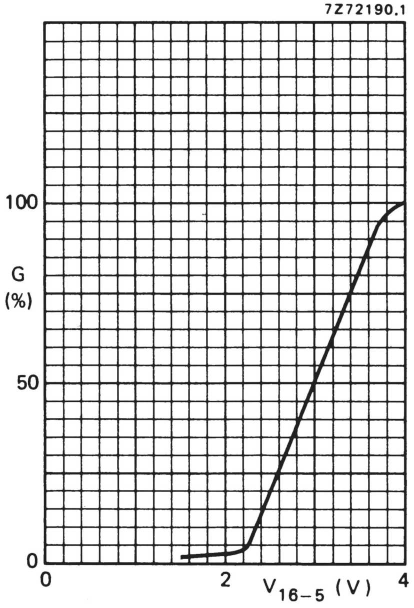
[1] For $I_{14}$ = 0, 2 mA (black-to-white value).

[2] All figures for the chrominance signals are based on a colour bar signal with 75% saturation: i.e. burst-to-chrominance ratio is 1:2.

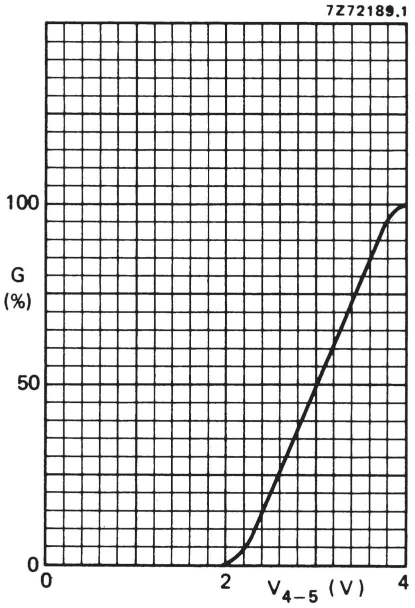
[3] At a burst signal of 1 V peak-to-peak; see also notes 4 and 5 on page 5.

## NOTES

1. The gain of the luminance amplifier can be adjusted, by setting the gain of the contrast control circuit by selection of discrete resistor $R_G$ (see also circuit on page 7). This circuit configuration has been chosen to reduce the spread of the gain to a minimum (main cause of spread is now the spread of the ratio of the delay line matching resistors and the resistor $R_G$). At $R_G$ = 2,7 kΩ the output voltage at nominal contrast (maximum −3 dB) is 3 V black-to-white for an input current of 0,2 mA black-to-white.
2. This pulse (pin 7) is used for gating of the chrominance amplifier and black level clamping. The latter function is actuated at a +7 V level. The input pulse must have such an amplitude that the clamping circuit is active only during the back porch of the blanking interval. The gating pulse switches the gain of the chroma amplifier to maximum during the flyback time, when the pulse rises above 2,3 V and switches it back to normal setting when the pulse falls below 1 V.
3. This pulse (pin 9) is used for blanking the luminance amplifier. When the pulse exceeds the +2,5 V level the output signal is blanked to a level of about 0 V.
   When the input exceeds a +6 V level a fixed level of typ. +1,5 V is inserted in the output signal. This level can be used for clamping purposes.
4. The chrominance and burst signal are both available on this pin (6).
   The burst signal is not affected by the contrast and saturation control and is kept constant by the a.c.c. circuit of the TDA2522.
   The output of the delay line matrix circuit, which is the input of the TDA2522, is thus automatically compensated for the insertion losses. This means that the output signal of the TDA2560 is determined by the insertion losses of the delay line.
   At nominal contrast and saturation setting the ratio of burst to chrominance signal at the output is typically identical to that at the input.
5. Nominal contrast is specified as maximum contrast −3 dB.
   Nominal saturation is specified as maximum saturation −6 dB.
6. A negative-going control voltage gives a decrease in gain.

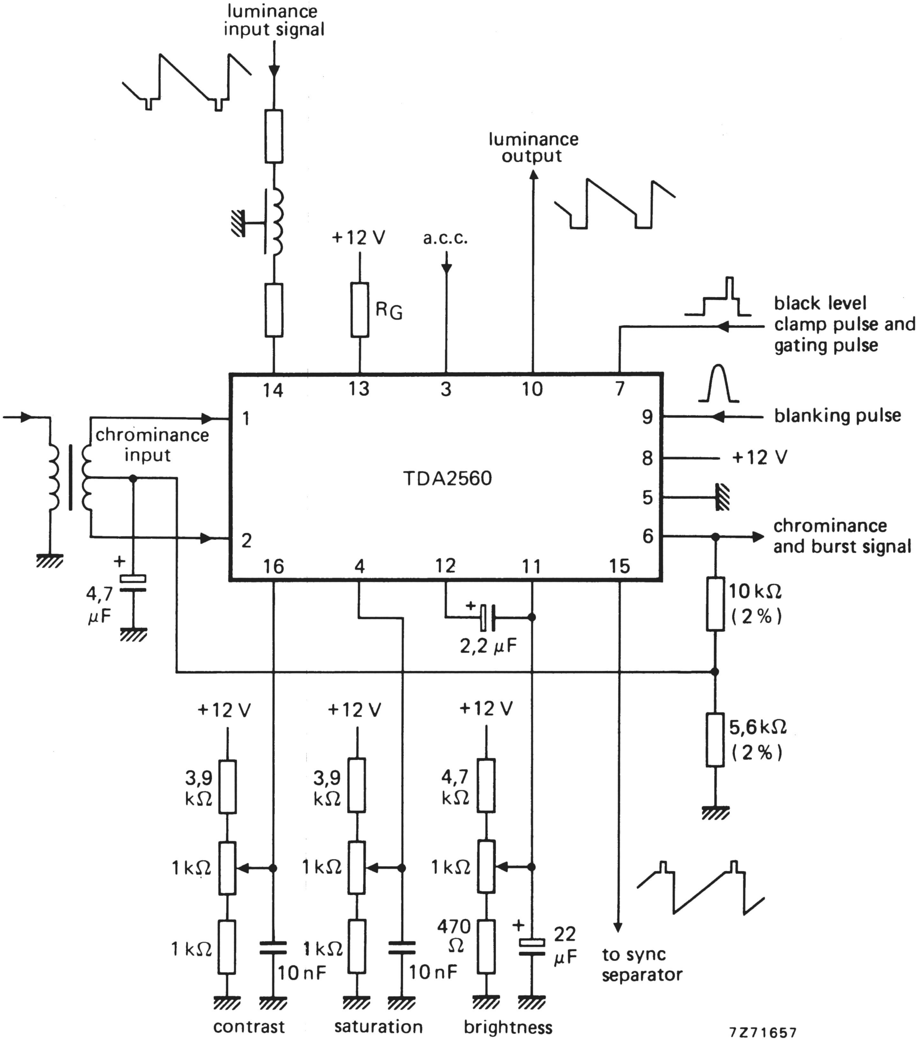


Contrast control of luminance and chrominance amplifier



Saturation control of chrominance amplifier

## APPLICATION INFORMATION


luminance input signal
luminance output
+12 V
RG
a.c.c.
black level clamp pulse and gating pulse
blanking pulse
+12 V
chrominance and burst signal
chrominance input
TDA2560
14
13
3
10
7
1
9
8
5
2
6
16
4
12
11
15
4,7 μF
2,2 μF
10 kΩ (2%)
5,6 kΩ (2%)
+12 V
+12 V
+12 V
3,9 kΩ
3,9 kΩ
4,7 kΩ
1 kΩ
1 kΩ
1 kΩ
1 kΩ
1 kΩ
470 Ω
10 nF
10 nF
22 μF
to sync separator
contrast
saturation
brightness
7Z71657

## APPLICATION INFORMATION (continued)

**The function is quoted against the corresponding pin number**

1. Balanced chrominance input signal (in conjunction with pin 2)

   This is derived from the chrominance signal bandpass filter, designed to provide a push-pull input. A signal amplitude of at least 4 mV peak-to-peak is required between pins 1 and 2. The chrominance amplifier is stabilized by an external feedback loop from the output (pin 6) to the input (pins 1 and 2). The required level at pins 1 and 2 will be 3 V.
   All figures for the chrominance signals are based on a colour bar signal with 75% saturation: i.e. burst-to-chrominance ratio of input signal is 1 : 2.

2. Chrominance signal input (see pin 1)

3. A.C.C. input

   A negative-going potential, starting at +1,2 V, gives a 40 dB range of a.c.c. Maximum gain reduction is achieved at an input voltage of 500 mV.

4. Chrominance saturation control

   A control range of +6 dB to >−14 dB is provided over a range of d.c. potential on pin 4 from +2 to +4 V. The saturation control is a linear function of the control voltage.

5. Negative supply (earth)

6. Chrominance signal output

   For nominal settings of saturation and contrast controls (max. −6 dB for saturation, and max. −3 dB for contrast) both the chroma and burst are available at this pin, and in the same ratio as at the input pins 1 and 2. The burst signal is not affected by the saturation and contrast controls. The a.c.c. circuit of the TDA2522 will hold constant the colour burst amplitude at the input of the TDA2522. As the PAL delay line is situated here between the TDA2560 and TDA2522 there may be some variation of the nominal 1 V peak-to-peak burst output of the TDA2560, according to the tolerances of the delay line. An external network is required from pin 6 of the TDA2560 to provide d.c. negative feedback in the chroma channel via pins 1 and 2.

7. Burst gating and clamping pulse input

   A two-level pulse is required at this pin to be used for burst gate and black level clamping. The black level clamp is activated when the pulse level is greater than 7 V. The timing of this interval should be such that no appreciable encroachment occurs into the sync pulse on picture line periods during normal operation of the receiver. The burst gate, which switches the gain of the chroma amplifier to maximum, requires that the input pulse at pin 7 should be sufficiently wide, at least 8 μs, at the actuating level of 2, 3 V.

**APPLICATION INFORMATION** (continued)

8. +12 V power supply

Correct operation occurs within the range 10 to 14 V. All signal and control levels have a linear dependency on supply voltage but, in any given receiver design, this range may be restricted due to considerations of tracking between the power supply variations and picture contrast and chroma levels.

9. Flyback blanking input waveform

This pin is used for blanking the luminance amplifier. When the input pulse exceeds the +2, 5 V level, the output signal is blanked to a level of about 0 V. When the input exceeds a +6 V level, a fixed level of about 1, 5 V is inserted in the output. This level can be used for clamping purposes.

10. Luminance signal output

An emitter follower provides a low impedance output signal of 3 V black-to-white amplitude at nominal contrast setting having a black level in the range 1 to 3 V. An external emitter load resistor is not required.
The luminance amplitude available for nominal contrast may be modified according to the resistor value from pin 13 to the +12 V supply. At an input bias current $I_{14}$ of 0, 25 mA during black level the amplifier is compensated so that no black level shift more than 10 mV occurs at contrast control. When the input current deviates from the quoted value the black level shift amounts to 100 mV/mA.

11. Brightness control

The black level at the luminance output (pin 10) is identical to the control voltage required at this pin. A range of black level from 1 to 3 V may be obtained.

12. Black level clamp capacitor

13. Luminance gain setting resistor

The gain of the luminance amplifier may be adjusted by selection of the resistor value from pin 13 to +12 V. Nominal luminance output amplitude is then 3 V black-to-white at pin 10 when this resistor is 2, 7 kΩ and the input current is 0, 2 mA black-to-white. Maximum and minimum values of this resistor are 3, 9 kΩ and 1, 8 kΩ.

14. Luminance signal input

A low input impedance in the form of a current sink is obtained at this pin. Nominal input current is 0, 2 mA black-to-white. The luminance signal may be coupled to pin 14 via a d.c. blocking capacitor and, in addition, a resistor employed to give a d.c. current into pin 14 at black level of about 0, 25 mA. Alternatively d.c. coupling from a signal source such as the TDA2540 and TDA2541 may be employed.

APPLICATION INFORMATION (continued)

15. Luminance signal output for sync separator purposes

A luminance signal output with positive-going sync is available which is not affected by the contrast control or the value of resistor at pin 13. This voltage is intended for drive of sync separator circuits. The output amplitude is 3, 4 V peak-to-peak when the luminance signal input is 0, 2 mA black-to-white.

16. Contrast control

With 3 V on this pin the gain of the luminance channel is such that 0, 2 mA black-to-white at pin 14 gives a luminance output on pin 10 of 3 V black-to-white. The nominal value of 2, 7 kΩ is then assumed for the resistor from pin 13 to the +12 V supply. The variation of control potential at pin 16 from 2 to 4 V gives −17 to +3 dB gain variation of the luminance channel. A similar variation in the chrominance channel occurs in order to provide correct tracking between the two signals.

# HORIZONTAL SYNCHRONIZATION AND VERTICAL 625 DIVIDER SYSTEM

The TDA2571A is designed in combination with the TDA2581 as a matched pair for switched-mode driven horizontal deflection stages. When supplied with a composite video signal the TDA2571A delivers drive pulses for the TDA2581 and sync pulses for the vertical deflection. The circuit is optimized for a horizontal and vertical frequency ratio of 625.

The circuit incorporates the following functions:
- Horizontal sync separator with sliding bias in such a way that the sync pulse is always sliced between top-sync level and blanking level.
- Noise gate.
- Horizontal phase detector switching to a small time constant during catching. The phase detector is gated when the oscillator is synchronized.
- Horizontal oscillator (31,25 kHz).
- Burst-key pulse generator. This pulse can also be applied as black level clamp pulse.
- Vertical sync pulse separator.
- Automatic vertical synchronization (625 divider system), without delay after channel change.

## QUICK REFERENCE DATA

| | | | | |
|---|---|---|---|---|
| Supply voltage | | | | |
| horizontal | $V_{12\text{-}11}$ | typ. | 12 | V |
| vertical | $V_{16\text{-}11}$ | typ. | 12 | V |
| Sync input voltage (peak-to-peak value) | $V_{2\text{-}11(p\text{-}p)}$ | | 0,07 to 1 | V |
| Slicing level | | typ. | 50 | % |
| Control sensitivity of horizontal PLL | | typ. | 2000 | Hz/µs |
| Holding range | Δf | typ. | ± 1000 | Hz |
| Catching range | Δf | typ. | ± 900 | Hz |
| Horizontal output pulse (peak-to-peak value) | $V_{8\text{-}11(p\text{-}p)}$ | typ. | 11 | V |
| Vertical sync output pulse (peak-to-peak value) | $V_{1\text{-}11(p\text{-}p)}$ | typ. | 11 | V |
| Burst-key output pulse (peak-to-peak value) | $V_{13\text{-}11(p\text{-}p)}$ | typ. | 11 | V |

## PACKAGE OUTLINES

TDA2571A: 16 lead DIL; plastic (SOT-38).
TDA2571AQ: 16-lead QIL; plastic (SOT-58).

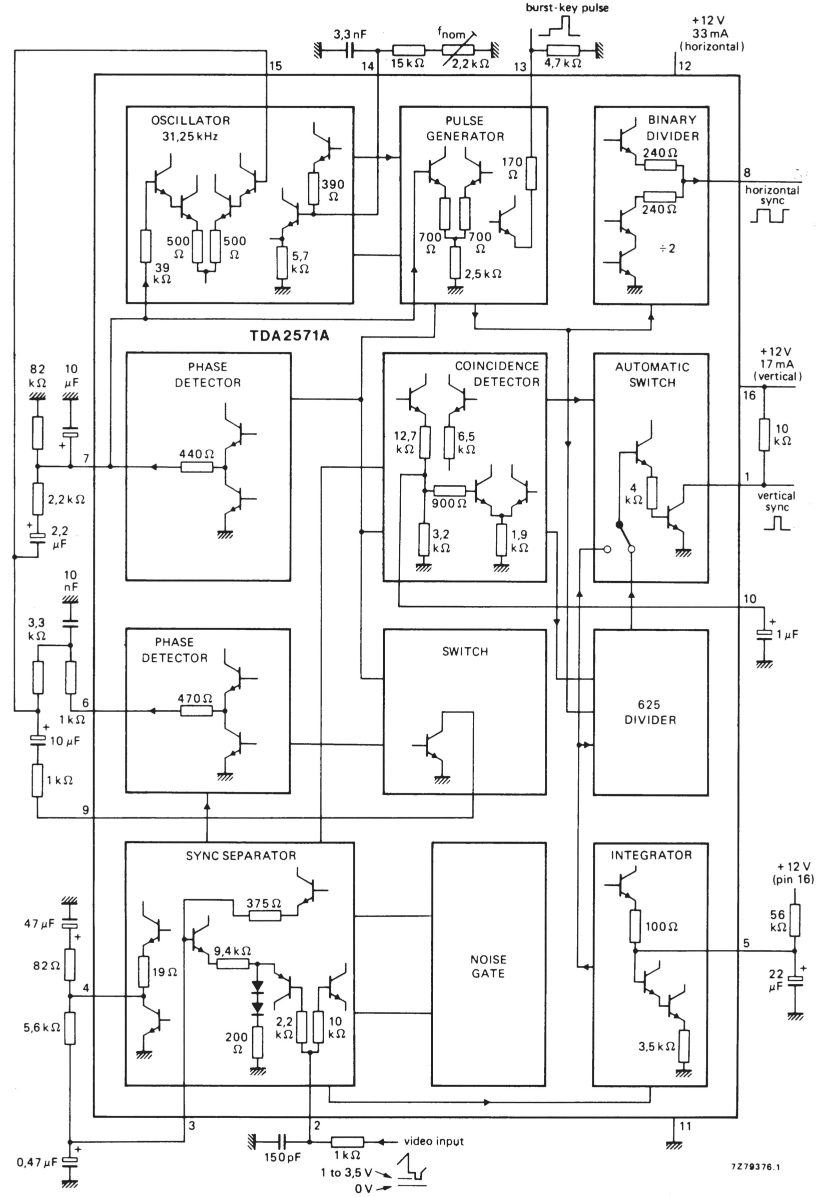

burst-key pulse
3,3 nF
f_nom
15 kΩ
2,2 kΩ
4,7 kΩ
+12 V
33 mA
(horizontal)
15
14
13
12
OSCILLATOR
31,25 kHz
500 Ω
500 Ω
39 kΩ
390 Ω
5,7 kΩ
PULSE
GENERATOR
170 Ω
700 Ω
700 Ω
2,5 kΩ
BINARY
DIVIDER
240 Ω
240 Ω
÷2
8
horizontal
sync
TDA2571A
82 kΩ
10 µF
7
2,2 kΩ
2,2 µF
PHASE
DETECTOR
440 Ω
COINCIDENCE
DETECTOR
12,7 kΩ
6,5 kΩ
900 Ω
3,2 kΩ
1,9 kΩ
AUTOMATIC
SWITCH
4 kΩ
+12 V
17 mA
(vertical)
16
10 kΩ
1
vertical
sync
10
1 µF
10 nF
3,3 kΩ
6
1 kΩ
10 µF
1 kΩ
9
PHASE
DETECTOR
470 Ω
SWITCH
625
DIVIDER
SYNC SEPARATOR
375 Ω
9,4 kΩ
19 Ω
200 Ω
2,2 kΩ
10 kΩ
NOISE
GATE
INTEGRATOR
100 Ω
3,5 kΩ
+12 V
(pin 16)
56 kΩ
5
22 µF
47 µF
82 Ω
4
5,6 kΩ
3
2
11
0,47 µF
150 pF
1 kΩ
video input
1 to 3,5 V
0 V
7Z79376.1

Fig. 1 Block diagram.

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | | |
|---|---|---|---|---|
| Sypply voltage | | | | |
| horizontal | $V_{12\text{-}11}$ | max. | 13,2 | V |
| vertical | $V_{16\text{-}11}$ | max. | 13,2 | V |
| Total power dissipation | $P_{tot}$ | max. | 1 | W |
| Storage temperature | $T_{stg}$ | | −25 to + 130 | °C |
| Operating ambient temperature | $T_{amb}$ | | −25 to + 65 | °C |

## CHARACTERISTICS

At $V_{12\text{-}11} = 12$ V; $V_{16\text{-}11} = 12$ V; $T_{amb} = 25$ °C; measured in Fig. 1

| | | | | |
|---|---|---|---|---|
| Supply voltage range (pins 12 and 16) | $V_{12\text{-}11}$; $V_{16\text{-}11}$ | typ. | 12 | V |
| | | | 10 to 13,2 | V |
| Current consumption | $I_{12} + I_{16}$ | typ. | 50 | mA |
| | | < | 75 | mA |

**Sync separator and noise gate**

| | | | | |
|---|---|---|---|---|
| Sync pulse amplitude (negative going) peak-to-peak value | $V_{2\text{-}11(p\text{-}p)}$ | | 0,07 to 1 | V* |
| Top-sync level | $V_{2\text{-}11}$ | | 1,0 to 3,5 | V |
| Slicing level | | typ. | 50 | %** |
| Slicing level noise gating | $V_{2\text{-}11}$ | typ. | 0,7 | V |

**Phase locked loop**

| | | | | |
|---|---|---|---|---|
| Holding range | $\Delta f$ | typ. | ± 1000 | Hz |
| Catching range | $\Delta f$ | typ. | ± 900 | Hz |
| Control sensitivity of horizontal PLL | | typ. | 2000 | Hz/µs |
| Control sensitivity of phase detector | | typ. | 1,2 | V/µs |
| Delay between sync input and detector output (pin 6) | $t_d$ | typ. | 0,4 | µs |
| Phase modulation due to hum on the supply line | | typ. | 2,0 | µs/V▲ |

---

* Up to 1 V peak-to-peak the slicing level is constant; at amplitudes exceeding 1 V peak-to-peak the slicing level will increase.

** The slicing level is defined as the ratio of the amplitude of the slicing level to black level to the amplitude of the sync pulse.

▲ The voltage is a peak-to-peak value; the figure given can be reduced to 0,6 µs/V(p-p) by means of an extra capacitor of 330 nF between pins 12 and 7.

## CHARACTERISTICS (continued)

**Horizontal oscillator**

| | | | | |
|---|---|---|---|---|
| Frequency; free running | $f_o$ | typ. | 31,250 | kHz |
| Frequency at output pin 8 | $f_8$ | typ. | 15,625 | kHz |
| Spread of frequency without spread of external components | $\Delta f_o$ | < | 4 | % |
| Temperature coefficient | T | typ. | $2,5 \times 10^{-4}$ | $K^{-1}$ |
| Change of frequency when $V_{12-11}$ drops to 6 V | $\Delta f_o$ | < | 10 | % |
| Change of frequency when $V_{12-11}$ increases from 10 to 13,2 V | $\Delta f_o$ | < | 0,5 | % |
| Output voltage; no load (peak-to-peak value) | $V_{8-11(p-p)}$ | > | 10 | V |
| Output resistance | $R_{8-11}$ | typ. | 300 | Ω |
| Output current range (peak-to-peak value) | $I_{8(p-p)}$ | | 0 to 40 | mA |
| Duty factor of output pulse | $\delta$ | typ. | 46 | %* |
| Delay between falling edge of output pulse and end of sync pulse at pin 2 | $t_d$ | typ. | 0,9 | μs** |

**Burst-key pulse**

| | | | | |
|---|---|---|---|---|
| Output voltage (peak-to-peak value) | $V_{13-11(p-p)}$ | > | 10 | V |
| Duration of upper part of output pulse | $t_p$ | typ. | 3,6 | μs** |
| Duration of lower part of output pulse | $t_p$ | typ. | 9,1 | μs** |
| Amplitude of lower part of output pulse | $V_{13-11(p-p)}$ | typ. | 3 | V** |
| Output resistance | $R_{13-11}$ | typ. | 200 | Ω |
| Delay between the end of the sync pulse at pin 2 and the rising edge of the burst key pulse | $t_d$ | typ. | 0,9 | μs** |

**Coincidence detector**

| | | | | |
|---|---|---|---|---|
| Voltage level of time constant switch | $V_{10-11}$ | typ. | 2,0 | V |
| Voltage when the oscillator is in sync | $V_{10-11}$ | typ. | 0,4 | V |
| Voltage when the oscillator is out-of-sync | $V_{10-11}$ | typ. | 2,5 | V |
| Voltage during noise | $V_{10-11}$ | typ. | 1,0 | V |

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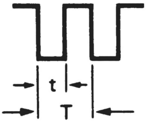
* The duty factor is specified as follows:



$$\delta = \frac{t}{T} \times 100\%.$$

** See waveforms Fig. 2.

**Vertical sync pulse**

| | | | |
|---|---|---|---|
| Output voltage (peak-to-peak value) | $V_{1\text{-}11(p\text{-}p)}$ | > | 10 V |
| Duration of output pulse during indirect synchronization | $t_p$ | typ. | 170 μs |
| Duration of output pulse during direct synchronization (coincidence detector high) | $t_p$ | typ. | 160 μs |
| Load resistor to pin 2 | $R_L$ | > | 2 kΩ |
| Output voltage low with $R_L$ = 2 kΩ | $V_{1\text{-}11}$ | < | 500 mV |
| Ratio between basic horizontal oscillator frequency and vertical pulse | | | 625 * |

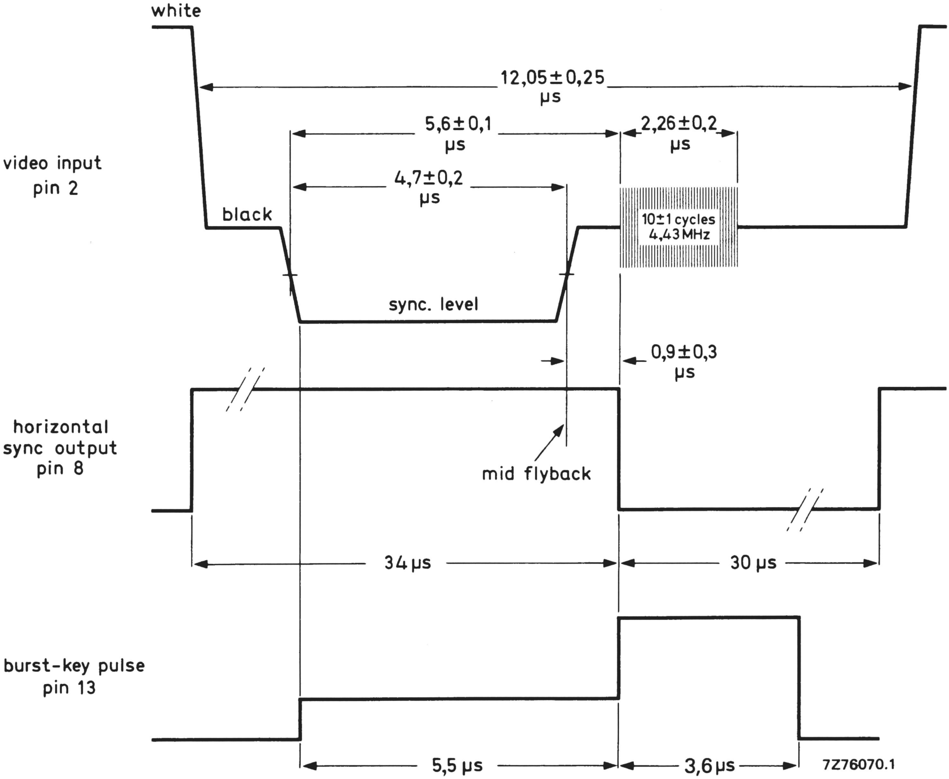

white
12,05±0,25 μs
5,6±0,1 μs
2,26±0,2 μs
4,7±0,2 μs
video input pin 2
black
10±1 cycles 4,43 MHz
sync. level
0,9±0,3 μs
horizontal sync output pin 8
mid flyback
34 μs
30 μs
burst-key pulse pin 13
5,5 μs
3,6 μs
7Z76070.1

Fig. 2 Relationship between the video input signal to the TDA2571A and the horizontal sync and burst-key pulse output.

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* When a non-standard sync signal is applied the separated vertical sync pulse of the incoming signal is connected to pin 1; the pulse of the divider circuit is switched off.

## PINNING

1. Vertical sync pulse output
2. Video input
3. Sync separator slicing level output
4. Black level detector output
5. Vertical integrator bias network
6. Horizontal phase detector output
7. Reference voltage horizontal frequency control stage
8. Horizontal sync pulse output
9. Time constant switch
10. Coincidence detector output
11. Negative supply (ground)
12. Positive supply (horizontal)
13. Burst-key pulse output
14. RC-network horizontal oscillator
15. Control horizontal oscillator
16. Positive supply (vertical)

## APPLICATION INFORMATION

**The function is quoted against the corresponding pin number**

1. Vertical sync pulse output

   A resistor of about 10 kΩ must be connected between pin 1 and the positive supply line (pin 16; vertical supply).

   The output pulse will come from the 625 divider stage (standard signal) or from the vertical sync pulse separator (non-standard signal), depending on the input signal on pin 2. The standard and non-standard signals are detected automatically.

2. Video input

   The input signal must have negative-going sync pulses. The top-sync level can vary between 1 V and 3,5 V without affecting the sync separator operation.

   The slicing level of the sync separator is fixed at 50%, for the sync pulse amplitude range 0,07 to 1 V. As a consequence the circuit gives a good sync separation down to pulses with an amplitude of 70 mV peak-to-peak (sync pulse compression). For sync pulses in excess of 1 V peak-to-peak the slicing level will increase.

   The noise gate is activated at an input level $< 0,7$ V, thus, when noise gating is required the top-sync level should be chosen close to the minimum level of 1 V. When i.f. circuits with a noise gate are used (e.g. TDA2540; TDA2541) the noise gate of the TDA2571A is not required.

3. Sync separator slicing level output

   The sync separator slicing level is determined on this pin. A slicing level of 50% is obtained by comparing this level with the black level of the video signal, which is detected at pin 4. The capacitor connected to pin 3 must be about 0,47 μF.

4. Black level detector output

   The black level of the input signal is detected on this pin, which is required to obtain good sync separator operation. A capacitor of 47 μF in series with a resistor of 82 Ω has to be connected to this pin. A 5,6 kΩ resistor must be connected between pins 3 and 4.

5. Vertical sync pulse integrator bias network

   The vertical sync pulse is obtained by integrating the composite sync signal in an internal RC-network. An external RC-network is required for the correct biasing of this circuit for various input conditions. Typical values are: R = 56 kΩ; C = 22 μF.

6. Horizontal phase detector output

   The control voltage for the horizontal oscillator is obtained on this pin. The output current is about 2 mA.

7. Reference voltage horizontal frequency control stage

This pin has two functions. It is used to decouple the reference voltage for the frequency control of the horizontal oscillator (so a good suppression of interference is obtained which may be present on the supply line). This pin is also used to control the reference waveform for the phase detector to the middle of the gating, giving a good noise immunity of the synchronization.

8. Horizontal sync pulse output

This pulse is obtained from the horizontal oscillator via a divider circuit. The duty factor is 46%. The falling edge of this pulse has a delay of 0,9 μs with respect to the end of the sync pulse. Because of this phase relationship this pulse can directly drive the TDA2581.

9. Time constant switch

This pin is used to switch the time constant of the flywheel filter. The pin condition is determined by the coincidence detector (pin 10). During in-sync or when only noise is received pin 9 assumes ground level, which results in a long time constant and good noise immunity.

During out-of-sync or VCR playback, pin 9 has a high impedance and consequently only the short time constant is available. In this condition a large catching range is obtained.

10. Coincidence detector output

A 1 μF capacitor must be connected to this pin. The output voltage depends on the oscillator condition (synchronized or not) and on the video input signal.
The following output voltages can occur:

| | |
|---|---|
| — when in-sync: | 0,4 V |
| — when out-of-sync: | 2,0 V |
| — during noise at input: | 1,0 V |

When the output voltage < 1,85 V, the flywheel filter is switched to a long time constant, and the gating of the phase detector is switched-on.

For a voltage > 1,85 V, the flywheel filter has a short time constant, and the gating of the phase detector is switched-off. The result is that during noise the flywheel time constant remains long thus preventing large shifts in the frequency of the horizontal oscillator (and screening of the horizontal output transformer).

The information of the line coincidence detector is fed to the divider circuit so that there is no delay in vertical synchronization after a channel change, or an unsynchronized camera change in the studio. Thus, the divider circuit is reset to direct sync, when line synchronization is lost.

The time constant value can be switched manually by a resistor (10 kΩ) to + 12 V.

11. Negative supply (ground)

12. Positive supply horizontal oscillator

Interference and hum on this supply line can affect the oscillator frequency. It is therefore necessary to have a separate decoupling of this pin with respect to pin 16. The current-draw of this pin is typically 33 mA.

13. Burst-key pulse output

This pulse is composed of two parts. The lower part has an amplitude of 3 V peak-to-peak and a width of 9,1 μs (for phase relation see Fig. 2). The upper part has a total amplitude in excess of 10 V peak-to-peak and a width of 3,6 μs. The leading edge of this pulse has a delay of 0,9 μs with respect to the falling edge of the sync pulse at the input (pin 2).

This pulse can directly drive the burst gate/black level clamp input of the TDA2560.

**APPLICATION INFORMATION** (continued)

14. RC-network horizontal oscillator

    Stable components should be chosen for good frequency stability. For adjusting the frequency a part of the total resistance must be variable. This part should be as small as possible, because of poor stability of variable carbon resistors.

    The oscillator can be adjusted when pins 7 and 15 are short-circuited.

15. Horizontal oscillator control pin

16. Positive supply sync separator and divider circuit (vertical)

    For this supply only a simple decoupling is required. The current-draw of this pin is typically 17 mA.

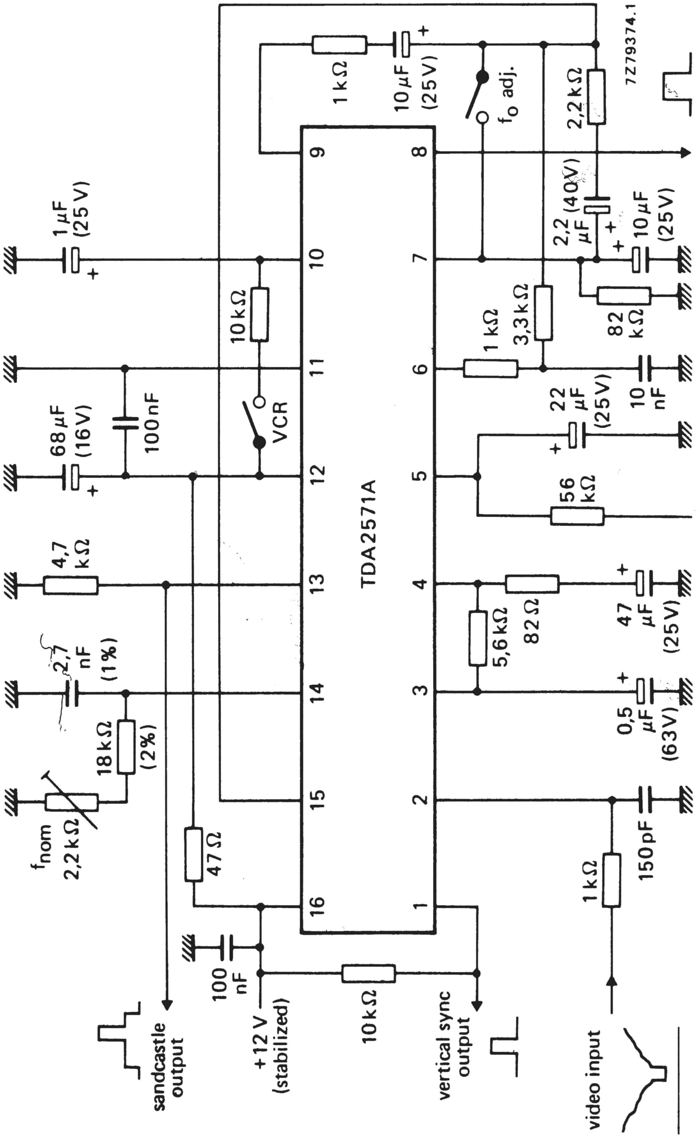

TDA2571A
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
1 kΩ
10 μF (25 V)
+
fo adj.
2,2 kΩ
7Z79374.1
horizontal sync output (to pin 3 TDA2581)
2,2 μF (40 V)
10 μF (25 V)
82 kΩ
3,3 kΩ
1 kΩ
10 nF
22 μF (25 V)
56 kΩ
+12 V (pin 16)
82 Ω
5,6 kΩ
47 μF (25 V)
0,5 μF (63V)
150 pF
1 kΩ
video input
vertical sync output
10 kΩ
+12 V (stabilized)
100 nF
sandcastle output
47 Ω
fnom 2,2 kΩ
18 kΩ (2%)
2,7 nF (1%)
4,7 kΩ
68 μF (16V)
100 nF
VCR
10 kΩ
1 μF (25 V)

Fig. 3 Typical application circuit diagram; for combination of the TDA2571A with the TDA2581 see Fig. 4.

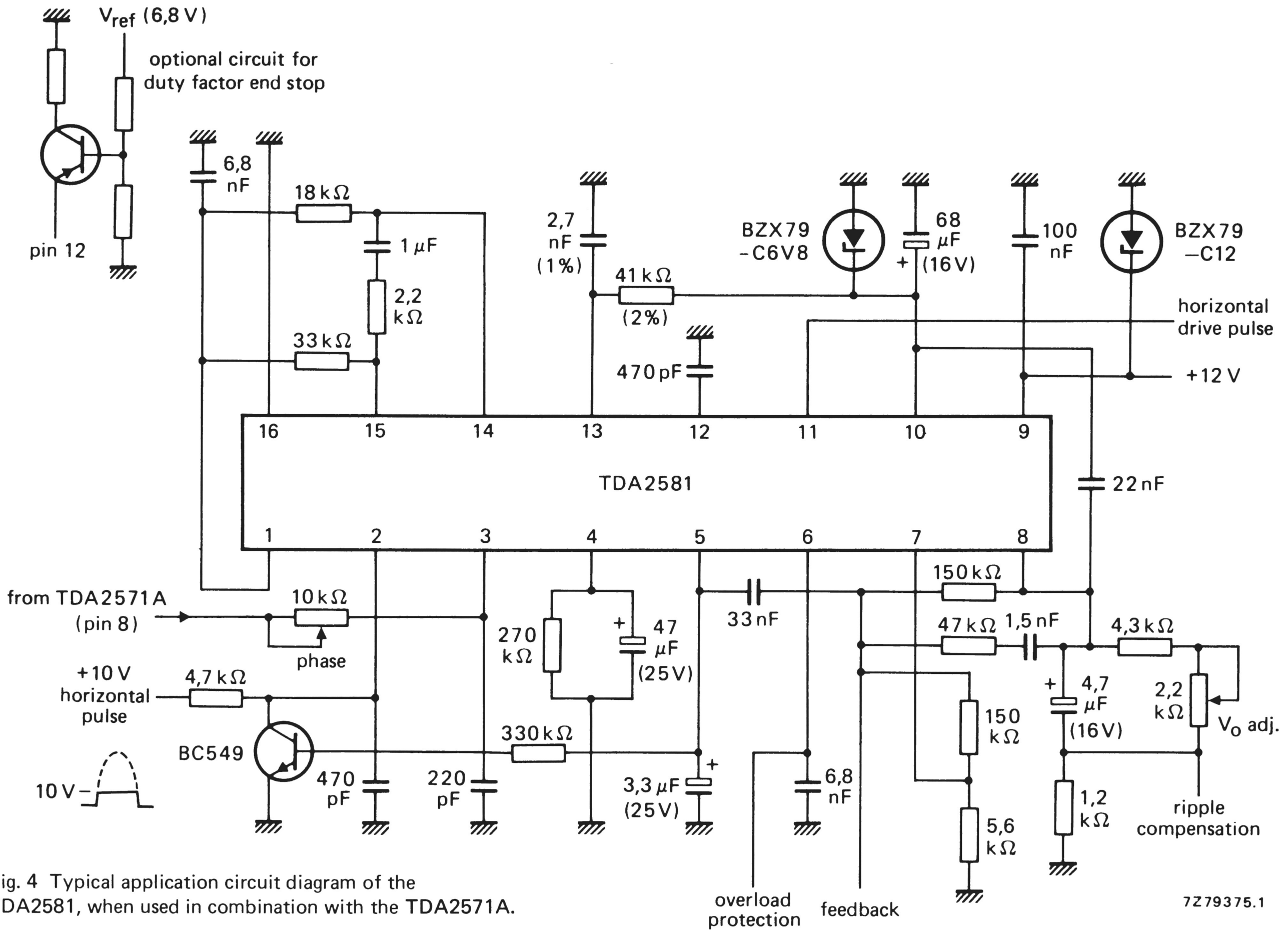

V$_{ref}$ (6,8 V)
optional circuit for duty factor end stop
pin 12
6,8 nF
18 kΩ
1 μF
2,2 kΩ
33 kΩ
2,7 nF (1%)
41 kΩ (2%)
470 pF
BZX79 -C6V8
68 μF (16 V)
100 nF
BZX79 —C12
horizontal drive pulse
+12 V
16
15
14
13
12
11
10
9
TDA2581
22 nF
1
2
3
4
5
6
7
8
from TDA2571A (pin 8)
10 kΩ
phase
+10 V horizontal pulse
4,7 kΩ
BC549
10 V
470 pF
220 pF
270 kΩ
47 μF (25 V)
330 kΩ
3,3 μF (25 V)
33 nF
6,8 nF
150 kΩ
47 kΩ
1,5 nF
4,3 kΩ
150 kΩ
5,6 kΩ
4,7 μF (16 V)
1,2 kΩ
2,2 kΩ
V$_o$ adj.
ripple compensation
overload protection
feedback
7Z79375.1

Fig. 4 Typical application circuit diagram of the TDA2581, when used in combination with the TDA2571A.

# HORIZONTAL SYNCHRONIZATION AND VERTICAL 525 DIVIDER SYSTEM

The TDA2575A is designed in combination with the TDA2581 as a matched pair for switched-mode driven horizontal deflection stages. When supplied with a composite video signal the TDA2575A delivers drive pulses for the TDA2581 and sync pulses for the vertical deflection. The circuit is optimized for a horizontal and vertical frequency ratio of 525.

The circuit incorporates the following functions:

- Horizontal sync separator with sliding bias in such a way that the sync pulse is always sliced between top-sync level and blanking level.
- Noise gate.
- Horizontal phase detector switching to a small time constant during catching. The phase detector is gated when the oscillator is synchronized.
- Horizontal oscillator (31,5 kHz).
- Burst-key pulse generator. This pulse can also be applied as black level clamp pulse.
- Vertical sync pulse separator.
- Automatic vertical synchronization (525 divider system), without delay after channel change.

## QUICK REFERENCE DATA

| | | | | |
|---|---|---|---|---|
| Supply voltage | | | | |
| horizontal | $V_{12\text{-}11}$ | typ. | 12 | V |
| vertical | $V_{16\text{-}11}$ | typ. | 12 | V |
| Sync input voltage (peak-to-peak value) | $V_{2\text{-}11(p\text{-}p)}$ | | 0,07 to 1 | V |
| Slicing level | | typ. | 50 | % |
| Control sensitivity of horizontal PLL | | typ. | 2000 | Hz/μs |
| Holding range | Δf | typ. | ± 1000 | Hz |
| Catching range | Δf | typ. | ± 900 | Hz |
| Horizontal output pulse (peak-to-peak value) | $V_{8\text{-}11(p\text{-}p)}$ | typ. | 11 | V |
| Vertical sync output pulse (peak-to-peak value) | $V_{1\text{-}11(p\text{-}p)}$ | typ. | 11 | V |
| Burst-key output pulse (peak-to-peak value) | $V_{13\text{-}11(p\text{-}p)}$ | typ. | 11 | V |

## PACKAGE OUTLINES

TDA2575A : 16-lead DIL; plastic (SOT-38).
TDA2575AQ: 16-lead QIL; plastic (SOT-58).

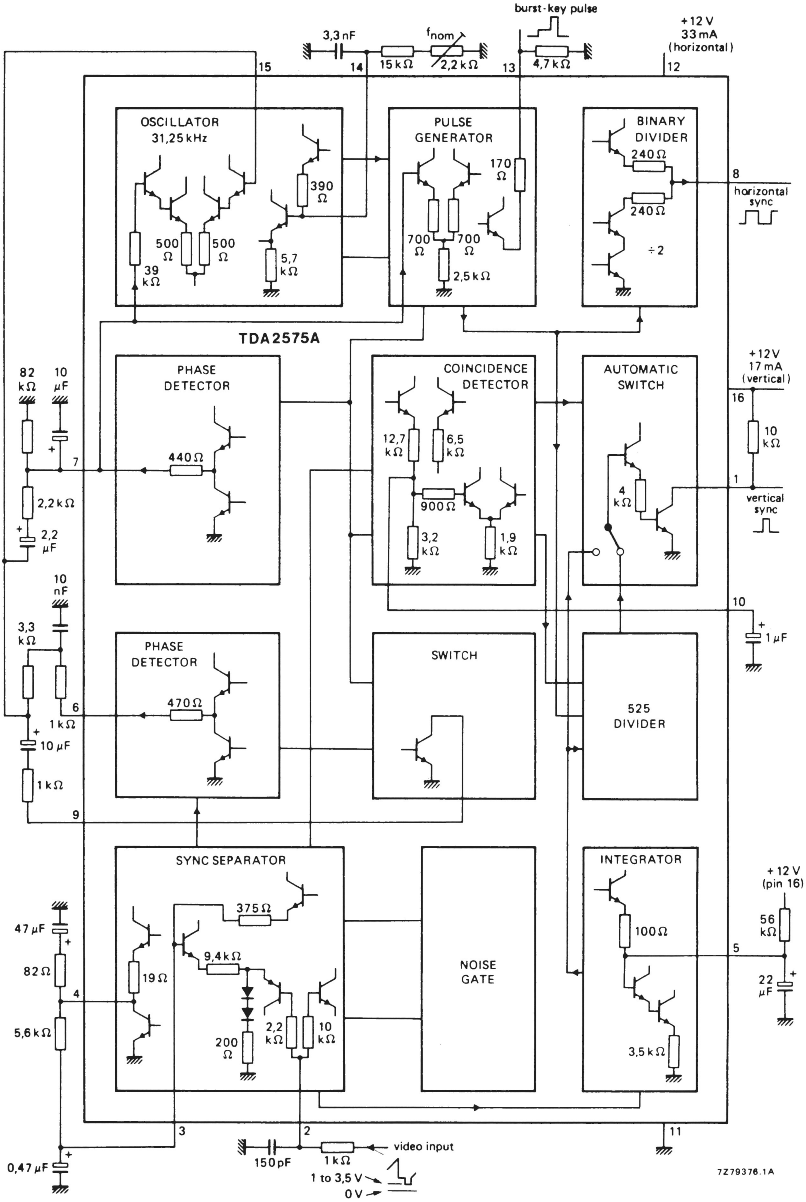

burst-key pulse
+12 V
33 mA
(horizontal)
3,3 nF
f<sub>nom</sub>
15 kΩ
2,2 kΩ
4,7 kΩ
15
14
13
12
OSCILLATOR
31,25 kHz
390 Ω
500 Ω
500 Ω
39 kΩ
5,7 kΩ
PULSE
GENERATOR
170 Ω
700 Ω
700 Ω
2,5 kΩ
BINARY
DIVIDER
240 Ω
240 Ω
÷ 2
8
horizontal
sync
TDA2575A
82 kΩ
10 μF
2,2 kΩ
2,2 μF
7
PHASE
DETECTOR
440 Ω
COINCIDENCE
DETECTOR
12,7 kΩ
6,5 kΩ
900 Ω
3,2 kΩ
1,9 kΩ
AUTOMATIC
SWITCH
4 kΩ
+12 V
17 mA
(vertical)
16
10 kΩ
1
vertical
sync
10
1 μF
10 nF
3,3 kΩ
1 kΩ
6
10 μF
1 kΩ
9
PHASE
DETECTOR
470 Ω
SWITCH
525
DIVIDER
SYNC SEPARATOR
375 Ω
19 Ω
9,4 kΩ
200 Ω
2,2 kΩ
10 kΩ
47 μF
82 Ω
4
5,6 kΩ
0,47 μF
3
NOISE
GATE
INTEGRATOR
100 Ω
3,5 kΩ
+12 V
(pin 16)
56 kΩ
5
22 μF
2
150 pF
1 kΩ
video input
1 to 3,5 V
0 V
11
7Z79376.1A

Fig. 1 Block diagram.

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | | |
|---|---|---|---|---|
| Supply voltage | | | | |
| horizontal | $V_{12\text{-}11}$ | max. | 13,2 | V |
| vertical | $V_{16\text{-}11}$ | max. | 13,2 | V |
| Total power dissipation | $P_{tot}$ | max. | 1 | W |
| Storage temperature | $T_{stg}$ | | −25 to + 130 | °C |
| Operating ambient temperature | $T_{amb}$ | | −25 to + 65 | °C |

## CHARACTERISTICS

At $V_{12\text{-}11} = 12$ V; $V_{16\text{-}11} = 12$ V; $T_{amb} = 25$ °C; measured in Fig. 1

| | | | | |
|---|---|---|---|---|
| Supply voltage range (pins 12 and 16) | $V_{12\text{-}11}$; $V_{16\text{-}11}$ | typ. | 12 | V |
| | | | 10 to 13,2 | V |
| Current consumption | $I_{12} + I_{16}$ | typ. | 50 | mA |
| | | < | 75 | mA |
| **Sync separator and noise gate** | | | | |
| Sync pulse amplitude (negative going) peak-to-peak value | $V_{2\text{-}11(p\text{-}p)}$ | | 0,07 to 1 | V * |
| Top-sync level | $V_{2\text{-}11}$ | | 1,0 to 3,5 | V |
| Slicing level | | typ. | 50 | % ** |
| Slicing level noise gating | $V_{2\text{-}11}$ | typ. | 0,7 | V |
| **Phase locked loop** | | | | |
| Holding range | Δf | typ. | ± 1000 | Hz |
| Catching range | Δf | typ. | ± 900 | Hz |
| Control sensitivity of horizontal PLL | | typ. | 2000 | Hz/μs |
| Control sensitivity of phase detector | | typ. | 1,2 | V/μs |
| Delay between sync input and detector output (pin 6) | $t_d$ | typ. | 0,4 | μs |
| Phase modulation due to hum on the supply line | | typ. | 2,0 | μs/V ▲ |

---

* Up to 1 V peak-to-peak the slicing level is constant; at amplitudes exceeding 1 V peak-to-peak the slicing level will increase.

** The slicing level is defined as the ratio of the amplitude of the slicing level to black level to the amplitude of the sync pulse.

▲ The voltage is a peak-to-peak value; the figure given can be reduced to 0,6 μs/V (p-p) by means of an extra capacitor of 330 nF between pins 12 and 7.

## CHARACTERISTICS (continued)

### Horizontal oscillator

| | | | | |
|---|---|---|---|---|
| Frequency; free running | $f_o$ | typ. | 31,500 | kHz |
| Frequency at output pin 8 | $f_8$ | typ. | 15,750 | kHz |
| Spread of frequency without spread of external components | $\Delta f_o$ | < | 4 | % |
| Temperature coefficient | T | typ. | $2,5 \times 10^{-4}$ | $K^{-1}$ |
| Change of frequency when $V_{12\text{-}11}$ drops to 6 V | $\Delta f_o$ | < | 10 | % |
| Change of frequency when $V_{12\text{-}11}$ increases from 10 to 13,2 V | $\Delta f_o$ | < | 0,5 | % |
| Output voltage; no load (peak-to-peak value) | $V_{8\text{-}11(p\text{-}p)}$ | > | 10 | V |
| Output resistance | $R_{8\text{-}11}$ | typ. | 300 | Ω |
| Output current range (peak-to-peak value) | $I_{8(p\text{-}p)}$ | | 0 to 40 | mA |
| Duty factor of output pulse | $\delta$ | typ. | 46 | % * |
| Delay between falling edge of output pulse and end of sync pulse at pin 2 | $t_d$ | typ. | 0,9 | μs ** |

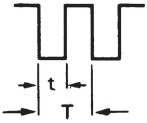
### Burst-key pulse

| | | | | |
|---|---|---|---|---|
| Output voltage (peak-to-peak value) | $V_{13\text{-}11(p\text{-}p)}$ | > | 10 | V |
| Duration of upper part of output pulse | $t_p$ | typ. | 3,6 | μs ** |
| Duration of lower part of output pulse | $t_p$ | typ. | 9,1 | μs ** |
| Amplitude of lower part of output pulse | $V_{13\text{-}11(p\text{-}p)}$ | typ. | 3 | V ** |
| Output resistance | $R_{13\text{-}11}$ | typ. | 200 | Ω |
| Delay between the end of the sync pulse at pin 2 and the rising edge of the burst key pulse | $t_d$ | typ. | 0,9 | μs ** |

### Coincidence detector

| | | | | |
|---|---|---|---|---|
| Voltage level of time constant switch | $V_{10\text{-}11}$ | typ. | 2,0 | V |
| Voltage when the oscillator is in sync | $V_{10\text{-}11}$ | typ. | 0,4 | V |
| Voltage when the oscillator is out-of-sync | $V_{10\text{-}11}$ | typ. | 2,5 | V |
| Voltage during noise | $V_{10\text{-}11}$ | typ. | 1,0 | V |

* The duty factor is specified as follows:



$$\delta = \frac{t}{T} \times 100\%.$$

** See waveforms Fig. 2.

**Vertical sync pulse**

| | | | | |
|---|---|---|---|---|
| Output voltage (peak-to-peak value) | $V_{1\text{-}11(p\text{-}p)}$ | > | 10 | V |
| Duration of output pulse during indirect synchronization | $t_p$ | typ. | 170 | μs |
| Duration of output pulse during direct synchronization (coincidence detector high) | $t_p$ | typ. | 190 | μs |
| Load resistor to pin 2 | $R_L$ | > | 2 | kΩ |
| Output voltage low with $R_L$ = 2 kΩ | $V_{1\text{-}11}$ | < | 500 | mV |
| Ratio between basic horizontal oscillator frequency and vertical pulse | | | 525 | * |

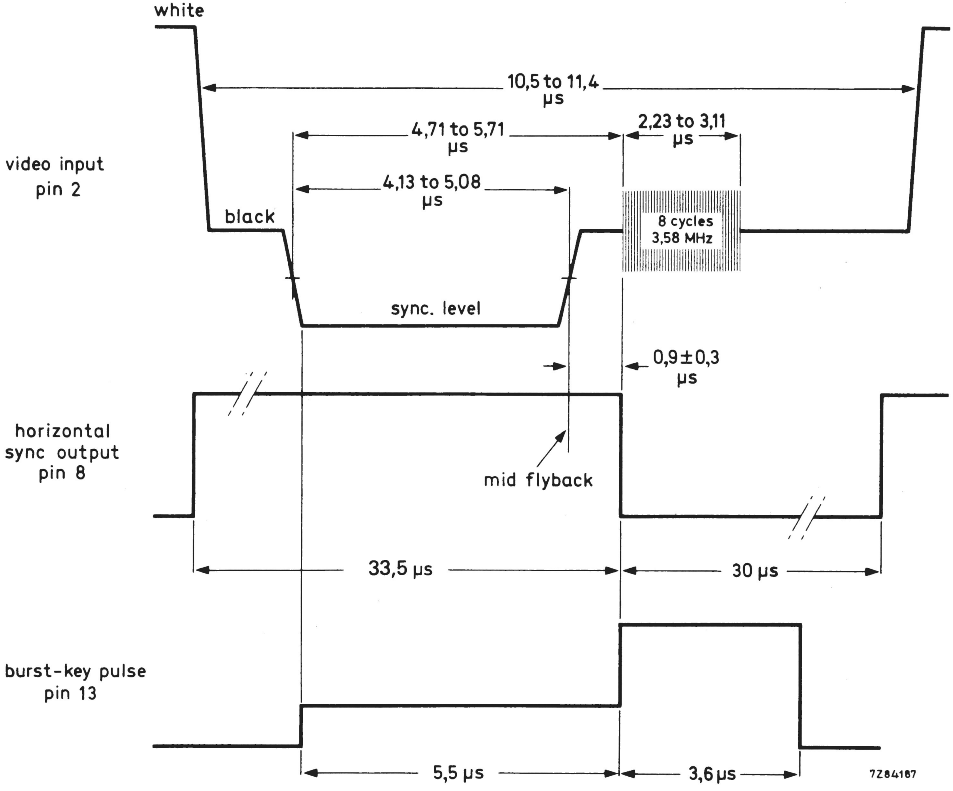

white
10,5 to 11,4 μs
4,71 to 5,71 μs
2,23 to 3,11 μs
video input pin 2
4,13 to 5,08 μs
black
8 cycles 3,58 MHz
sync. level
0,9±0,3 μs
horizontal sync output pin 8
mid flyback
33,5 μs
30 μs
burst-key pulse pin 13
5,5 μs
3,6 μs
7Z84187

Fig. 2 Relationship between the video input signal to the TDA2575A and the horizontal sync and burst-key pulse output.

* When a non-standard sync signal is applied the separated vertical sync pulse of the incoming signal is connected to pin 1; the pulse of the divider circuit is switched off.

## PINNING

1. Vertical sync pulse output
2. Video input
3. Sync separator slicing level output
4. Black level detector output
5. Vertical integrator bias network
6. Horizontal phase detector output
7. Reference voltage horizontal frequency control stage
8. Horizontal sync pulse output
9. Time constant switch
10. Coincidence detector output
11. Negative supply (ground)
12. Positive supply (horizontal)
13. Burst-key pulse output
14. RC-network horizontal oscillator
15. Control horizontal oscillator
16. Positive supply (vertical)

## APPLICATION INFORMATION

**The function is quoted against the corresponding pin number**

1. Vertical sync pulse output

   A resistor of about 10 kΩ must be connected between pin 1 and the positive supply line (pin 16; vertical supply).

   The output pulse will come from the 525 divider stage (standard signal) or from the vertical sync pulse separator (non-standard signal), depending on the input signal on pin 2. The standard and non-standard signals are detected automatically.

2. Video input

   The input signal must have negative-going sync pulses. The top-sync level can vary between 1 V and 3,5 V without affecting the sync separator operation.

   The slicing level of the sync separator is fixed at 50%, for the sync pulse amplitude range 0,07 to 1 V. As a consequence the circuit gives a good sync separation down to pulses with an amplitude of 70 mV peak-to-peak (sync pulse compression). For sync pulses in excess of 1 V peak-to-peak the slicing level will increase.

   The noise gate is activated at an input level $< 0,7$ V, thus, when noise gating is required the top-sync level should be chosen close to the minimum level of 1 V. When i.f. circuits with a noise gate are used (e.g. TDA2540; TDA2541) the noise gate of the TDA2575A is not required.

3. Sync separator slicing level output

   The sync separator slicing level is determined on this pin. A slicing level of 50% is obtained by comparing this level with the black level of the video signal, which is detected at pin 4. The capacitor connected to pin 3 must be about 0,47 μF.

4. Black level detector output

   The black level of the input signal is detected on this pin, which is required to obtain good sync separator operation. A capacitor of 47 μF in series with a resistor of 82 Ω has to be connected to this pin. A 5,6 kΩ resistor must be connected between pins 3 and 4.

5. Vertical sync pulse integrator bias network

   The vertical sync pulse is obtained by integrating the composite sync signal in an internal RC-network. An external RC-network is required for the correct biasing of this circuit for various input conditions. Typical values are: R = 56 kΩ; c = 22 μF.

6. Horizontal phase detector output

   The control voltage for the horizontal oscillator is obtained on this pin. The output current is about 2 mA.

7. Reference voltage horizontal frequency control stage

   This pin has two functions. It is used to decouple the reference voltage for the frequency control of the horizontal oscillator (so a good suppression of interference is obtained which may be present on the supply line). This pin is also used to control the reference waveform for the phase detector to the middle of the gating, giving a good noise immunity of the synchronization.

8. Horizontal sync pulse output

   This pulse is obtained from the horizontal oscillator via a divider circuit. The duty factor is 46%. The falling edge of this pulse has a delay of 0,9 μs with respect to the end of the sync pulse. Because of this phase relationship this pulse can directly drive the TDA2581.

9. Time constant switch

   This pin is used to switch the time constant of the flywheel filter. The pin condition is determined by the coincidence detector (pin 10). During in-sync or when only noise is received pin 9 assumes ground level, which results in a long time constant and good noise immunity.

   During out-of-sync or VCR playback, pin 9 has a high impedance and consequently only the short time constant is available. In this condition a large catching range is obtained.

10. Coincidence detector output

    A 1 μF capacitor must be connected to this pin. The output voltage depends on the oscillator condition (synchronized or not) and on the video input signal.
    The following output voltages can occur:

    | | |
    |---|---|
    | — when in-sync: | 0,4 V |
    | — when out-of-sync: | 2,0 V |
    | — during noise at input: | 1,0 V |

    When the output voltage $<$ 1,85 V, the flywheel filter is switched to a long time constant, and the gating of the phase detector is switched-on.

    For a voltage $>$ 1,85 V, the flywheel filter has a short time constant, and the gating of the phase detector is switched-off. The result is that during noise the flywheel time constant remains long thus preventing large shifts in the frequency of the horizontal oscillator (and screening of the horizontal output transformer).

    The information of the line coincidence detector is fed to the divider circuit so that there is no delay in vertical synchronization after a channel change, or an unsynchronized camera change in the studio. Thus, the divider circuit is reset to direct sync, when line synchronization is lost.

    The time constant value can be switched manually by a resistor (10 kΩ) to + 12 V.

11. Negative supply (ground)

12. Positive supply horizontal oscillator

    Interference and hum on this supply line can affect the oscillator frequency. It is therefore necessary to have a separate decoupling of this pin with respect to pin 16. The current-draw of this pin is typically 33 mA.

13. Burst-key pulse output

    This pulse is composed of two parts. The lower part has an amplitude of 3 V peak-to-peak and a width of 9,1 μs (for phase relation see Fig. 2). The upper part has a total amplitude in excess of 10 V peak-to-peak and a width of 3,6 μs. The leading edge of this pulse has a delay of 0,9 μs with respect to the falling edge of the sync pulse at the input (pin 2).

    This pulse can directly drive the burst gate/black level clamp input of the TDA2560.

**APPLICATION INFORMATION** (continued)

14. RC-network horizontal oscillator

    Stable components should be chosen for good frequency stability. For adjusting the frequency a part of the total resistance must be variable. This part should be as small as possible, because of poor stability of variable carbon resistors.

    The oscillator can be adjusted when pins 7 and 15 are short-circuited.

15. Horizontal oscillator control pin

16. Positive supply sync separator and divider circuit (vertical)

    For this supply only a simple decoupling is required. The current-draw of this pin is typically 17 mA.

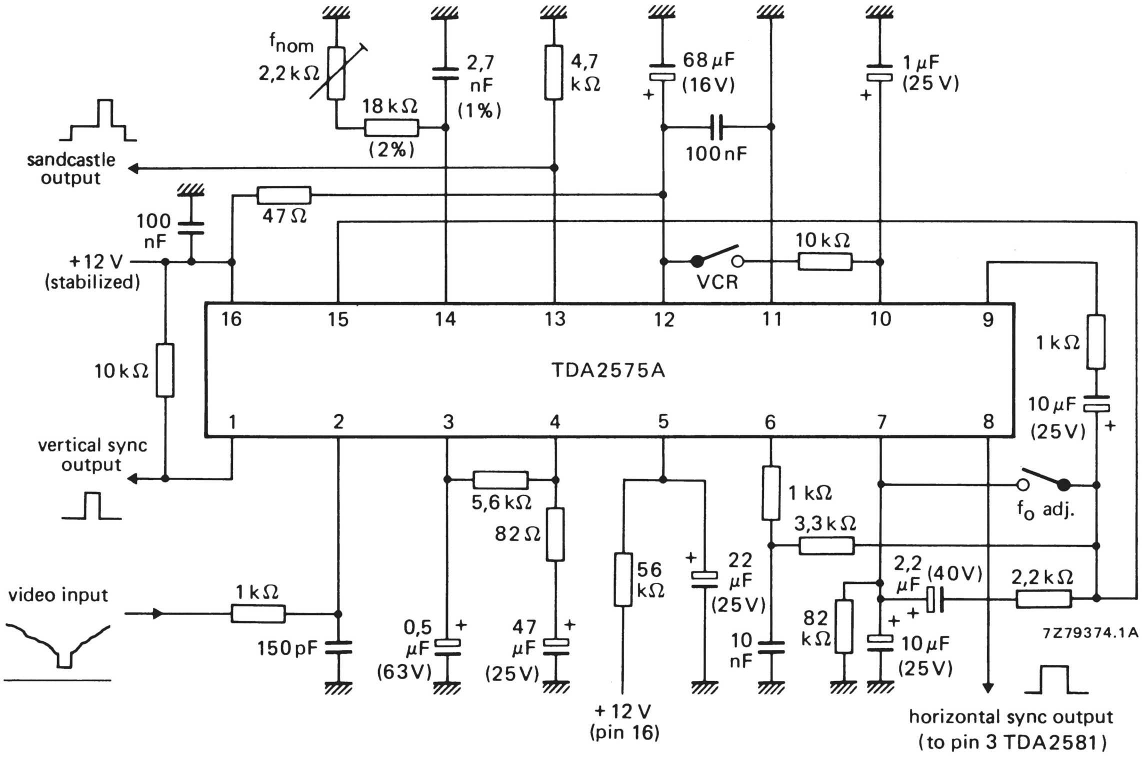

f<sub>nom</sub>
2,2 kΩ
18 kΩ
(2%)
2,7 nF (1%)
4,7 kΩ
68 μF (16V)
100 nF
1 μF (25 V)
sandcastle output
100 nF
47 Ω
+12 V (stabilized)
10 kΩ
VCR
16
15
14
13
12
11
10
9
TDA2575A
1
2
3
4
5
6
7
8
1 kΩ
10 μF (25V)
10 kΩ
vertical sync output
5,6 kΩ
82 Ω
1 kΩ
3,3 kΩ
f<sub>o</sub> adj.
video input
1 kΩ
150 pF
0,5 μF (63V)
47 μF (25V)
56 kΩ
22 μF (25V)
10 nF
82 kΩ
2,2 μF (40V)
2,2 kΩ
10 μF (25V)
7Z79374.1A
+12 V (pin 16)
horizontal sync output (to pin 3 TDA2581)

Fig. 3 Typical application circuit diagram; for combination of the TDA2575A with the TDA2581 see Fig. 4.

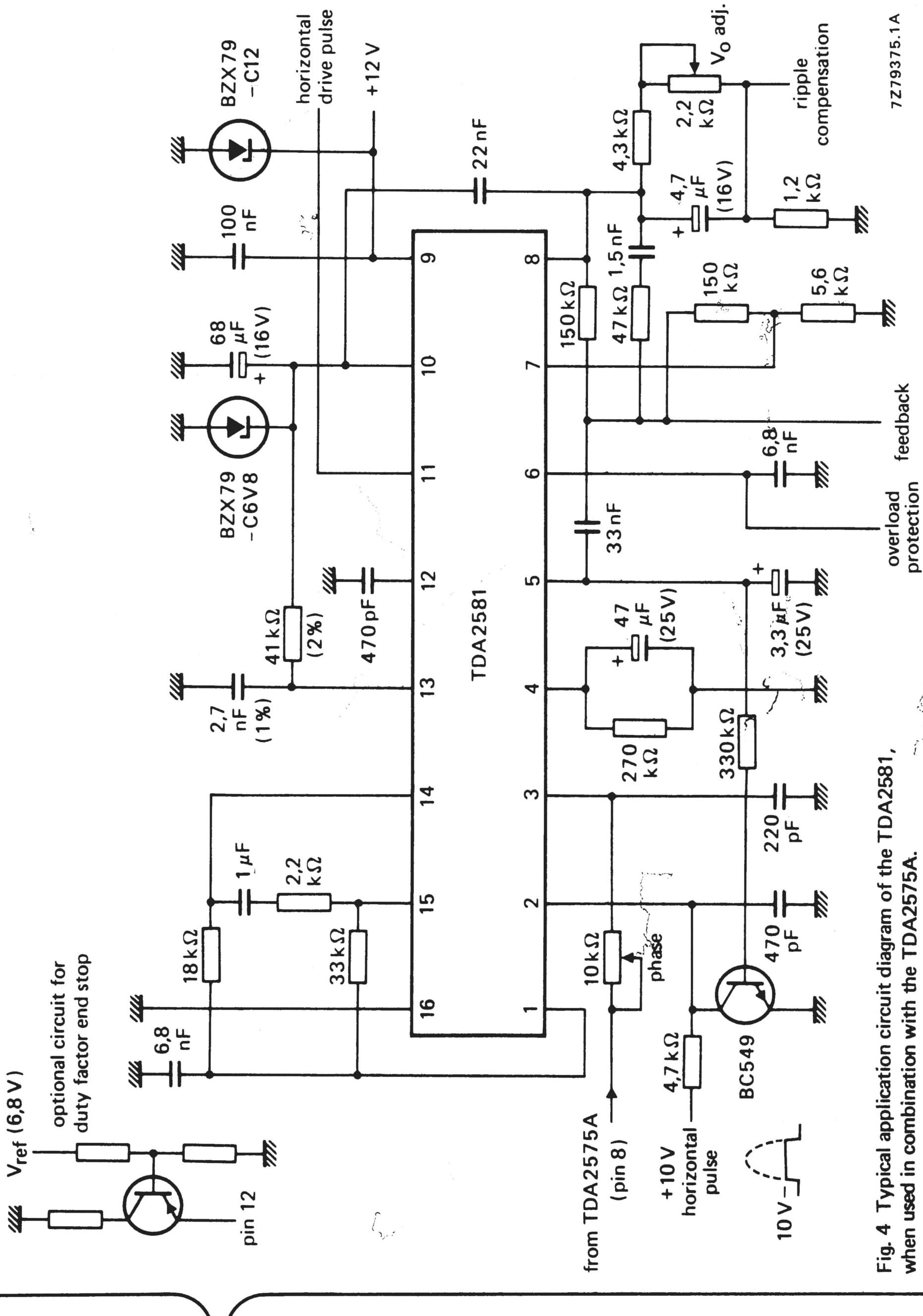

TDA2581
BZX79 −C12
horizontal drive pulse
+12 V
100 nF
22 nF
68 μF (16V)
BZX79 −C6V8
470 pF
41 kΩ (2%)
2,7 nF (1%)
1 μF
2,2 kΩ
18 kΩ
33 kΩ
6,8 nF
optional circuit for duty factor end stop
V$_{ref}$ (6,8 V)
pin 12
150 kΩ
47 kΩ
1,5 nF
4,3 kΩ
4,7 μF (16V)
2,2 kΩ
V$_o$ adj.
ripple compensation
1,2 kΩ
150 kΩ
5,6 kΩ
feedback
6,8 nF
overload protection
33 nF
3,3 μF (25V)
47 μF (25V)
270 kΩ
330 kΩ
220 pF
470 pF
10 kΩ
phase
from TDA2575A (pin 8)
+10 V horizontal pulse
4,7 kΩ
BC549
10 V
7Z79375.1A
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16

Fig. 4 Typical application circuit diagram of the TDA2581, when used in combination with the TDA2575A.

# HORIZONTAL OSCILLATOR COMBINATION WITH VERTICAL 625 DIVIDER SYSTEM

The TDA2576A is a horizontal oscillator combination intended to be used in various types of transistorized horizontal deflection circuits, e.g. switched-mode driven and power-pack system circuits.

The circuit is optimized for a horizontal and vertical frequency ratio of 625.

The circuit incorporates the following functions:

- Horizontal sync separator with sliding bias in such way that the sync pulse is always sliced between top-sync level and blanking level.
- Noise gate.
- Phase detector which compares the sync pulse with the oscillator voltage; this phase detector is gated.
- Phase detector which compares the line flyback pulse with the oscillator voltage.
- Horizontal oscillator (31,25 kHz).
- Time constant switching of the first control loop (short time constant during catching and reception of VCR signals).
- Burst key pulse generator (sandcastle pulse with three levels).
- Vertical sync pulse separator.
- Very stable vertical synchronization due to the 625 divider system, without delay after channel change.

## QUICK REFERENCE DATA

| | | | | |
|---|---|---|---|---|
| Supply voltage | $V_{16\text{-}9}$ | typ. | 12 | V |
| Supply current consumption | $I_{16}$ | typ. | 53 | mA |
| Sync input voltage (peak-to-peak value) | $V_{4\text{-}9(p\text{-}p)}$ | | 0,1 to 1 | V |
| Slicing level | | typ. | 50 | % |
| Control sensitivity sync to flyback | | typ. | 10 | kHz/μs |
| Holding range | Δf | typ. | ± 1000 | Hz |
| Catching range | Δf | typ. | ± 900 | Hz |
| Horizontal output pulse (peak-to-peak value) | $V_{10\text{-}9(p\text{-}p)}$ | typ. | 11 | V |
| Vertical output pulse; pin 2 (peak-to-peak value) | $V_{2\text{-}9(p\text{-}p)}$ | typ. | 11 | V |
| Sandcastle output pulse (peak-to-peak value) | $V_{14\text{-}9(p\text{-}p)}$ | typ. | 11 | V |

## PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).

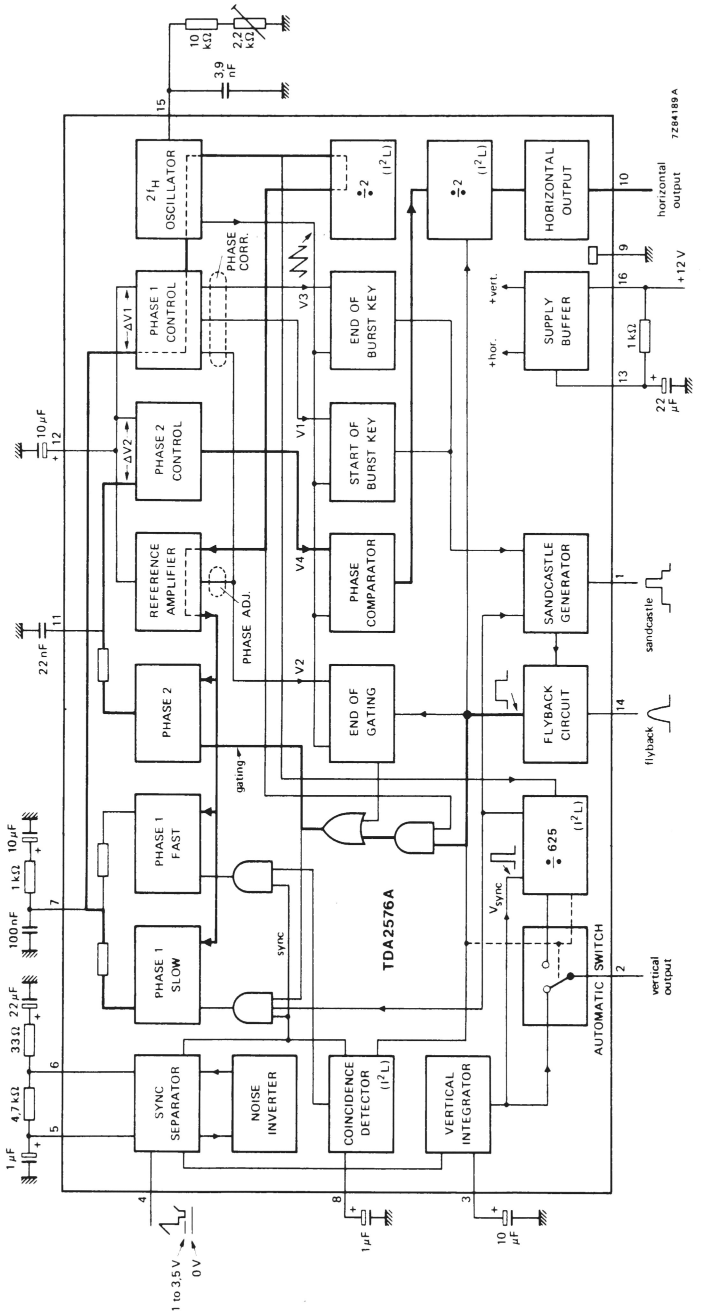

TDA2576A
SYNC SEPARATOR
NOISE INVERTER
COINCIDENCE DETECTOR ($I^2L$)
VERTICAL INTEGRATOR
PHASE 1 SLOW
PHASE 1 FAST
PHASE 2
REFERENCE AMPLIFIER
PHASE 2 CONTROL
PHASE 1 CONTROL
$2f_H$ OSCILLATOR
÷2 ($I^2L$)
END OF BURST KEY
START OF BURST KEY
PHASE COMPARATOR
END OF GATING
÷2 ($I^2L$)
HORIZONTAL OUTPUT
SUPPLY BUFFER
SANDCASTLE GENERATOR
FLYBACK CIRCUIT
÷625 ($I^2L$)
AUTOMATIC SWITCH
PHASE CORR.
PHASE ADJ.
gating
sync
$V_{sync}$
V1
V2
V3
V4
$\Delta V1$
$\Delta V2$
+hor.
+vert.
1 to 3,5 V
0 V
1 μF
4,7 kΩ
33 Ω
22 μF
100 nF
1 kΩ
10 μF
22 nF
10 μF
3,9 nF
10 kΩ
2,2 kΩ
1 μF
10 μF
1 kΩ
22 μF
+12 V
horizontal output
sandcastle
flyback
vertical output
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
7Z84189A

Fig. 1 Block diagram.

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | | |
|---|---|---|---|---|
| Supply voltage | $V_{16-9}$ | max. | 13,2 | V |
| Total power dissipation | $P_{tot}$ | max. | 1 | W |
| Storage temperature | $T_{stg}$ | | −55 to + 125 | °C |
| Operating ambient temperature | $T_{amb}$ | | −25 to + 65 | °C |

## CHARACTERISTICS

$V_{16-9} = 12$ V; $T_{amb} = 25$ °C; measured in Fig. 2.

| | | | | |
|---|---|---|---|---|
| Supply voltage | $V_{16-9}$ | typ. | 12 | V |
| | | | 10 to 13,2 | V |
| Supply current consumption | $I_{16}$ | typ. | 53 | mA |
| | | < | 70 | mA |
| **Sync separator and noise gate** | | | | |
| Sync pulse amplitude (negative going) peak-to-peak value | $V_{4-9(p-p)}$ | | 0,1 to 1 | V* |
| Top-sync level | $V_{4-9}$ | | 1,0 to 3,5 | V |
| Slicing level noise gate | $V_{4-9}$ | < | 1 | V |
| Delay between sync input and detector output (pin 7) | | typ. | 0,35 | μs |
| **First control loop** (sync-to-oscillator) | | | | |
| Holding range | Δf | typ. | ± 1000 | Hz |
| Catching range | Δf | typ. | ± 900 | Hz |
| Control sensitivity video | | | | |
| with respect to oscillator | | typ. | 2,0 | kHz/μs |
| with respect to sandcastle | | typ. | 10,0 | kHz/μs |
| with respect to flyback pulse | | typ. | 10,0 | kHz/μs |
| Phase modulation due to hum on the supply line (pin 16) | | < | 1,0 | μs/V** |
| **Second control loop** (oscillator-to-flyback) | | | | |
| Control sensitivity | $\Delta t_d/\Delta t_o$ | typ. | 250 | ▲ |
| Control range | $t_d$ | < | 26 | μs |

---

* Up to 1 V peak-to-peak the slicing level is constant; at amplitudes exceeding 1 V peak-to-peak the slicing level will increase.

** This voltage is a peak-to-peak value.

▲ $t_d$ = delay between positive transient of horizontal output pulse and the rising edge of the flyback pulse.
$t_o$ = delay between the rising edge of the flyback pulse and the start of the current in $\varphi_1$ ($I_7$).

## CHARACTERISTICS (continued)

### Horizontal oscillator

| | | | | |
|---|---|---|---|---|
| Frequency; free running | $f_o$ | typ. | 31,250 | kHz |
| Frequency at output pin 10 | $f_{10}$ | typ. | 15,625 | kHz |
| Spread of frequency without spread of external components | $\Delta f_o$ | < | 4 | % |
| Temperature coefficient | T | typ. | $2,5 \times 10^{-4}$ | |
| Change of frequency when $V_{16\text{-}9}$ increases from 10 to 13,2 V | $\Delta f_o$ | < | 0,5 | % |
| Minimum supply voltage (+ hor. see Fig. 1) | | typ. | 7 | V |
| Frequency deviation at min. supply voltage | | < | 10 | % |

### Horizontal output (pin 10)

| | | | | |
|---|---|---|---|---|
| Maximum supply voltage | | < | 13,2 | V |
| Minimum output voltage at a current of 60 mA | $V_{10\text{-}9}$ | < | 700 | mV |
| Maximum output current | $I_{10}$ | < | 60 | mA |
| Duration of the output pulse | $t_p$ | | 12 to 38 | μs |

### Sandcastle pulse (pin 1)

| | | | | |
|---|---|---|---|---|
| Output voltage during burst key pulse | $V_{1\text{-}9}$ | > | 10 | V |
| Pulse duration | $t_p$ | typ. | 4,0 | μs |
| Amplitude of second level of output pulse | $V_{1\text{-}9}$ | typ. | 4,5 | V |
| Pulse duration | flyback pulse | | | |
| Amplitude of third level of output pulse | $V_{1\text{-}9}$ | typ. | 2,5 | V |
| Pulse duration | $t_p$ | typ. | 1,34 | μs* |
| Delay between the start of the sync pulse at the video input (pin 4) and the rising edge of the burst key pulse | $t_d$ | typ. | 4,9 | μs |

### Phase adjustment (pin 12)

| | | | | |
|---|---|---|---|---|
| Voltage at pin 12 | $V_{12\text{-}9}$ | typ. | 2,8 | V |
| Control sensitivity | | typ. | 0,6 | V/μs |
| Control range | | typ. | ± 1 | μs |

### Coincidence detector (pin 8)

| | | | | |
|---|---|---|---|---|
| Voltage level of time constant switch | $V_{8\text{-}9}$ | typ. | 2,1 | V |
| Voltage when the oscillator is in sync | $V_{8\text{-}9}$ | typ. | 1,2 | V |
| Voltage when the oscillator is out-of-sync | $V_{8\text{-}9}$ | typ. | 2,6 | V |
| Voltage during noise | $V_{8\text{-}9}$ | typ. | 1,7 | V |

---

* During standard video signals.

| | | | |
|---|---|---|---|
| **Flyback input pulse** (pin 14) | | | |
| Switching level | $V_{14\text{-}9}$ | typ. | 0,7 V |
| Input pulse | $V_{14\text{-}9}$ | < | 12 V |
| Input resistance | | typ. | 2,5 kΩ |
| Delay between the start of the sync pulse at the video input (pin 4) and the rising edge of the flyback pulse | $t_p$ | typ. | 1,5 μs |
| **Vertical outputs** | | | |
| Output voltage (peak-to-peak value) | $V_{2\text{-}9(p\text{-}p)}$ | > | 10 V |
| Output current | $I_2$ | < | 5 mA |
| Output voltage low at $I_2 = 5$ mA | $V_{2\text{-}9}$ | < | 500 mV |
| Duration of output pulse during indirect synchronization | $t_p$ | typ. | 190 μs |
| Duration of output pulse during direct synchronization | $t_p$ | typ. | 160 μs |
| Ratio between basic horizontal oscillator frequency and vertical pulse | | | 625 * |

---

* When a non-standard sync signal is applied the separated vertical sync pulse of the incoming signal is connected to pin 2; the pulse of the divider circuit is switched off.

## APPLICATION INFORMATION (see also Fig. 2)

**The function is described against the corresponding pin number**

1. Sandcastle output pulse

   This output pulse has three levels. The first and highest level (10 V) is the burst key pulse with a typical duration of 4,0 μs. The second level for the line blanking is typ. 4,5 V with a pulse duration equal to the line flyback pulse. The third level (typ. 2,5 V) is used for frame blanking and has a duration of typ. 1,34 ms (21 lines). This last pulse is only available with a standard video input signal. Under all other conditions, an external vertical flyback pulse must be applied to this pin. This pulse will be clamped to 2,5 V by means of an internal clamping circuit. The input current is typ. 2 mA.

2. Vertical output pulse

   This pulse is obtained from the divider circuit, the amplitude is in excess of 10 V peak-to-peak. This pulse has a duration of 190 μs when standard signals are received. The pulse is obtained from the vertical sync pulse integrator during non-standard signals and has a duration of about 160 μs. It has good stability and accuracy, so it is intended to be used for triggering the vertical oscillator.

3. Vertical sync pulse integrator bias network

   The vertical sync pulse is obtained by integrating the composite sync signal in an internal RC-network. An external capacitor with an internal resistor are required for the correct biasing of this circuit for various input conditions. A typical value for the capacitor is 10 μF.

4. Video input

   The input signal must have negative-going sync pulses. The top-sync level can vary between 1 V and 3,5 V without affecting the sync separator operation.

   The slicing level of the sync separator is fixed at 50%, for the sync pulse amplitude range 0,1 to 1 V peak-to-peak. As a consequence the circuit gives a good sync separation down to pulses with an amplitude of 100 mV peak-to-peak (sync pulse compression). For sync pulses in excess of 1 V peak-to-peak the slicing level will increase.

   The noise gate is activated at an input level < 1 V (typ. 0,7 V), thus, when noise gating is required the top-sync level should be chosen close to the minimum level of 1 V.

5. Sync separator slicing level output

   The sync separator slicing level is determined on this pin. A slicing level of 50% is obtained by comparing this level with the black level of the video signal, which is detected at pin 6. The capacitor connected to pin 5 must be about 1 μF.

6. Black level detector output

   The black level of the input signal is detected on this pin. A capacitor of 22 μF in series with a resistor of 33 Ω has to be connected to this pin. A 4,7 kΩ resistor must be connected between pins 5 and 6.

7. Horizontal phase detector output and control oscillator input

   The flywheel filter must be connected to this pin. Typical values for the components are a capacitor of 100 nF in parallel with an RC-network of 1 kΩ and 10 μF. Furthermore, a resistor of 270 kΩ should be connected between pins 7 and 12.
   The output current of the phase detector depends on the condition of the coincidence detector. The output current is high when the oscillator is out of sync. The result is a large catching range, and the phase detector is not gated in that condition. The output current is low when the oscillator is synchronized and the phase detector is gated. A good noise immunity is obtained in this case.

8 Coincidence detector output

A 1 $\mu$F capacitor must be connected to this pin. The output voltage depends on the oscillator condition (synchronized or not) and on the video input signal.
The following output voltages can occur:

| | |
|---|---|
| – when in-sync | 1,2 V |
| – when out-of-sync | 2,6 V |
| – during noise at the input | 1,7 V |

When the output voltage $<$ 2,1 V, the phase detector output current is low and the phase detector is gated. A good noise immunity is obtained in this case. For a voltage $>$ 2,1 V, the output current of the phase detector is high and the phase detector is not gated. This results in a large catching range and a high dynamical steepness of the PLL. This latter condition is required during VCR-playback. It can be obtained by connecting pin 8 to the positive supply line via a resistor of 10 kΩ. The information of the line coincidence detector is fed to the divider circuit so that there is no delay in vertical synchronization after a channel change, or an unsynchronized camera change in the studio. Thus, the divider circuit is reset to direct sync, when line synchronization is lost.

9. Negative supply (ground)

10. Horizontal output

This is an open collector output. The collector resistor must be chosen such that sufficient current is supplied to the driver stage. The maximum current is 60 mA. The output stage is designed such that the line output transistor cannot be switched-on during flyback. Switching-on occurs directly after the flyback pulse to avoid linearity errors. The duty factor of the output pulse depends on the delay in the output stage (correction via the second control loop).

11. Control voltage second loop

This voltage controls the start of the output pulse at pin 10 (positive-going edge). The capacitor connected to this pin must have a value of about 22 nF.

12. Reference voltage control loops

The reference voltage must be decoupled by means of a capacitor of about 10 $\mu$F.
It is possible to obtain a phase shift between video and flyback pulse by changing this reference voltage externally. The possible phase shift is ± 1 $\mu$s.
The required voltage change is ± 0,6 V.

13. Decoupling internal power supply

The IC has two power supply terminals. The main terminal (pin 16) supplies the output stages, the sync separator and the divider circuit. The specially decoupled supply terminal (pin 13) supplies the horizontal oscillator. This is to avoid coupling of the video signal into the oscillator part. The capacitor connected to pin 13 should have a value of about 22 $\mu$F. The resistor connected between pins 13 and 16 should have a value of about 1 kΩ.

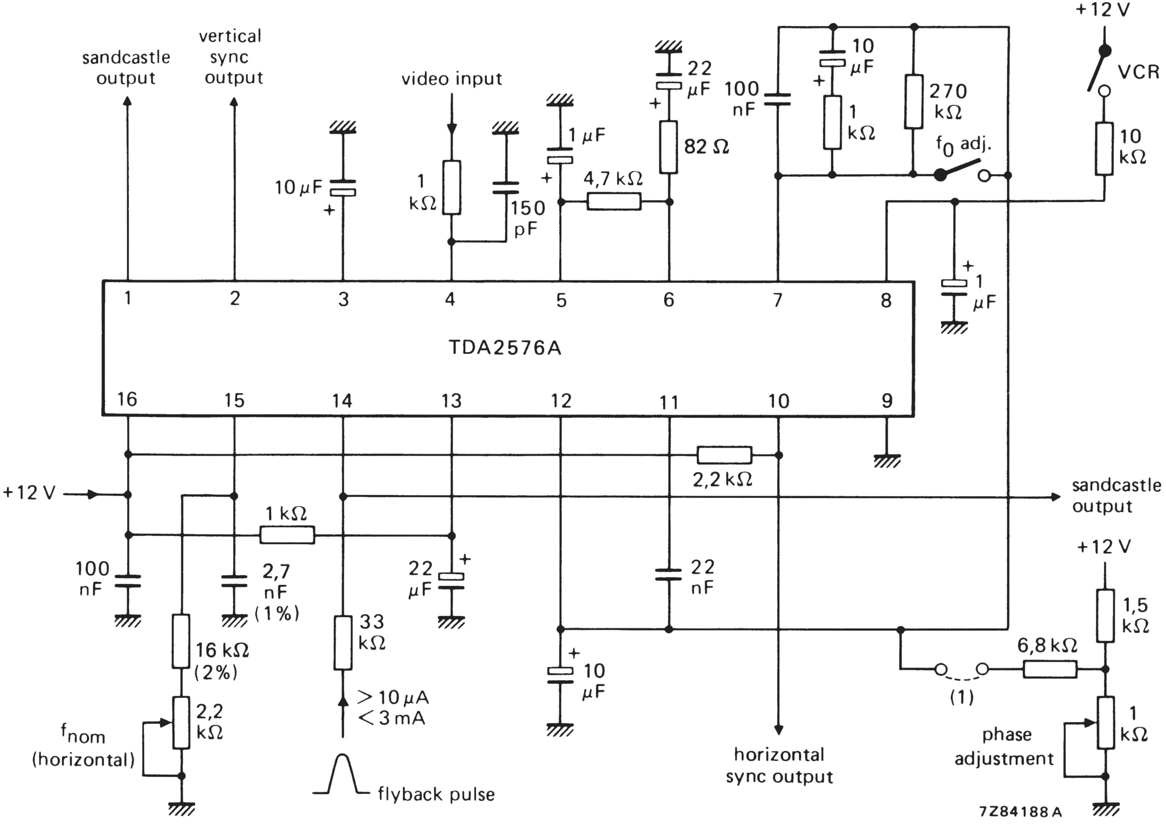
14. Flyback input pulse

The flyback input pulse is required for the second phase control loop and for generating the line blanking pulse in the sandcastle output. The input current should be at least 10 $\mu$A and not exceed 3 mA.

15. RC-network horizontal oscillator

Stable components should be chosen for a good frequency stability. A part of the total resistance must be variable for adjusting the frequency. This part should be as small as possible, because of poor stability of variable carbon resistors.
The oscillator can be adjusted when pins 7 and 12 are short-circuited (see Fig. 2).

16. Positive supply: The supply voltage may vary between 10 V and 13,2 V. The current-draw is 53 mA (typical) and a range of 35 to 70 mA at 12 V.


sandcastle output
vertical sync output
video input
10 μF
1 kΩ
150 pF
1 μF
4,7 kΩ
22 μF
82 Ω
100 nF
10 μF
1 kΩ
270 kΩ
f0 adj.
+12 V
VCR
10 kΩ
1 μF
1
2
3
4
5
6
7
8
TDA2576A
16
15
14
13
12
11
10
9
2,2 kΩ
+12 V
sandcastle output
1 kΩ
100 nF
2,7 nF (1%)
22 μF
22 nF
+12 V
1,5 kΩ
16 kΩ (2%)
33 kΩ
6,8 kΩ
10 μF
(1)
2,2 kΩ
> 10 μA
< 3 mA
1 kΩ
fnom (horizontal)
horizontal sync output
phase adjustment
flyback pulse
7Z84188 A

(1) Optional circuit for phase adjustment.

Fig. 2 Application circuit diagram.

This information is derived from development samples
made available for evaluation. It does not necessarily
imply that the device will go into regular production.

# SYNCHRONIZATION CIRCUIT WITH VERTICAL OSCILLATOR AND DRIVER STAGES

## GENERAL DESCRIPTION

The TDA2577A separates the vertical and horizontal sync pulses from the composite TV video signal and uses them to synchronize horizontal and vertical oscillators.

### Features

- Horizontal sync separator and noise inverter
- Horizontal oscillator
- Horizontal output stage
- Horizontal phase detector (sync to oscillator)
- Time constant switch for phase detector (fast time constant during catching)
- Slow time constant for noise only conditions
- Time constant externally switchable (e.g. fast for VCR)
- Inhibit of horizontal phase detector and video transmitter identification circuit during vertical oscillator flyback
- Second phase detector ($\varphi 2$) for storage compensation of horizontal deflection stage
- Sandcastle pulse generator (3-levels)
- Video transmitter identification circuit
- Stabilizer and supply circuit for starting the horizontal oscillator and output stage directly from the mains rectifier
- Duty factor of horizontal output pulse is 50% when flyback pulse is absent
- Vertical sync separator
- Bandgap 6,5 V reference voltage for vertical oscillator and comparator
- Synchronized vertical oscillator/sawtooth generator (synchronization inhibited when no video transmitter is detected)
- Internal circuit for 3% parabolic pre-correction of the oscillator/sawtooth generator. Comparator supplied with pre-corrected sawtooth and external feedback input
- Vertical comparator with internal 3% pre-correction circuit for vertical oscillator/sawtooth generator
- Vertical driver stage
- Vertical blanking pulse generator with external adjustment of pulse duration (50 Hz: 21 lines; 60Hz: 17 lines)
- Vertical guard circuit

## QUICK REFERENCE DATA

| | | | | |
|---|---|---|---|---|
| **Supply** | | | | |
| Minimum current required to start horizontal oscillator and output stage (pin 16) | $I_{16}$ | > | 4 | mA |
| Main supply voltage (pin 10) | $V_P = V_{10\text{-}9}$ | typ. | 12 | V |
| Supply current | $I_P = I_{10}$ | typ. | 55 | mA |
| **Input signals** | | | | |
| Sync pulse input voltage (peak-to-peak value; negative-going) | $V_{5\text{-}9(p\text{-}p)}$ | | 0,15 to 1 | V |
| **Output signals** | | | | |
| Horizontal output pulse (open collector) at $I_{11}$ = 40 mA | $V_{11\text{-}9}$ | < | 0,5 | V |
| Vertical output pulse (emitter-follower) at $I_1$ = 10 mA | $V_{1\text{-}9}$ | > | 4 | V |

## PACKAGE OUTLINE

18-lead DIL; plastic (SOT-102HE).

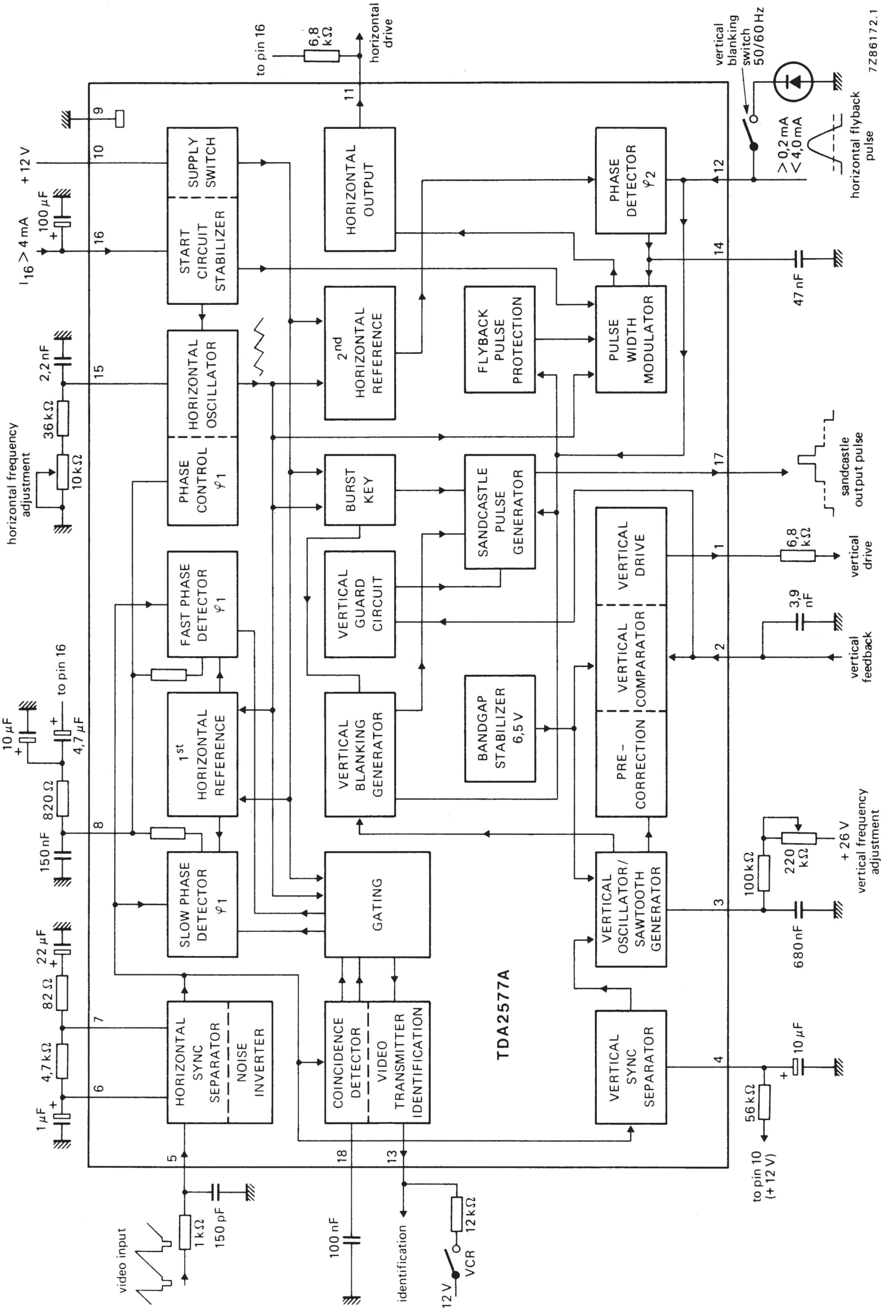

to pin 16
6,8 kΩ
horizontal drive
11
9
10
+12 V
SUPPLY SWITCH
START CIRCUIT STABILIZER
16
I16 > 4 mA
100 µF
HORIZONTAL OUTPUT
vertical blanking switch 50/60 Hz
7Z86172.1
PHASE DETECTOR φ2
12
> 0,2 mA
< 4,0 mA
horizontal flyback pulse
14
47 nF
2nd HORIZONTAL REFERENCE
FLYBACK PULSE PROTECTION
PULSE WIDTH MODULATOR
2,2 nF
15
HORIZONTAL OSCILLATOR
36 kΩ
10 kΩ
horizontal frequency adjustment
PHASE CONTROL φ1
BURST KEY
SANDCASTLE PULSE GENERATOR
17
sandcastle output pulse
FAST PHASE DETECTOR φ1
VERTICAL GUARD CIRCUIT
VERTICAL DRIVE
1
6,8 kΩ
vertical drive
3,9 nF
2
vertical feedback
VERTICAL COMPARATOR
to pin 16
10 µF
4,7 µF
1st HORIZONTAL REFERENCE
VERTICAL BLANKING GENERATOR
BANDGAP STABILIZER 6,5 V
PRE-CORRECTION
820 Ω
8
150 nF
SLOW PHASE DETECTOR φ1
GATING
VERTICAL OSCILLATOR/ SAWTOOTH GENERATOR
100 kΩ
220 kΩ
+26 V
vertical frequency adjustment
3
680 nF
22 µF
82 Ω
7
4,7 kΩ
6
1 µF
HORIZONTAL SYNC SEPARATOR
NOISE INVERTER
COINCIDENCE DETECTOR
VIDEO TRANSMITTER IDENTIFICATION
TDA2577A
VERTICAL SYNC SEPARATOR
4
10 µF
56 kΩ
to pin 10 (+12 V)
5
18
13
video input
1 kΩ
150 pF
100 nF
identification
+12 V
VCR
12 kΩ

Fig. 1 Block diagram.

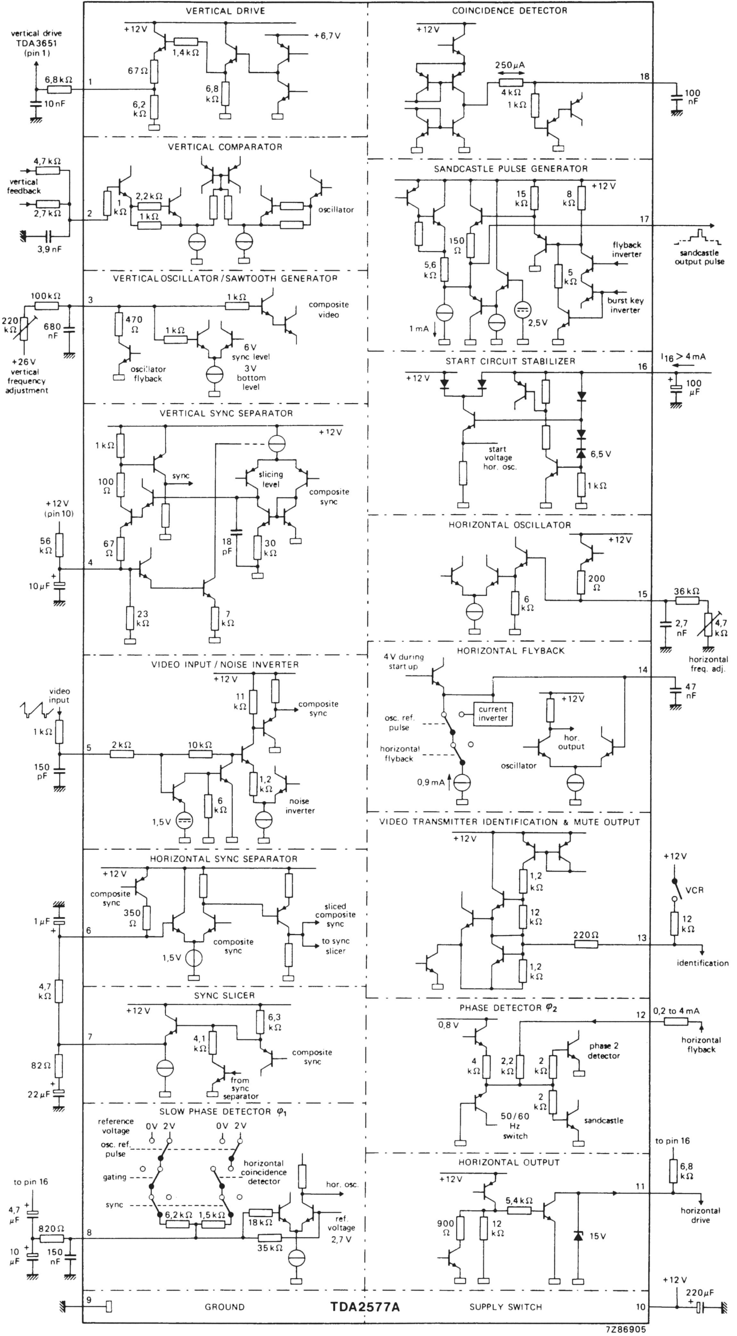

VERTICAL DRIVE
vertical drive TDA3651 (pin 1)
6,8 kΩ
10 nF
+12 V
1,4 kΩ
67 Ω
6,2 kΩ
6,8 kΩ
+6,7 V
VERTICAL COMPARATOR
4,7 kΩ
vertical feedback
2,7 kΩ
3,9 nF
2,2 kΩ
1 kΩ
oscillator
VERTICAL OSCILLATOR / SAWTOOTH GENERATOR
100 kΩ
220 kΩ
680 nF
+26 V
vertical frequency adjustment
470 Ω
oscillator flyback
composite video
6 V sync level
3 V bottom level
VERTICAL SYNC SEPARATOR
+12 V (pin 10)
56 kΩ
10 μF
100 Ω
67 Ω
23 kΩ
7 kΩ
sync
slicing level
composite sync
18 pF
30 kΩ
VIDEO INPUT / NOISE INVERTER
video input
1 kΩ
150 pF
2 kΩ
10 kΩ
11 kΩ
composite sync
1,2 kΩ
noise inverter
6 kΩ
1,5 V
HORIZONTAL SYNC SEPARATOR
1 μF
composite sync
350 Ω
1,5 V
sliced composite sync
to sync slicer
SYNC SLICER
4,7 kΩ
82 Ω
22 μF
6,3 kΩ
4,1 kΩ
from sync separator
SLOW PHASE DETECTOR φ1
reference voltage
0V 2V
osc. ref. pulse
gating
sync
horizontal coincidence detector
hor. osc.
6,2 kΩ
1,5 kΩ
18 kΩ
35 kΩ
ref. voltage 2,7 V
to pin 16
4,7 μF
820 Ω
10 μF
150 nF
GROUND
TDA2577A
SUPPLY SWITCH
COINCIDENCE DETECTOR
250 μA
4 kΩ
1 kΩ
100 nF
SANDCASTLE PULSE GENERATOR
15 kΩ
8 kΩ
150 Ω
5,6 kΩ
5 kΩ
1 mA
2,5 V
flyback inverter
burst key inverter
sandcastle output pulse
START CIRCUIT STABILIZER
I16 > 4 mA
100 μF
start voltage hor. osc.
6,5 V
HORIZONTAL OSCILLATOR
200 Ω
6 kΩ
36 kΩ
2,7 nF
4,7 kΩ
horizontal freq. adj.
HORIZONTAL FLYBACK
4 V during start up
osc. ref. pulse
horizontal flyback
current inverter
0,9 mA
hor. output
47 nF
VIDEO TRANSMITTER IDENTIFICATION & MUTE OUTPUT
VCR
12 kΩ
220 Ω
identification
PHASE DETECTOR φ2
0,2 to 4 mA
horizontal flyback
0,8 V
4 kΩ
2,2 kΩ
2 kΩ
phase 2 detector
50/60 Hz switch
sandcastle
HORIZONTAL OUTPUT
5,4 kΩ
900 Ω
12 kΩ
15 V
6,8 kΩ
horizontal drive
220 μF
7Z86905

Fig. 2 TDA2577A circuit diagram.

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | | |
|---|---|---|---|---|
| Start current (pin 16) | $I_{16}$ | max. | 8 | mA |
| Supply voltage (pin 10) | $V_P = V_{10\text{-}9}$ | max. | 13,2 | V |
| Total power dissipation | $P_{tot}$ | max. | 1,1 | W |
| Storage temperature range | $T_{stg}$ | | −55 to + 150 | °C |
| Operating ambient temperature range | $T_{amb}$ | | −25 to + 65 | °C |

## THERMAL RESISTANCE

| | | | | |
|---|---|---|---|---|
| From junction to ambient in free air | $R_{th\ j\text{-}a}$ | typ. | 50 | K/W |

## CHARACTERISTICS

$I_{16}$ = 5 mA; $V_P$ = 12 V; $T_{amb}$ = 25 °C; unless otherwise specified

### Supply

| | | | | |
|---|---|---|---|---|
| Supply current at pin 16 | $I_{16}$ | | 4 to 8 | mA |
| Stabilized supply voltage (pin 16) | $V_{16\text{-}9}$ | typ. | 8,7 | V |
| | | | 8,0 to 9,5 | V |
| Supply current (pin 10) | $I_{10}$ | typ. | 55 | mA |
| | | < | 70 | mA |
| Supply voltage (pin 10) | $V_P = V_{10\text{-}9}$ | typ. | 12 | V |
| | | | 10 to 13,2 | V |

### **Video input** (pin 5)

| | | | | |
|---|---|---|---|---|
| Top-sync level | $V_{5\text{-}9}$ | typ. | 3,1 | V |
| | | | 1,5 to 3,75 | V |
| Sync pulse amplitude (peak-to-peak value) (note 1) | $V_{5\text{-}9(p\text{-}p)}$ | typ. | 0,6 | V |
| | | | 0,15 to 1 | V |
| Slicing level | | typ. | 50 | % |
| | | | 35 to 65 | % |
| Delay between video input and detector output | $t_1$ | typ. | 0,35 | µs |

### **Noise gate** (pin 5)

| | | | | |
|---|---|---|---|---|
| Switching level | $V_{5\text{-}9}$ | typ. | 0,7 | V |
| | | < | 1 | V |

### **First control loop** (sync to oscillator; pin 8)

| | | | | |
|---|---|---|---|---|
| Holding range | $\Delta f$ | typ. | ± 800 | Hz |
| Catching range | $\Delta f$ | typ. | ± 800 | Hz |
| | | | ± 600 to 1100 | Hz |
| Control sensitivity video with respect to oscillator, burst key and flyback pulse | | | | |
| for slow time constant | | typ. | 1 | kHz/µs |
| for fast time constant | | typ. | 2,75 | kHz/µs |

| | | | | |
|---|---|---|---|---|
| **Second control loop** (horizontal output to flyback; pin 14) | | | | |
| Control sensitivity; static (see note 2) | $\Delta t_d/\Delta t_o$ | typ. | 400 | µs/µs |
| Control range | $t_d$ | | 1 to 50 | µs |
| Controlled edge | negative | | | |
| **Phase adjustment** (via 2nd control loop; pin 14) | | | | |
| Control sensitivity | | typ. | 25 | µA/µs |
| Maximum permissible control current | $\pm I_{14}$ | $<$ | 50 | µA |
| **Horizontal oscillator** (pin 15) | | | | |
| Frequency (no sync) | $f_{osc}$ | typ. | 15 625 | Hz |
| Frequency spread ($C_{osc}$ = 2,2 nF; $R_{osc}$ = 40 kΩ) | $\Delta f_{osc}$ | $<$ | 4 | % |
| Frequency deviation between starting point of output signal and stabilized condition | $\Delta f_{osc}$ | typ.<br>$<$ | 6<br>8 | %<br>% |
| Temperature coefficient | TC | typ. | $1 \cdot 10^{-4}$ | $K^{-1}$ |
| **Horizontal output** (pin 11) | | | | |
| Output voltage; high level | $V_{11\text{-}9}$ | $<$ | 13,2 | V |
| Voltage at which protection starts | $V_{11\text{-}9}$ | | 13 to 15,8 | V |
| Output voltage; low level start condition at $I_{11}$ = 10 mA | $V_{11\text{-}9}$ | typ.<br>$<$ | 0,3<br>0,5 | V<br>V |
| normal condition at $I_{11}$ = 40 mA | $V_{11\text{-}9}$ | typ.<br>$<$ | 0,3<br>0,5 | V<br>V |
| Duty factor of output signal during starting (no phase shift; voltage at pin 11 low) | δ | typ. | 65 | % |
| Duty factor of output signal without flyback pulse | δ | typ. | 50<br>45 to 55 | %<br>% |
| Controlled edge | negative | | | |
| Duration of output pulse (see Fig. 3) | | | $t_d + t_o + 2{,}5$ | µs |
| **Sandcastle output pulse** (pin 17) | | | | |
| Output voltage during: burst key | $V_{17\text{-}9}$ | $>$ | 10 | V |
| horizontal blanking | $V_{17\text{-}9}$ | typ. | 4,6<br>4,2 to 5 | V<br>V |
| vertical blanking | $V_{17\text{-}9}$ | typ. | 2,5<br>2 to 3 | V<br>V |
| Pulse duration | | | | |
| burst key | $t_p$ | typ. | 4<br>3,6 to 4,4 | µs<br>µs |
| horizontal blanking | flyback pulse (see note 3) | | | |
| vertical blanking | | | | |
| for 50 Hz application ($-I_{12}$ : 0 to 0,1 mA) | | | 21 | lines |
| for 60 Hz application ($-I_{12}$ : typ. 0,2 mA) | | | 17 | lines |

**CHARACTERISTICS** (continued)

| | | | | |
|---|---|---|---|---|
| Delay between the start of the sync at the video input and the rising edge of the burst key pulse | $t_2$ | typ. | 4,9 | µs |
| | | | 4,5 to 5,3 | µs |

**Coincidence detector; video transmitter identification circuit; time constant switches** (pin 18); see also Fig. 2

| | | | | |
|---|---|---|---|---|
| Detector output current | $\pm I_{18}$ | typ. | 300 | µA |
| Voltage during noise (note 4) | $V_{18\text{-}9}$ | typ. | 0,3 | V |
| Voltage level for in-sync condition | $V_{18\text{-}9}$ | typ. | 7,5 | V |
| Switching level slow to fast | $V_{18\text{-}9}$ | typ. | 3,5 | V |
| | | | 3,2 to 3,8 | V |
| Switching level<br>mute function active; $\varphi_1$ fast to slow | $V_{18\text{-}9}$ | typ. | 1,2 | V |
| | | | 1,0 to 1,4 | V |
| vertical period counter 3 periods fast | $V_{18\text{-}9}$ | typ. | 0,12 | V |
| | | | 0,08 to 0,16 | V |
| Switching level slow to fast (locking) mute function inactive | $V_{18\text{-}9}$ | typ. | 1,7 | V |
| | | | 1,5 to 1,9 | V |
| Switching level fast to slow (locking) | $V_{18\text{-}9}$ | typ. | 5,0 | V |
| | | | 4,7 to 5,3 | V |
| Switching level for VCR (fast time constant) without mute function | $V_{18\text{-}9}$ | typ. | 8,6 | V |
| | | | 8,2 to 9,0 | V |

**Video transmitter identification output** (pin 13)

| | | | | |
|---|---|---|---|---|
| Output voltage active (no sync) at $I_{13} = 1$ mA | $V_{13\text{-}9}$ | > | 10 | V |
| | | typ. | 11 | V |
| Output voltage active (no sync) at $I_{13} = 5$ mA | $V_{13\text{-}9}$ | > | 7 | V |
| | | typ. | 10 | V |
| Output voltage inactive | $V_{13\text{-}9}$ | < | 0,5 | V |
| | | typ. | 0,1 | V |

**VCR switching** (pin 13)

| | | | | |
|---|---|---|---|---|
| Input current for fast time constant phase detector $\varphi_1$, with mute function active | $I_{13}$ | typ. | 0,6 | mA |
| | | | 0,4 to 0,8 | mA |

**Flyback input pulse** (pin 12)

| | | | | |
|---|---|---|---|---|
| Switching level | $V_{12\text{-}9}$ | typ. | 1 | V |
| Input current | $I_{12}$ | | 0,2 to 4 | mA |
| Input pulse amplitude (peak-to-peak value) | $V_{12\text{-}9(p\text{-}p)}$ | < | 12 | V |
| Input resistance | $R_{12\text{-}9}$ | typ. | 2,7 | kΩ |
| Delay time of sync pulse (measured in $\varphi_1$) to flyback at switching level; $t_{fl} = 12$ µs (see also note 2 and Fig. 4) | $t_o$ | typ. | 1,3 | µs |

| | | | | |
|---|---|---|---|---|
| **Duration of vertical blanking pulse** (pin 12) | | | | |
| Required input current (negative) | | | | |
| for 50 Hz application; 21 lines blanking | $-I_{12}$ | typ.<br>$>$ 0,15 to $<$ | 0,2<br>0,3 | mA<br>mA |
| for 60 Hz application; 17 lines blanking | $-I_{12}$ | $<$ | 0,1 | mA |
| Maximum allowed input current | $-I_{12}$ | $<$ | 0,4 | mA |
| **Vertical sawtooth generator** (pin 3) | | | | |
| Vertical frequency (no sync) | $f_s$ | typ. | 46 | Hz |
| Frequency spread ($C_{osc}$ = 680 nF; $R_{osc}$ = 180 kΩ; at + 26 V) | $\Delta f_s$ | $<$ | 4 | % |
| Synchronization range | | typ. | 22 | % |
| Input current at $V_{3\text{-}9}$ = 6 V | $I_3$ | $<$ | 2 | μA |
| Frequency shift for $V_P$ = 10 to 13 V | $\Delta f_s$ | $<$ | 0,2 | % |
| Temperature coefficient | TC | typ. | $1 \cdot 10^{-4}$ | $K^{-1}$ |
| **Comparator** (pin 2) | | | | |
| Input voltage; d.c. level | $V_{2\text{-}9}$ | typ. | 4,4<br>4,0 to 4,8 | V<br>V |
| a.c. level (peak-to-peak value) | $V_{2\text{-}9(p\text{-}p)}$ | typ. | 1,6 | V |
| Input current at $V_{2\text{-}9}$ = 6 V | $I_2$ | $<$ | 2 | μA |
| Sawtooth internal pre-correction (parabolic convex) | | typ. | 3 | % |
| **Vertical output stage; emitter follower** (pin 1) | | | | |
| Output voltage at $I_1$ = 10 mA | $V_{1\text{-}9}$ | typ. | 3,6<br>3,2 to 5 | V<br>V |
| Output current | $I_1$ | $<$ | 20 | mA |
| **Vertical guard circuit** | | | | |
| Activating voltage levels (vertical blanking level is 2,5 V) | | | | |
| switching level low | $V_{2\text{-}9}$ | typ. | 3<br>2,7 to 3,3 | V<br>V |
| switching level high | $V_{2\text{-}9}$ | typ. | 5,7<br>5,3 to 6,1 | V<br>V |

**Notes to characteristics**

1. Up to 1 V peak-to-peak the slicing level is constant; at amplitudes exceeding 1 V peak-to-peak the slicing level will increase.
2. $t_d$ = delay between negative transient of horizontal output pulse and the rising edge of the flyback pulse.
   $t_o$ = delay between the rising edge of the flyback pulse and the start of the current in $\varphi_1$ (pin 8).
3. The duration of the flyback pulse is measured at the input switching level, which is about 1 V ($t_{fl}$).
4. Depends on d.c. level at pin 5; value given applicable for $V_{5\text{-}9} \approx 5$ V.

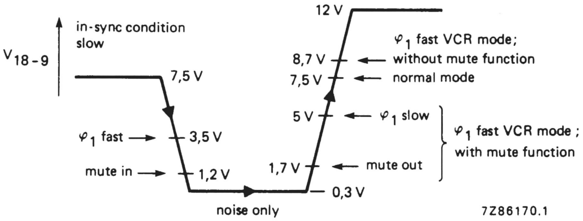


Fig. 3 Voltage levels at pin 18 ($V_{18\text{-}9}$).

## APPLICATION INFORMATION

The TDA2577A generates the signal for driving the horizontal deflection output circuit. It also contains a synchronized vertical sawtooth generator for direct drive of the vertical deflection output stage.

The horizontal oscillator and output stage can start operating on a very low supply current ($I_{16} \geqslant 4$ mA), which can be taken directly from the mains rectifier. Therefore, it is possible to derive the main supply (pin 10) from the horizontal deflection output stage. The duty factor of the horizontal output signal is about 65% during the starting-up procedure. After starting-up, the second phase detector ($\varphi_2$) is activated to control the timing of the negative-going edge of the horizontal output signal.

A bandgap reference voltage (6,5 V) is provided for supply and reference of the vertical oscillator and comparator stage.

The slicing level of the horizontal sync separator is independent of the amplitude of the sync pulse at the input. The resistor between pins 6 and 7 determines its value. A 4,7 kΩ resistor gives a slicing level at the middle of the sync pulse. The nominal top sync level at the input is 3,1 V. The amplitude selective noise inverter is activated at a level of 0,7 V.

Good stability is obtained by means of the two control loops. In the first loop, the phase of the horizontal sync signal is compared with a waveform of which the rising edge refers to the top of the horizontal oscillator signal. In the second loop, the phase of the flyback pulse is compared with another reference waveform, the timing of which is such that the top of the flyback pulse is situated symmetrically on the horizontal blanking interval of the video signal. Therefore the first loop can be designed for a good noise immunity, whereas the second loop can be as fast as desired for compensation of switch-off delays in the horizontal output stage.

The first phase detector is gated with a pulse derived from the horizontal oscillator signal. This gating (slow time constant) is switched off during catching. Also, the output current of the phase detector is increased fivefold, during the catching time and VCR conditions (fast time constant). The first phase detector is inhibited during the retrace time of the vertical oscillator.

The in-sync, out-of-sync or no video condition is detected by the video transmitter identification/coincidence detector circuit (pin 18). The voltage on pin 18 defines the time constant and gating of the first phase detector. The relationship between this voltage and the various switching levels is shown in Fig. 3. The complete survey of the switching actions is given in Table 1.

DEVELOPMENT SAMPLE DATA

## APPLICATION INFORMATION (continued)

**Table 1** Switching levels at pin 18.

| voltage at pin 18 | first phase detector $\varphi_1$ | | | | mute output at pin 13 | | receiving conditions |
|---|---|---|---|---|---|---|---|
| | time constant | | gating | | | | |
| | slow | fast | on | off | on | off | |
| 7,5 V | X | | X | | | X | video signal detected |
| 7,5 to 3,5 V | X | | X | | | X | video signal detected |
| 3,5 to 1,2 V | | X | | X | | X | video signal detected |
| 1,2 to 0,1 V | X | | X | | X | | noise only |
| 0,1 to 1,7 V | X | * | X | * | X | | new video signal detected |
| 1,7 to 5,0 V | | X | | X | | X | horizontal oscillator locked<br>VCR playback with mute function |
| 5,0 to 7,5 V | X | | X | | | X | horizontal oscillator locked |
| 8,7 V | | X | | X | | X | VCR playback without mute function |

Where: * = 3 vertical periods.

The stability of displayed video information (e.g. channel number), during noise only conditions, is improved by the first phase detector time constant being set to slow.

The average voltage level of the video input on pin 5 during noise only conditions should not exceed 5,5 V otherwise the time constant switch may be set to fast due to the average voltage level on pin 18 dropping below 0,1 V. When the voltage on pin 18 drops below 100 mV a counter is activated which sets the time constant switch to fast, and not gated for 3 vertical periods. This condition occurs when a new video signal is present at pin 5. When the horizontal oscillator is locked the voltage on pin 18 increases. Nominally a level of 5 V is reached within 15 ms (1 vertical period). The mute switching level of 1,2 V is reached within 5 ms ($C_{18}$ = 47 nF). If the video transmitter identification circuit is required to operate under VCR playback conditions the first phase detector can be set to fast by connecting a resistor of 180 kΩ between pin 18 and ground. Also a current of 0,6 mA into pin 13 sets the first phase detector to fast without affecting the mute output function (active HIGH with no video signal detected). For VCR playback without mute function, the first phase detector can be set to fast by connecting a resistor of 1 kΩ to the supply (pin 10).

The supply for the horizontal oscillator (pin 15) and horizontal output stage (pin 11) is derived from the voltage at pin 16 during the start condition. The horizontal output signal starts at a nominal supply current into pin 16 of 3,5 mA, which will result in a supply voltage of about 5,5 V (for guaranteed operation of all devices $I_{16} > 4$ mA). It is possible that the main supply voltage at pin 10 is 0 V during starting, so the main supply of the IC can be taken from the horizontal deflection output stage. The start of the other IC functions depends on the value of the main supply voltage at pin 10. At 5,5 V all IC functions start operating except the second phase detector (oscillator to flyback pulse). The output voltage of the second phase detector at pin 14 is clamped by means of an internally loaded n-p-n emitter follower. This ensures that the duty factor of the horizontal output signal (pin 11) remains at about 65%. The second phase detector will close if the supply voltage at pin 10 reaches 8,8 V. At this value the supply current for the horizontal oscillator and output stage is delivered by pin 10, which also causes the voltage at pin 16 to change to a stabilized 8,7 V. This change switches off the n-p-n emitter follower at pin 14 and activates the second phase detector. The supply voltage for the horizontal oscillator will, however, still be referred to the stabilized voltage at pin 16, and the duty factor of the output signal at pin 12 is at the value required by the delay at the horizontal deflection stage. Thus switch-off delays in the horizontal output stage are compensated. When no horizontal flyback signal is detected the duty factor of the horizontal output signal is 50%.

Horizontal picture shift is possible by externally charging or discharging the 47 nF capacitor connected to pin 14.

The IC also contains a synchronized vertical oscillator/sawtooth generator. The oscillator signal is connected to the internal comparator (the other side of which is connected to pin 2), via an inverter and amplitude divider stage. The output of the comparator drives an emitter-follower output stage at pin 1. For a linear sawtooth in the oscillator, the load resistor at pin 3 should be connected to a voltage source of 26 V or higher. The sawtooth amplitude is not influenced by the main supply at pin 10. The feedback signal is applied to pin 2 and compared to the sawtooth signal at pin 3. For an economical feedback circuit with less picture bounce the sawtooth signal is internally precorrected by 3% (convex) referred to pin 2. The linearity of the vertical deflection current depends upon the oscillator signal at pin 3 and the feedback signal at pin 2.

Synchronization of the vertical oscillator is inhibited when the mute output is present at pin 13.

To minimize the influence of the horizontal part on the vertical part a 6,5 V bandgap reference source is provided for supply and reference of the vertical oscillator and comparator.

The sandcastle pulse, generated at pin 17, has three different voltage levels. The highest level (11 V) can be used for burst gating and black level clamping. The second level (4,6 V) is obtained from the horizontal flyback pulse at pin 12 and used for horizontal blanking. The third level (2,5 V) is used for vertical blanking and is derived by counting the horizontal frequency pulses. For 50 Hz the blanking pulse duration is 21 lines and for 60 Hz it is 17 lines. The blanking pulse duration is set by the negative voltage value of the horizontal flyback pulse at pin 12.

The IC also incorporates a vertical guard circuit, which monitors the vertical feedback signal at pin 2. If this level is below 3 V or higher than 5,8 V, the guard circuit will insert a continuous level of 2,5 V into the sandcastle output signal. This will result in complete blanking of the screen if the sandcastle pulse is used for blanking in the TV set.

## APPLICATION INFORMATION (continued)

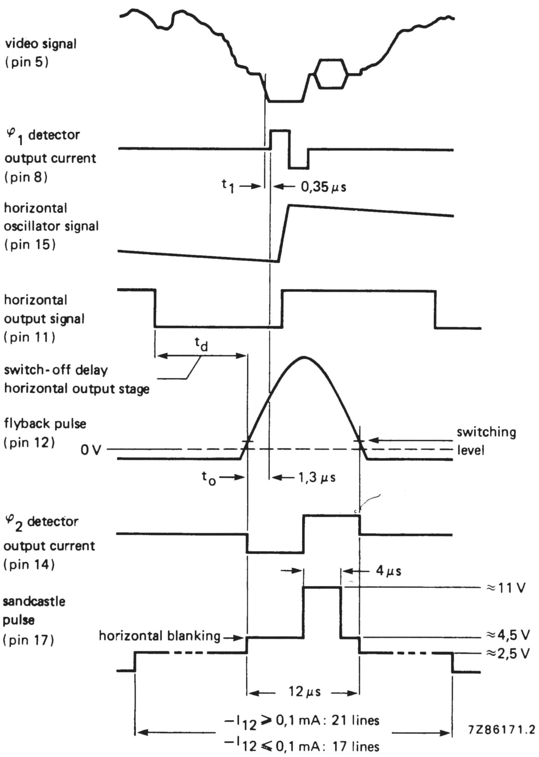

video signal
(pin 5)
$\varphi_1$ detector
output current
(pin 8)
$t_1$
0,35 μs
horizontal
oscillator signal
(pin 15)
horizontal
output signal
(pin 11)
$t_d$
switch-off delay
horizontal output stage
flyback pulse
(pin 12)
0 V
switching
level
$t_o$
1,3 μs
$\varphi_2$ detector
output current
(pin 14)
4 μs
sandcastle
pulse
(pin 17)
≈11 V
horizontal blanking
≈4,5 V
≈2,5 V
12 μs
$-I_{12} \geqslant 0,1$ mA: 21 lines
$-I_{12} \leqslant 0,1$ mA: 17 lines
7Z86171.2

Fig. 4 Timing diagram of the TDA2577A.

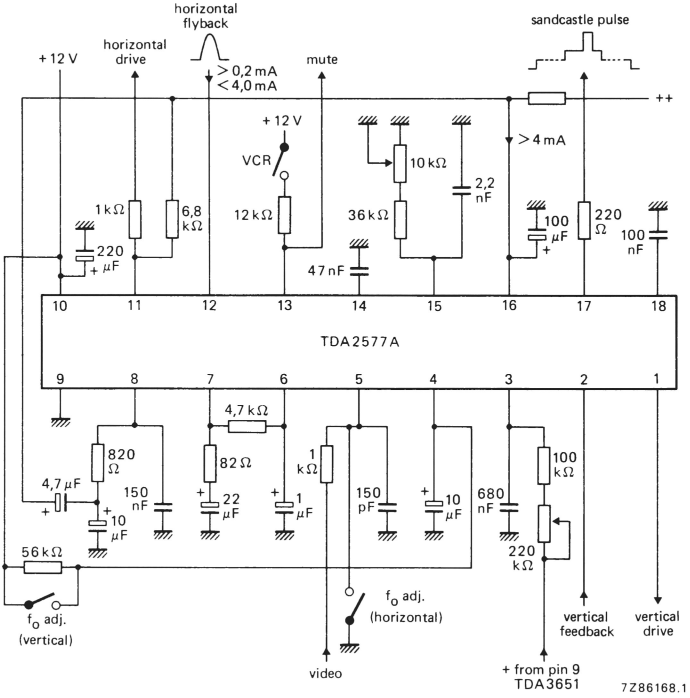

horizontal flyback
sandcastle pulse
+ 12 V
horizontal drive
> 0,2 mA
< 4,0 mA
mute
++
+ 12 V
VCR
10 kΩ
> 4 mA
2,2 nF
1 kΩ
6,8 kΩ
12 kΩ
36 kΩ
100 μF
220 Ω
100 nF
220 μF
47 nF
10
11
12
13
14
15
16
17
18
TDA2577A
9
8
7
6
5
4
3
2
1
4,7 kΩ
820 Ω
82 Ω
1 kΩ
100 kΩ
4,7 μF
150 nF
22 μF
1 μF
150 pF
10 μF
680 nF
10 μF
56 kΩ
220 kΩ
f<sub>o</sub> adj. (vertical)
f<sub>o</sub> adj. (horizontal)
vertical feedback
vertical drive
video
+ from pin 9 TDA3651
7Z86168.1

Fig. 5 Typical application circuit diagram; for combination of the TDA2577A with the TDA3651 see Fig. 7.

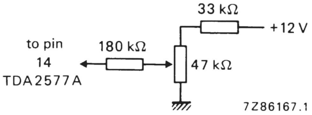

33 kΩ
+12 V
to pin 14 TDA2577A
180 kΩ
47 kΩ
7Z86167.1

Fig. 6 Circuit configuration at pin 14 for phase adjustment.

**APPLICATION INFORMATION** (continued)

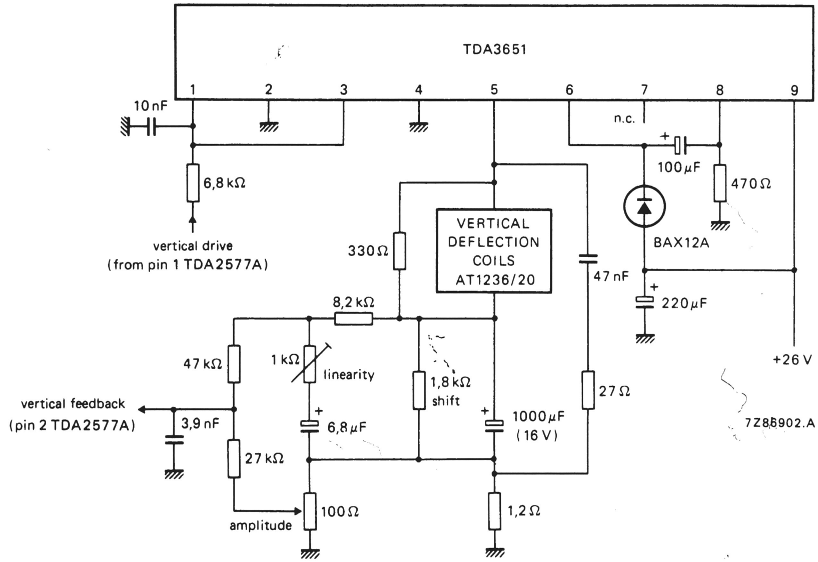

TDA3651
1
2
3
4
5
6
7
8
9
10 nF
n.c.
100 μF
470 Ω
6,8 kΩ
vertical drive
(from pin 1 TDA2577A)
330 Ω
VERTICAL
DEFLECTION
COILS
AT1236/20
BAX12A
47 nF
220 μF
8,2 kΩ
47 kΩ
1 kΩ
linearity
1,8 kΩ
shift
+26 V
27 Ω
vertical feedback
(pin 2 TDA2577A)
3,9 nF
6,8 μF
1000 μF
(16 V)
7Z86902.A
27 kΩ
100 Ω
amplitude
1,2 Ω

Fig. 7 Typical application circuit diagram of the TDA3651 (vertical output), when used in combination with the TDA2577A (90° application).

# SYNCHRONIZATION CIRCUIT
# WITH VERTICAL OSCILLATOR AND DRIVER STAGES

## GENERAL DESCRIPTION

The TDA2578A separates the vertical and horizontal sync pulses from the composite TV video signal and uses them to synchronize horizontal and vertical oscillators.

### Features

- Horizontal sync separator and noise inverter
- Horizontal oscillator
- Horizontal output stage
- Horizontal phase detector (sync to oscillator)
- Time constant switch for phase detector (fast time constant during catching)
- Slow time constant for noise only conditions
- Time constant externally switchable (e.g. fast for VCR)
- Inhibit of horizontal phase detector and video transmitter identification circuit during vertical oscillator flyback
- Second phase detector ($\varphi_2$) for storage compensation of horizontal deflection stage
- Sandcastle pulse generator (3-levels)
- Video transmitter identification circuit
- Stabilizer and supply circuit for starting the horizontal oscillator and output stage directly from the mains rectifier
- Duty factor of horizontal output pulse is 50% when flyback pulse is absent
- Vertical sync separator
- Bandgap 6,5 V reference voltage for vertical oscillator and comparator
- Synchronized vertical oscillator/sawtooth generator
  (synchronization inhibited when no video transmitter is detected)
- Internal circuit for 6% parabolic pre-correction of the oscillator/sawtooth generator. Comparator supplied with pre-corrected sawtooth and external feedback input
- Vertical driver stage
- Vertical blanking pulse generator
- 50/60 Hz detector
- 50/60 Hz identification output
- Automatic amplitude adjustment for 60 Hz
- Automatic adjustment of blanking pulse duration
  (50 Hz: 21 lines; 60 Hz: 17 lines)
- Vertical guard curcuit

## QUICK REFERENCE DATA

| | | | | |
|---|---|---|---|---|
| **Supply** | | | | |
| Minimum current required to start horizontal oscillator and output stage (pin 16) | $I_{16}$ | > | 4 | mA |
| Main supply voltage (pin 10) | $V_P = V_{10\text{-}9}$ | typ. | 12 | V |
| Supply current | $I_P = I_{10}$ | typ. | 55 | mA |
| **Input signals** | | | | |
| Sync pulse input voltage (peak-to-peak value; negative-going) | $V_{5\text{-}9(p\text{-}p)}$ | | 0,15 to 1 | V |
| **Output signals** | | | | |
| Horizontal output pulse (open collector) at $I_{11}$ = 40 mA | $V_{11\text{-}9}$ | < | 0,5 | V |
| Vertical output pulse (emitter-follower) at $I_1$ = 10 mA | $V_{1\text{-}9}$ | > | 4 | V |

## PACKAGE OUTLINE

18-lead DIL; plastic (SOT-102HE).

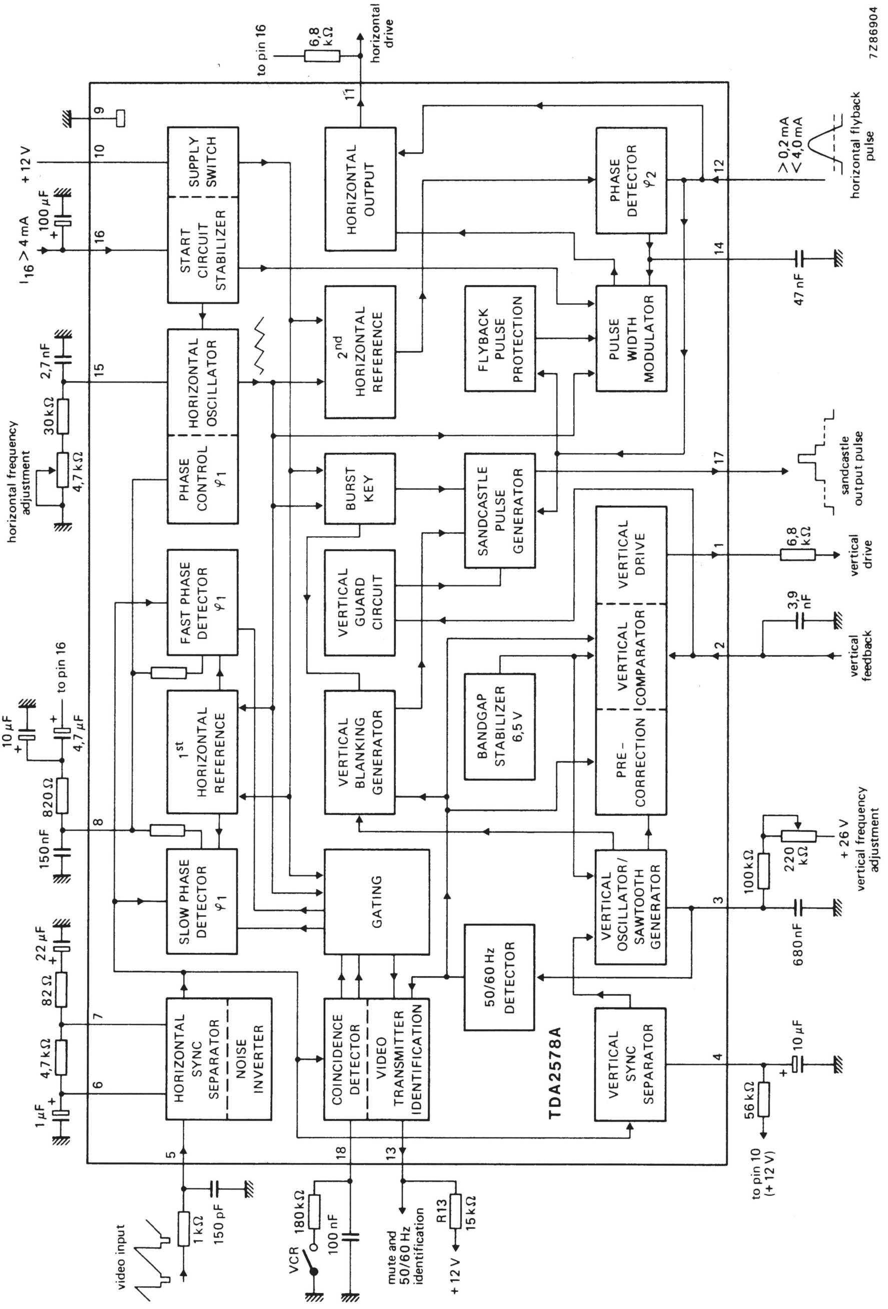

TDA2578A
SUPPLY SWITCH
START CIRCUIT STABILIZER
HORIZONTAL OSCILLATOR
PHASE CONTROL φ1
FAST PHASE DETECTOR φ1
1st HORIZONTAL REFERENCE
SLOW PHASE DETECTOR φ1
HORIZONTAL SYNC SEPARATOR
NOISE INVERTER
HORIZONTAL OUTPUT
2nd HORIZONTAL REFERENCE
BURST KEY
VERTICAL GUARD CIRCUIT
VERTICAL BLANKING GENERATOR
GATING
COINCIDENCE DETECTOR
VIDEO TRANSMITTER IDENTIFICATION
PHASE DETECTOR φ2
FLYBACK PULSE PROTECTION
PULSE WIDTH MODULATOR
SANDCASTLE PULSE GENERATOR
BANDGAP STABILIZER 6,5 V
50/60 Hz DETECTOR
VERTICAL DRIVE
VERTICAL COMPARATOR
PRE-CORRECTION
VERTICAL OSCILLATOR/ SAWTOOTH GENERATOR
VERTICAL SYNC SEPARATOR
+12 V
I16 > 4 mA
100 μF
2,7 nF
30 kΩ
4,7 kΩ
horizontal frequency adjustment
10 μF
4,7 μF
to pin 16
820 Ω
150 nF
22 μF
82 Ω
4,7 kΩ
1 μF
video input
1 kΩ
150 pF
VCR
180 kΩ
100 nF
mute and 50/60 Hz identification
R13
15 kΩ
+12 V
to pin 16
6,8 kΩ
horizontal drive
>0,2 mA
<4,0 mA
horizontal flyback pulse
47 nF
sandcastle output pulse
6,8 kΩ
vertical drive
3,9 nF
vertical feedback
100 kΩ
220 kΩ
+26 V
vertical frequency adjustment
680 nF
10 μF
56 kΩ
to pin 10 (+12 V)
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
7Z86904

Fig. 1 Block diagram.

**DEVELOPMENT SAMPLE DATA**

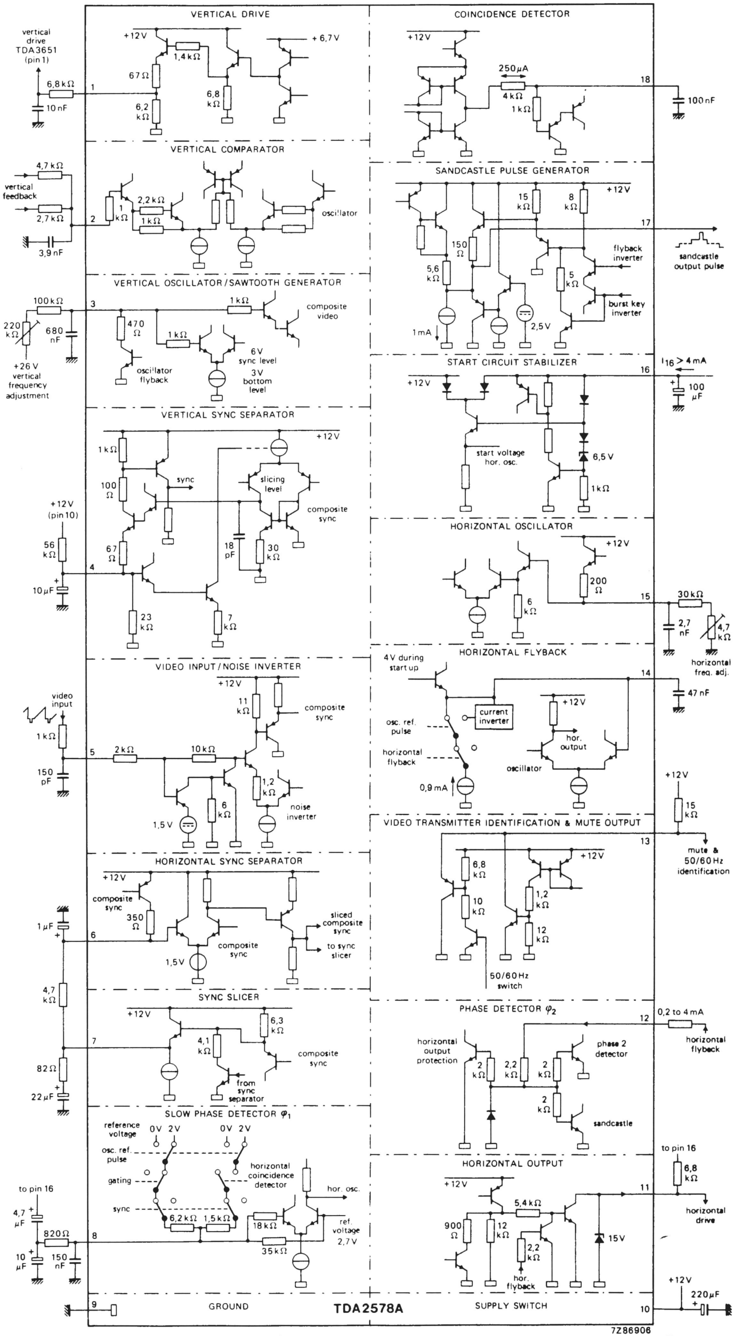

VERTICAL DRIVE
vertical drive TDA3651 (pin 1)
6,8 kΩ
10 nF
+12 V
1,4 kΩ
67 Ω
6,2 kΩ
6,8 kΩ
+ 6,7 V
COINCIDENCE DETECTOR
250 μA
4 kΩ
1 kΩ
100 nF
VERTICAL COMPARATOR
4,7 kΩ
vertical feedback
2,7 kΩ
3,9 nF
2,2 kΩ
1 kΩ
oscillator
SANDCASTLE PULSE GENERATOR
15 kΩ
8 kΩ
150 Ω
5,6 kΩ
5 kΩ
1 mA
2,5 V
flyback inverter
burst key inverter
sandcastle output pulse
VERTICAL OSCILLATOR / SAWTOOTH GENERATOR
100 kΩ
220 kΩ
680 nF
+26 V vertical frequency adjustment
470 Ω
oscillator flyback
composite video
6 V sync level
3 V bottom level
START CIRCUIT STABILIZER
$I_{16} > 4$ mA
100 μF
start voltage hor. osc.
6,5 V
VERTICAL SYNC SEPARATOR
+12 V (pin 10)
56 kΩ
10 μF
100 Ω
67 Ω
23 kΩ
7 kΩ
sync
slicing level
composite sync
18 pF
30 kΩ
HORIZONTAL OSCILLATOR
200 Ω
6 kΩ
30 kΩ
2,7 nF
4,7 kΩ
horizontal freq. adj.
VIDEO INPUT / NOISE INVERTER
video input
1 kΩ
150 pF
2 kΩ
10 kΩ
11 kΩ
1,5 V
6 kΩ
1,2 kΩ
noise inverter
HORIZONTAL FLYBACK
4 V during start up
current inverter
osc. ref. pulse
horizontal flyback
0,9 mA
hor. output
oscillator
47 nF
VIDEO TRANSMITTER IDENTIFICATION & MUTE OUTPUT
15 kΩ
mute & 50/60 Hz identification
10 kΩ
12 kΩ
50/60 Hz switch
HORIZONTAL SYNC SEPARATOR
1 μF
350 Ω
sliced composite sync
to sync slicer
SYNC SLICER
4,7 kΩ
82 Ω
22 μF
4,1 kΩ
6,3 kΩ
from sync separator
PHASE DETECTOR $\varphi_2$
0,2 to 4 mA
horizontal output protection
2 kΩ
2,2 kΩ
phase 2 detector
sandcastle
SLOW PHASE DETECTOR $\varphi_1$
reference voltage
0 V 2 V
gating
horizontal coincidence detector
hor. osc.
6,2 kΩ
1,5 kΩ
18 kΩ
35 kΩ
ref. voltage 2,7 V
to pin 16
4,7 μF
820 Ω
10 μF
150 nF
HORIZONTAL OUTPUT
900 Ω
12 kΩ
5,4 kΩ
2,2 kΩ
hor. flyback
15 V
6,8 kΩ
horizontal drive
GROUND
TDA2578A
SUPPLY SWITCH
220 μF
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
7Z86906

Fig. 2 TDA2578A circuit diagram.

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | | |
|---|---|---|---|---|
| Start current (pin 16) | $I_{16}$ | max. | 8 | mA |
| Supply voltage (pin 10) | $V_P = V_{10\text{-}9}$ | max. | 13,2 | V |
| Total power dissipation | $P_{tot}$ | max. | 1,1 | W |
| Storage temperature range | $T_{stg}$ | | −55 to + 150 | °C |
| Operating ambient temperature range | $T_{amb}$ | | −25 to + 65 | °C |

## THERMAL RESISTANCE

| | | | | |
|---|---|---|---|---|
| From junction to ambient in free air | $R_{th\ j\text{-}a}$ | typ. | 50 | K/W |

## CHARACTERISTICS

$I_{16} = 5$ mA; $V_P = 12$ V; $T_{amb} = 25$ °C; unless otherwise specified

| | | | | |
|---|---|---|---|---|
| **Supply** | | | | |
| Supply current at pin 16 | $I_{16}$ | | 4 to 8 | mA |
| Stabilized supply voltage (pin 16) | $V_{16\text{-}9}$ | typ. | 8,7 | V |
| | | | 8,0 to 9,5 | V |
| Supply current (pin 10) | $I_{10}$ | typ. | 55 | mA |
| | | < | 70 | mA |
| Supply voltage (pin 10) | $V_P = V_{10\text{-}9}$ | typ. | 12 | V |
| | | | 10 to 13,2 | V |
| **Video input** (pin 5) | | | | |
| Top-sync level | $V_{5\text{-}9}$ | typ. | 3,1 | V |
| | | | 1,5 to 3,75 | V |
| Sync pulse amplitude (peak-to-peak value) (note 1) | $V_{5\text{-}9(p\text{-}p)}$ | typ. | 0,6 | V |
| | | | 0,15 to 1 | V |
| Slicing level | | typ. | 50 | % |
| | | | 35 to 65 | % |
| Delay between video input and detector output | $t_1$ | typ. | 0,35 | μs |
| **Noise gate** (pin 5) | | | | |
| Switching level | $V_{5\text{-}9}$ | typ. | 0,7 | V |
| | | < | 1 | V |
| **First control loop** (sync to oscillator; pin 8) | | | | |
| Holding range | $\Delta f$ | typ. | ± 800 | Hz |
| Catching range | $\Delta f$ | typ. | ± 800 | Hz |
| | | | ± 600 to 1100 | Hz |
| Control sensitivity video with respect to oscillator, burst key and flyback pulse | | | | |
| for slow time constant | | typ. | 1 | kHz/μs |
| for fast time constant | | typ. | 2,75 | kHz/μs |

**Second control loop** (horizontal output to flyback; pin 14)

| | | | | |
|---|---|---|---|---|
| Control sensitivity; static (see note 2) | $\Delta t_d/\Delta t_o$ | typ. | 400 | μs/μs |
| Control range | $t_d$ | | 1 to 45 | μs |
| Controlled edge | positive | | | |

**Phase adjustment** (via 2nd control loop; pin 14)

| | | | | |
|---|---|---|---|---|
| Control sensitivity | | typ. | 25 | μA/μs |
| Maximum permissible control current | $\pm I_{14}$ | < | 50 | μA |

**Horizontal oscillator** (pin 15)

| | | | | |
|---|---|---|---|---|
| Frequency (no sync) | $f_{osc}$ | typ. | 15 625 | Hz |
| Frequency spread ($C_{osc}$ = 2,7 nF; $R_{osc}$ = 33 kΩ; no sync) | $\Delta f_{osc}$ | < | 4 | % |
| Frequency deviation between starting point of output signal and stabilized condition | $\Delta f_{osc}$ | typ.<br>< | 6<br>8 | %<br>% |
| Temperature coefficient | TC | typ. | $1 \cdot 10^{-4}$ | $K^{-1}$ |

**Horizontal output** (pin 11)

| | | | | |
|---|---|---|---|---|
| Output voltage; high level | $V_{11\text{-}9}$ | < | 13,2 | V |
| Voltage at which protection starts | $V_{11\text{-}9}$ | | 13 to 15,8 | V |
| Output voltage; low level | | | | |
| start condition at $I_{11}$ = 10 mA | $V_{11\text{-}9}$ | typ.<br>< | 0,3<br>0,5 | V<br>V |
| normal condition at $I_{11}$ = 40 mA | $V_{11\text{-}9}$ | typ.<br>< | 0,3<br>0,5 | V<br>V |
| Duty factor of output signal during starting (no phase shift) $I_{16}$ = 4 mA (voltage at pin 11 low) | $\delta$ | typ. | 65 | % |
| Duty factor of output signal without flyback pulse | $\delta$ | typ.<br> | 50<br>45 to 55 | %<br>% |
| Controlled edge | positive | | | |
| Duration of output pulse (see Fig. 4) | $t_d$ + horizontal flyback pulse | | | |

**Sandcastle output pulse** (pin 17)

| | | | | |
|---|---|---|---|---|
| Output voltage during: | | | | |
| burst key | $V_{17\text{-}9}$ | > | 10 | V |
| horizontal blanking | $V_{17\text{-}9}$ | typ.<br> | 4,6<br>4,2 to 5 | V<br>V |
| vertical blanking | $V_{17\text{-}9}$ | typ.<br> | 2,5<br>2 to 3 | V<br>V |
| Pulse duration | | | | |
| burst key | $t_p$ | typ.<br> | 4<br>3,6 to 4,4 | μs<br>μs |
| horizontal blanking | flyback pulse (see note 3) | | | |
| vertical blanking | | | | |
| at 50 Hz | 21 lines | | | |
| at 60 Hz | 17 lines | | | |

## CHARACTERISTICS (continued)

| | | | | |
|---|---|---|---|---|
| Delay between the start of the sync at the video input and the rising edge of the burst key pulse | $t_2$ | typ. | 4,9 | μs |
| | | | 4,5 to 5,3 | μs |

**Coincidence detector; video transmitter identification circuit; time constant switches** (pin 18); see also Fig. 3

| | | | | |
|---|---|---|---|---|
| Detector output current | $\pm I_{18}$ | typ. | 300 | μA |
| Voltage during noise (note 4) | $V_{18\text{-}9}$ | typ. | 0,3 | V |
| Voltage level for in-sync condition | $V_{18\text{-}9}$ | typ. | 7,5 | V |
| Switching level slow to fast | $V_{18\text{-}9}$ | typ. | 3,5 | V |
| | | | 3,2 to 3,8 | V |
| Switching level<br>mute function active; $\varphi_1$ fast to slow | $V_{18\text{-}9}$ | typ. | 1,2 | V |
| | | | 1,0 to 1,4 | V |
| vertical period counter<br>3 periods fast | $V_{18\text{-}9}$ | typ. | 0,12 | V |
| | | | 0,08 to 0,16 | V |
| Switching level slow to fast (locking)<br>mute function inactive | $V_{18\text{-}9}$ | typ. | 1,7 | V |
| | | | 1,5 to 1,9 | V |
| Switching level fast to slow (locking) | $V_{18\text{-}9}$ | typ. | 5,0 | V |
| | | | 4,7 to 5,3 | V |
| Switching level for VCR (fast time constant)<br>without mute function | $V_{18\text{-}9}$ | typ. | 8,6 | V |
| | | | 8,2 to 9,0 | V |

**Video transmitter identification output** (pin 13)

| | | | | |
|---|---|---|---|---|
| Output voltage active (no sync) at $I_{13}$ = 1 mA | $V_{13\text{-}9}$ | < | 0,5 | V |
| | | typ. | 0,3 | V |
| Sink current active (no sync) | $I_{13}$ | ⩽ | 5 | mA |
| Output current inactive (sync: 50 Hz) | $I_{13}$ | < | 1 | μA |

**50/60 Hz identification** (pin 13)

| | | | | |
|---|---|---|---|---|
| R13 = 15 kΩ to + 12 V (note 5)<br>at f = 50 Hz (in sync condition) | $V_{13\text{-}9}$ | typ. | $V_{10\text{-}9}$ | V |
| at f = 60 Hz (in sync condition) | $V_{13\text{-}9}$ | typ. | 7,6 | V |
| | | | 7,2 to 8 | V |

**Flyback input pulse** (pin 12)

| | | | | |
|---|---|---|---|---|
| Switching level | $V_{12\text{-}9}$ | typ. | 1 | V |
| Input current | $I_{12}$ | | 0,2 to 4 | mA |
| Input pulse amplitude (peak-to-peak value) | $V_{12\text{-}9(p\text{-}p)}$ | < | 12 | V |
| Input resistance | $R_{12\text{-}9}$ | typ. | 2,7 | kΩ |
| Delay time of sync pulse (measured in $\varphi_1$) to flyback at switching level; $t_{fl}$ = 12 μs (see also note 2 and Fig. 4) | $t_o$ | typ. | 1,3 | μs |

**Vertical sawtooth generator** (pin 3)

| | | | | |
|---|---|---|---|---|
| Vertical frequency (no sync) | $f_s$ | typ. | 46 | Hz |
| Frequency spread ($C_{osc}$ = 680 nF; $R_{osc}$ = 180 kΩ; at + 26 V) | $\Delta f_s$ | < | 4 | % |
| Synchronization range (note 6) | | typ. | 33 | % |
| Input current at $V_{3\text{-}9}$ = 6 V | $I_3$ | < | 3 | μA |
| Frequency shift for $V_P$ = 10 to 13 V | $\Delta f_s$ | < | 0,2 | % |
| Temperature coefficient | TC | typ. | $1 \cdot 10^{-4}$ | $K^{-1}$ |

**Comparator** (pin 2)

| | | | | |
|---|---|---|---|---|
| Input voltage; d.c. level | $V_{2\text{-}9}$ | typ. | 4,4 | V |
| | | | 4,0 to 4,8 | V |
| a.c. level (peak-to-peak value) | $V_{2\text{-}9(p\text{-}p)}$ | typ. | 0,8 | V |
| Input current at $V_{2\text{-}9}$ = 6 V | $I_2$ | < | 2 | μA |
| Sawtooth internal pre-correction (parabolic convex) | | typ. | 6 | % |

**Vertical output stage; emitter follower** (pin 1)

| | | | | |
|---|---|---|---|---|
| Output voltage at $I_1$ = 10 mA | $V_{1\text{-}9}$ | typ. | | V |
| | | | 3,2 to 5 | V |
| Output current | $I_1$ | < | 20 | mA |

**Vertical guard circuit**

| | | | | |
|---|---|---|---|---|
| Activating voltage levels (vertical blanking level is 2,5 V) | | | | |
| switching level low | $V_{2\text{-}9}$ | typ. | 3,35 | V |
| | | | 3,0 to 3,7 | V |
| switching level high | $V_{2\text{-}9}$ | typ. | 5,15 | V |
| | | | 4,75 to 5,55 | V |

**Notes to characteristics**

1. Up to 1 V peak-to-peak the slicing level is constant; at amplitudes exceeding 1 V peak-to-peak the slicing level will increase.
2. $t_d$ = delay between positive transient of horizontal output pulse and the rising edge of the flyback pulse.
   $t_o$ = delay between the rising edge of the flyback pulse and the start of the current in $\varphi_1$ (pin 8).
3. The duration of the flyback pulse is measured at the input switching level, which is about 1 V ($t_{fl}$).
4. Depends on d.c. level at pin 5; value given applicable for $V_{5\text{-}9} \approx 5$ V.
5. For 60 Hz a p-n-p emitter clamp is activated.
6. When $f_o$ = 46 Hz the 50/60 Hz detector switches over to 60 Hz; video input signal at pin 5 ≈ 55 Hz.

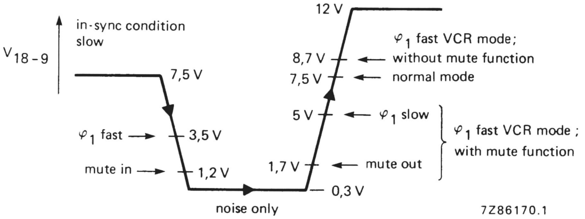

V18-9
in-sync condition
slow
7,5 V
φ1 fast
3,5 V
mute in
1,2 V
noise only
0,3 V
1,7 V
mute out
5 V
φ1 slow
φ1 fast VCR mode ;
with mute function
7,5 V
normal mode
8,7 V
φ1 fast VCR mode;
without mute function
12 V
7Z86170.1

Fig. 3 Voltage levels at pin 18 ($V_{18\text{-}9}$).

## APPLICATION INFORMATION

The TDA2578A generates the signal for driving the horizontal deflection output circuit. It also contains a synchronized vertical sawtooth generator for direct drive of the vertical deflection output stage.

The horizontal oscillator and output stage can start operating on a very low supply current ($I_{16} \geqslant 4$ mA), which can be taken directly from the mains rectifier. Therefore, it is possible to derive the main supply (pin 10) from the horizontal deflection output stage. The duty factor of the horizontal output signal is about 65% during the starting-up procedure. After starting-up, the second phase detector ($\varphi_2$) is activated to control the timing of the positive-going edge of the horizontal output signal.

A bandgap reference voltage (6,5 V) is provided for supply and reference of the vertical oscillator and comparator stage.

The slicing level of the horizontal sync separator is independent of the amplitude of the sync pulse at the input. The resistor between pins 6 and 7 determines its value. A 4,7 kΩ resistor gives a slicing level at the middle of the sync pulse. The nominal top sync level at the input is 3,1 V. The amplitude selective noise inverter is activated at a level of 0,7 V.

Good stability is obtained by means of the two control loops. In the first loop, the phase of the horizontal sync signal is compared with a waveform of which the rising edge refers to the top of the horizontal oscillator signal. In the second loop, the phase of the flyback pulse is compared with another reference waveform, the timing of which is such that the top of the flyback pulse is situated symmetrically on the horizontal blanking internal of the video signal. Therefore the first loop can be designed for a good noise immunity, whereas the second loop can be as fast as desired for compensation of switch-off delays in the horizontal output stage.

The first phase detector is gated with a pulse derived from the horizontal oscillator signal. This gating (slow time constant) is switched off during catching. Also, the output current of the phase detector is increased fivefold, during the catching time and VCR conditions (fast time constant). The first phase detector is inhibited during the retrace time of the vertical oscillator.

The in-sync, out-of-sync or no video condition is detected by the video transmitter identification/coincidence detector circuit (pin 18). The voltage on pin 18 defines the time constant and gating of the first phase detector. The relationship between this voltage and the various switching levels is shown in Fig. 3. The complete survey of the switching actions is given in Table 1.

**Table 1** Switching levels at pin 18.

| voltage at pin 18 | first phase detector $\varphi_1$ | | | | mute output at pin 13 | | receiving conditions |
|---|---|---|---|---|---|---|---|
| | time constant | | gating | | | | |
| | slow | fast | on | off | on | off | |
| 7,5 V | X | | X | | | X | video signal detected |
| 7,5 to 3,5 V | X | | X | | | X | video signal detected |
| 3,5 to 1,2 V | | X | | X | | X | video signal detected |
| 1,2 to 0,1 V | X | | X | | X | | noise only |
| 0,1 to 1,7 V | X | * | X | * | X | | new video signal detected |
| 1,7 to 5,0 V | | X | | X | | X | horizontal oscillator locked<br>VCR playback with mute function |
| 5,0 to 7,5 V | X | | X | | | X | horizontal oscillator locked |
| 8,7 V | | X | | X | | X | VCR playback without mute function |

Where: * = 3 vertical periods.

**APPLICATION INFORMATION** (continued)

The stability of displayed video information (e.g. channel number), during noise only conditions, is improved by the first phase detector time constant being set to slow.

The average voltage level of the video input on pin 5 during noise only conditions should not exceed 5,5 V otherwise the time constant switch may be set to fast due to the average voltage level on pin 18 dropping below 0,1 V. When the voltage on pin 18 drops below 100 mV a counter is activated which sets the time constant switch to fast, and not gated for 3 vertical periods. This condition occurs when a new video signal is present at pin 5. When the horizontal oscillator is locked the voltage on pin 18 increases. Nominally a level of 5 V is reached within 15 ms (1 vertical period). The mute switching level of 1,2 V is reached within 5 ms ($C_{18}$ = 47 nF). If the video transmitter identification circuit is required to operate under VCR playback conditions the first phase detector can be set to fast by connecting a resistor of 180 kΩ between pin 18 and ground (see Fig. 7).

The supply for the horizontal oscillator (pin 15) and horizontal output stage (pin 11) is derived from the voltage at pin 16 during the start condition. The horizontal output signal starts at a nominal supply current into pin 16 of 3,6 mA, which will result in a supply voltage of about 5,5 V (for guaranteed operation of all devices $I_{16} > 4$ mA). It is possible that the main supply voltage at pin 10 is 0 V during starting, so the main supply of the IC can be taken from the horizontal deflection output stage. The start of the other IC functions depends on the value of the main supply voltage at pin 10. At 5,5 V all IC functions start operating except the second phase detector (oscillator to flyback pulse). The output voltage of the second phase detector at pin 14 is clamped by means of an internally loaded n-p-n emitter follower. This ensures that the duty factor of the horizontal output signal (pin 11) remains at about 65%. The second phase detector will close if the supply voltage at pin 10 reaches 8,8 V. At this value the supply current for the horizontal oscillator and output stage is delivered by pin 10, which also causes the voltage at pin 16 to change to a stabilized 8,7 V. This change switches off the n-p-n emitter follower at pin 14 and activates the second phase detector. The supply voltage for the horizontal oscillator will, however, still be referred to the stabilized voltage at pin 16, and the duty factor of the output signal at pin 12 is at the value required by the delay at the horizontal deflection stage. Thus switch-off delays in the horizontal output stage are compensated. When no horizontal flyback signal is detected the duty factor of the horizontal output signal is 50%.

Horizontal picture shift is possible by externally charging or discharging the 47 nF capacitor connected to pin 14.

The IC also contains a synchronized vertical oscillator/sawtooth generator. The oscillator signal is connected to the internal comparator (the other side of which is connected to pin 2), via an inverter and amplitude divider stage. The output of the comparator drives an emitter-follower output stage at pin 1. For a linear sawtooth in the oscillator, the load resistor at pin 3 should be connected to a voltage source of 26 V or higher. The sawtooth amplitude is not influenced by the main supply at pin 10. The feedback signal is applied to pin 2 and compared to the sawtooth signal at pin 3. For an economical feedback circuit with less picture bounce the sawtooth signal is internally pre-corrected by 6% (convex) referred to pin 2. The linearity of the vertical deflection current depends upon the oscillator signal at pin 3 and the feedback signal at pin 2.

Synchronization of the vertical oscillator is inhibited when the mute output is present at pin 13.

To minimize the influence of the horizontal part on the vertical part a 6,7 V bandgap reference source is provided for supply and reference of the vertical oscillator and comparator.

The sandcastle pulse, generated at pin 17, has three different voltage levels. The highest level (11 V) can be used for burst gating and black level clamping. The second level (4,6 V) is obtained from the horizontal flyback pulse at pin 12 and used for horizontal blanking. The third level (2,5 V) is used for vertical blanking and is derived by counting the horizontal frequency pulses. For 50 Hz the blanking pulse duration is 21 lines and for 60 Hz it is 17 lines. The blanking pulse duration and sawtooth amplitude is automatically adjusted via the 50/60 Hz detector.

The IC also incorporates a vertical guard circuit, which monitors the vertical feedback signal at pin 2. If this level is below 3,35 V or higher than 5,15 V, the guard circuit will insert a continuous level of 2,5 V into the sandcastle output signal. This will result in complete blanking of the screen if the sandcastle pulse is used for blanking in the TV set.

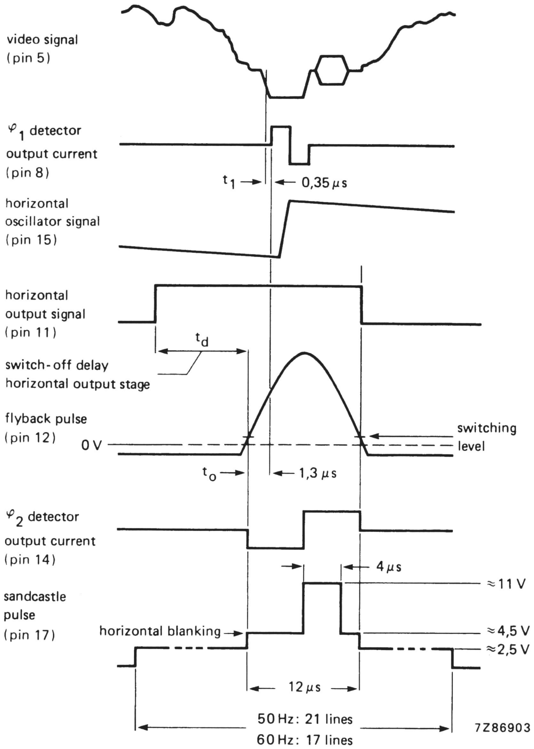
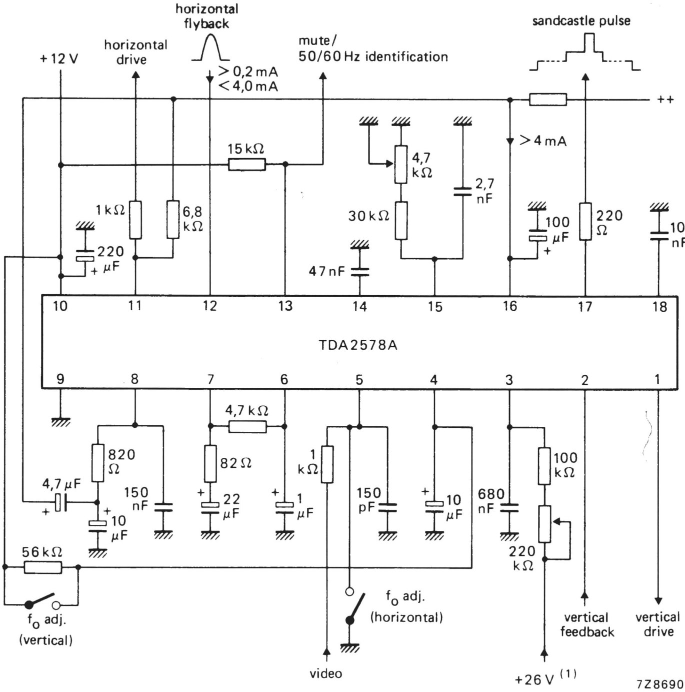

video signal (pin 5)
$\varphi_1$ detector output current (pin 8)
$t_1$
0,35 μs
horizontal oscillator signal (pin 15)
horizontal output signal (pin 11)
$t_d$
switch-off delay horizontal output stage
flyback pulse (pin 12)
0 V
switching level
$t_0$
1,3 μs
$\varphi_2$ detector output current (pin 14)
4 μs
sandcastle pulse (pin 17)
horizontal blanking
≈11 V
≈4,5 V
≈2,5 V
12 μs
50 Hz: 21 lines
60 Hz: 17 lines
7Z86903

Fig. 4 Timing diagram of the TDA2578A.

DEVELOPMENT SAMPLE DATA

## APPLICATION INFORMATION (continued)


horizontal flyback
sandcastle pulse
+12 V
horizontal drive
mute/
50/60 Hz identification
> 0,2 mA
< 4,0 mA
++
15 kΩ
4,7 kΩ
2,7 nF
> 4 mA
30 kΩ
1 kΩ
6,8 kΩ
100 µF
220 Ω
100 nF
220 µF
47 nF
10
11
12
13
14
15
16
17
18
TDA2578A
9
8
7
6
5
4
3
2
1
4,7 kΩ
820 Ω
82 Ω
1 kΩ
100 kΩ
4,7 µF
150 nF
22 µF
1 µF
150 pF
10 µF
680 nF
10 µF
56 kΩ
220 kΩ
f<sub>o</sub> adj. (horizontal)
f<sub>o</sub> adj. (vertical)
vertical feedback
vertical drive
video
+26 V (1)
7Z86901

(1) ⩾ 26 V for linear scan.

Fig. 5 Typical application circuit diagram; for application of the TDA2578A with the TDA3651 see Fig. 8.

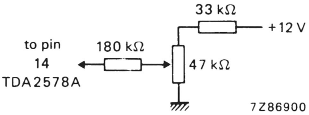

33 kΩ
+12 V
to pin 14 TDA2578A
180 kΩ
47 kΩ
7Z86900

Fig. 6 Circuit configuration at pin 14 for phase adjustment.

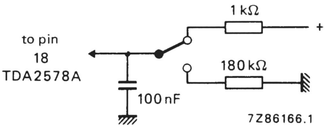

1 kΩ
+12 V
to pin 18 TDA2578A
180 kΩ
100 nF
7Z86166.1

Fig. 7 Circuit configuration at pin 18 for VCR mode.
1 kΩ resistor between pin 18 and + 12 V: without mute function.
180 kΩ between pin 18 and ground: with mute function.

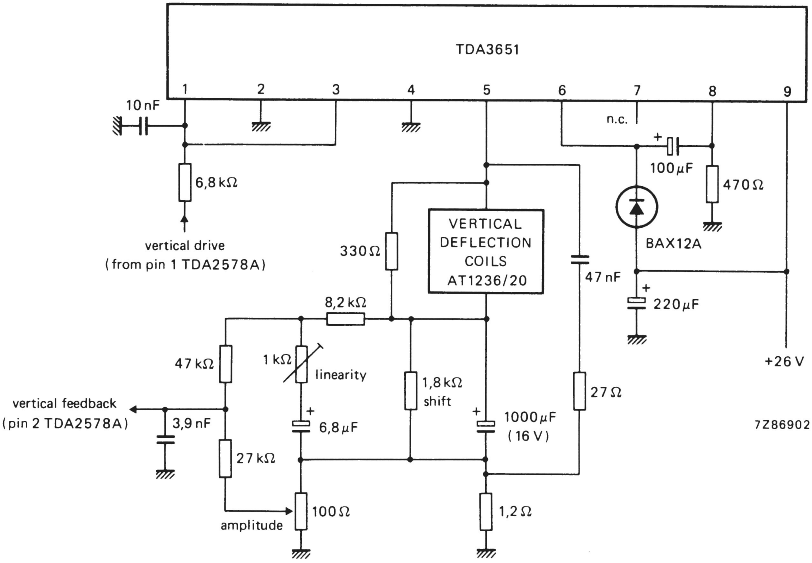

TDA3651
1
2
3
4
5
6
7
8
9
10 nF
6,8 kΩ
vertical drive
(from pin 1 TDA2578A)
n.c.
100 μF
470 Ω
BAX12A
VERTICAL DEFLECTION COILS AT1236/20
330 Ω
47 nF
220 μF
8,2 kΩ
47 kΩ
1 kΩ
linearity
1,8 kΩ
shift
27 Ω
+26 V
vertical feedback
(pin 2 TDA2578A)
3,9 nF
6,8 μF
1000 μF
(16 V)
7Z86902
27 kΩ
100 Ω
amplitude
1,2 Ω

Fig. 8 Typical application circuit diagram of the TDA3651 (vertical output), when used in combination with the TDA2578A, (90° application).

# CONTROL CIRCUIT FOR SMPS

The TDA2581 is a monolithic integrated circuit for controlling switched-mode power supplies (SMPS) which are provided with the drive for the horizontal deflection stage.

The circuit features the following:
- Voltage controlled horizontal oscillator.
- Phase detector.
- Duty factor control for the positive-going transient of the output signal.
- Duty factor increases from zero to its normal operation value.
- Adjustable maximum duty factor.
- Over-voltage and over-current protection with automatic re-start after switch-off.
- Counting circuit for permanent switch-off when n-times over-current or over-voltage is sensed.
- Protection for open-reference voltage.
- Protection for too low supply voltage.
- Protection against loop faults.
- Positive tracking of duty factor and feedback voltage when the feedback voltage is smaller than the reference voltage minus 1,5 V.

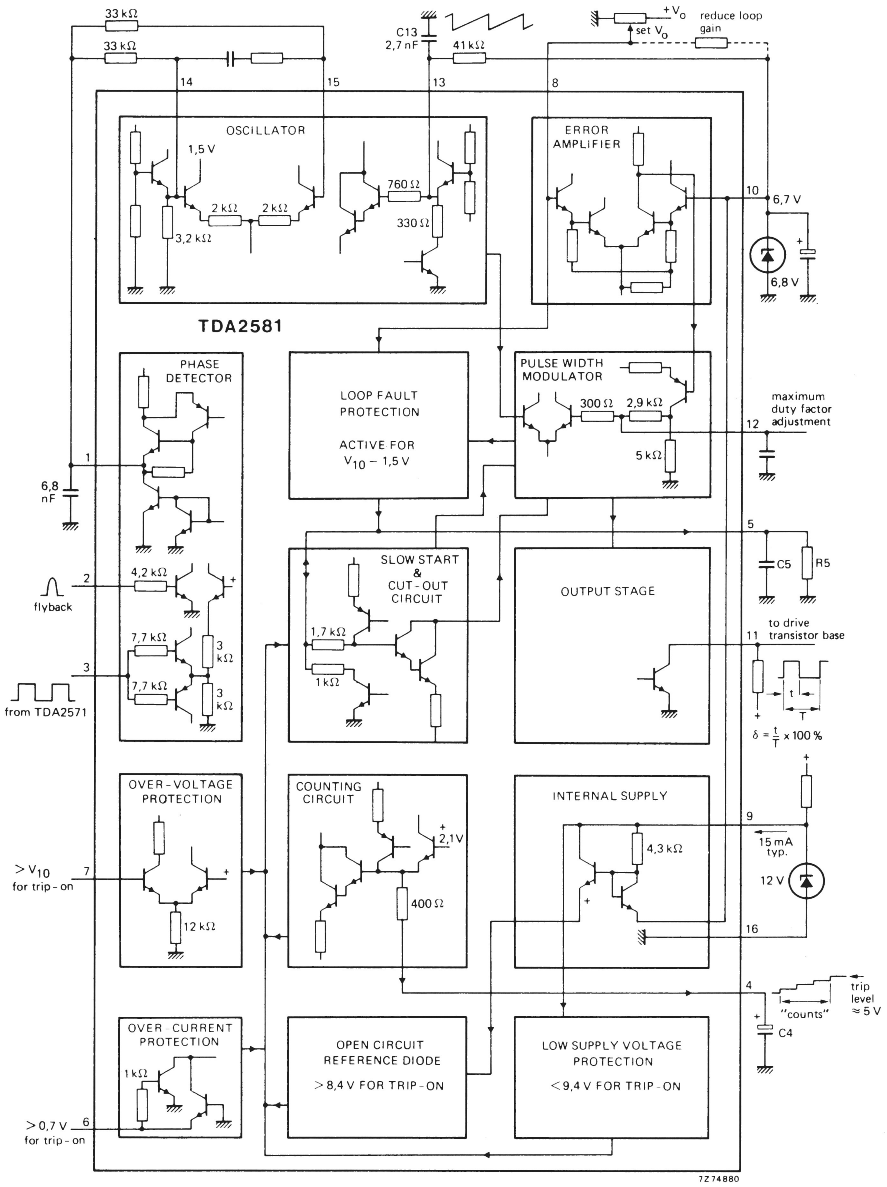
## QUICK REFERENCE DATA

| | | | | |
|---|---|---|---|---|
| Supply voltage | $V_{9\text{-}16}$ | typ. | 12 | V |
| Supply current | $I_9$ | typ. | 15 | mA |
| **Input signals** | | | | |
| Horizontal drive pulse (peak-to-peak value) | $V_{3\text{-}16(p\text{-}p)}$ | typ. | 11 | V |
| Flyback pulse (differentiated deflection current); peak-to-peak value | $V_{2\text{-}16(p\text{-}p)}$ | typ. | 5 | V |
| External reference voltage | $V_{10\text{-}16}$ | typ. | 6,7 | V |
| **Output signals** | | | | |
| Duty factor of output pulse | $\delta$ | > | 0 | % |
| | | < | 98 ± 0,6 | % |
| Output voltage at $I_o < 20$ mA (peak value) | $V_{11\text{-}16M}$ | typ. | 11,8 | V |
| Output current (peak value) | $I_{11M}$ | < | 40 | mA |

## PACKAGE OUTLINES

TDA2581: 16-lead DIL; plastic (SOT-38).
TDA2581Q: 16-lead QIL; plastic (SOT-58).

## BLOCK DIAGRAM


33 kΩ
33 kΩ
14
15
C13
2,7 nF
41 kΩ
13
+V₀
set V₀
reduce loop gain
8
OSCILLATOR
1,5 V
2 kΩ
2 kΩ
3,2 kΩ
760 Ω
330 Ω
ERROR AMPLIFIER
10
6,7 V
6,8 V
TDA2581
PHASE DETECTOR
1
6,8 nF
LOOP FAULT PROTECTION
ACTIVE FOR V₁₀ − 1,5 V
PULSE WIDTH MODULATOR
300 Ω
2,9 kΩ
5 kΩ
12
maximum duty factor adjustment
5
C5
R5
2
flyback
4,2 kΩ
3
from TDA2571
7,7 kΩ
7,7 kΩ
3 kΩ
3 kΩ
SLOW START & CUT-OUT CIRCUIT
1,7 kΩ
1 kΩ
OUTPUT STAGE
11
to drive transistor base
t
T
δ = t/T x 100 %
OVER-VOLTAGE PROTECTION
7
> V₁₀ for trip-on
12 kΩ
COUNTING CIRCUIT
2,1 V
400 Ω
INTERNAL SUPPLY
9
4,3 kΩ
15 mA typ.
12 V
16
4
"counts"
trip level ≈ 5 V
C4
OVER-CURRENT PROTECTION
1 kΩ
6
> 0,7 V for trip-on
OPEN CIRCUIT REFERENCE DIODE
> 8,4 V FOR TRIP-ON
LOW SUPPLY VOLTAGE PROTECTION
< 9,4 V FOR TRIP-ON
7Z74880

Note: trip levels are nominal values.

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | | |
|---|---|---|---|---|
| Supply voltage | $V_{9-16}$ | max. | 14 | V |
| Voltage at pin 11 | $V_{11-16}$ | | 0 to 14 | V |
| Output current | $I_{11}$ | max. | 40 | mA |
| Total power dissipation | $P_{tot}$ | max. | 340 | mW |
| Storage temperature | $T_{stg}$ | | −25 to +125 | °C |
| Operating ambient temperature | $T_{amb}$ | | −25 to +80 | °C |

## CHARACTERISTICS

$V_{9-16}$ = 12 V; $V_{10-16}$ = 6,7 V; $T_{amb}$ = 25 °C; measured in the circuit on page 2

| | | | | |
|---|---|---|---|---|
| Supply voltage range | $V_{9-16}$ | typ. | 12 | V |
| | | | 10 to 14 | V |
| Protection voltage too low supply voltage | $V_{9-16}$ | typ. | 9,4 | V |
| | | | 8,6 to 9,9 | V |
| Supply current at $\delta$ = 50% | $I_9$ | typ. | 15 | mA |
| Supply current during protection | $I_9$ | typ. | 15 | mA |
| Minimum required supply current | $I_9$ | < | 18,5 | mA* |
| Power consumption | P | typ. | 180 | mW |

**Required input signals**

| | | | | |
|---|---|---|---|---|
| Reference voltage | $V_{10-16}$ | typ. | 6,7 | V |
| | | | 5,6 to 7,5 | V** |
| High reference voltage protection: threshold voltage | $V_{10-16}$ | typ. | 8,4 | V |
| | | | 7,9 to 8,9 | V |
| Feedback input impedance at pin 8 | $\|Z_{8-16}\|$ | typ. | 200 | kΩ |
| Horizontal drive pulse (square-wave or differentiated; negative transient is reference) peak-to-peak value | $V_{3-16(p-p)}$ | typ. | 11 | V |
| | | | 5 to 12 | V |
| Flyback pulse or differential deflection current | $V_{2-16}$ | | 1 to 5 | V |
| Over-current protection: threshold voltage | $-V_{6-16}$ | typ. | 640 | mV |
| | | | 690 to 695 | mV▲ |
| | $+V_{6-16}$ | typ. | 680 | mV |
| | | | 640 to 735 | mV▲ |
| Over-voltage protection: threshold voltage | $V_{7-16}$ | typ. | $V_{10-16}$ −60 | mV |
| | | $V_{10-16}$ | −130 to $V_{10-16}$ −0 | mV |

---

* This value refers to the minimum required supply current that will start all devices under the following conditions: $V_{9-16}$ = 10 V; $V_{10-16}$ = 6,8 V; $\delta$ = 50%.

** Voltage obtained via an external reference diode. Specified voltages do not refer to the nominal voltages of reference diodes.

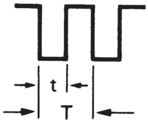
▲ This spread is inclusive temperature rise of the IC due to warming up. For other ambient temperatures the values must be corrected by using a temperature coefficient of typical −1,85 mV/°C.

## CHARACTERISTICS (continued)

| | | | | |
|---|---|---|---|---|
| Remote control voltage; switch off | $V_{4\text{-}16}$ | > | 5,8 | V* |
| switch on | $V_{4\text{-}16}$ | < | 4,5 | V* |
| **Delivered output signals** | | | | |
| Horizontal drive pulse (loaded with a resistor of 560 Ω to +12 V) peak-to-peak value | $V_{11\text{-}16(p\text{-}p)}$ | > | 11,6 | V |
| Output current; peak value | $I_{11M}$ | < | 40 | mA |
| Saturation voltage of output transistor at $I_{11}$ = 20 mA | $V_{CEsat}$ | typ. | 200 | mV |
| | | < | 400 | mV |
| at $I_{11}$ = 40 mA | $V_{CEsat}$ | < | 525 | mV |
| Duty factor of output pulse** | δ | > | 0 | % |
| | | < | 98 ± 0,6 | % |
| Charge current for capacitor on pin 4 | $I_4$ | typ. | 120 | μA |
| Charge current for capacitor on pin 5 | $I_5$ | typ. | 130 | μA |
| Supply current for reference | $I_{10}$ | typ. | 1 | mA |
| | | | 0,6 to 1,45 | mA |
| **Oscillator** | | | | |
| Temperature coefficient | | typ. | −300 | ppm/°C |
| | | < | −400 | ppm/°C |
| Relative frequency deviation for $V_{10\text{-}16}$ changing from 6 to 7 V | | typ. | −1,5 | % |
| | | ⩽ | −2 | % |
| Oscillator frequency spread (with fixed external components) | | ⩽ | ±3 | % |
| Frequency control sensitivity at pin 15 | | typ. | 4,5 | kHz/V▲ |
| **Phase control loop** | | | | |
| Loop gain of APC-system (automatic phase control) | | typ. | 5 | kHz/μs |
| Catching range | Δf | typ. | ±1,5 | kHz |
| Phase relation between negative transient of sync pulse and middle of flyback | t | typ. | 1 | μs |
| Tolerance of phase relation | Δt | ⩽ | ±0,4 | μs |

* See pin 4 on pages 7 and 8.

** The duty factor is specified as follows:



$$\delta = \frac{t}{T} \times 100\%.$$

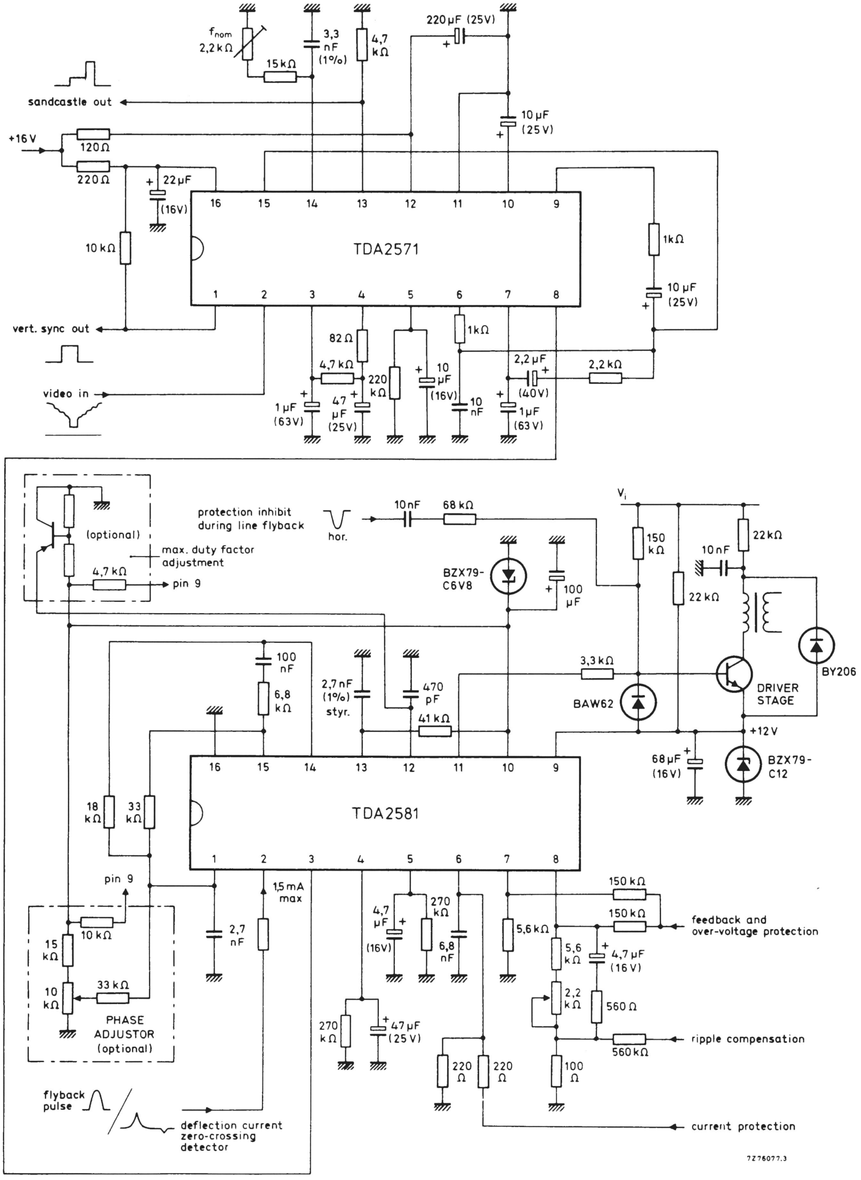
The maximum duty factor value can be set to a desired value (see application information pin 12 on page 9).

▲ For component values see circuit diagram on page 2.

## PINNING

1. Phase detector output
2. Flyback pulse position input
3. Reference frequency input
4. Re-start count capacitor/remote control input
5. Slow start and transfer characteristic for low feedback voltages
6. Over-current protection input
7. Over-voltage protection input
8. Feedback voltage input
9. Positive supply
10. Reference input
11. Output
12. Maximum duty factor adjustment/smoothing
13. Oscillator timing network
14. Reactance stage reference voltage
15. Reactance stage input
16. Negative supply (ground)

## APPLICATION INFORMATION


f_nom 2,2 kΩ
15 kΩ
3,3 nF (1%)
4,7 kΩ
220 μF (25V)
10 μF (25 V)
sandcastle out
+16 V
120 Ω
220 Ω
22 μF (16V)
10 kΩ
TDA2571
16
15
14
13
12
11
10
9
1
2
3
4
5
6
7
8
1 kΩ
10 μF (25V)
vert. sync out
video in
82 Ω
4,7 kΩ
220 kΩ
10 μF (16V)
1 kΩ
2,2 μF (40V)
2,2 kΩ
1 μF (63V)
47 μF (25V)
10 nF
1 μF (63 V)
(optional)
max. duty factor adjustment
4,7 kΩ
pin 9
protection inhibit during line flyback
hor.
10 nF
68 kΩ
V_i
BZX79-C6V8
100 μF
150 kΩ
10 nF
22 kΩ
22 kΩ
BY206
100 nF
6,8 kΩ
2,7 nF (1%) styr.
470 pF
41 kΩ
3,3 kΩ
BAW62
DRIVER STAGE
+12 V
68 μF (16V)
BZX79-C12
TDA2581
18 kΩ
33 kΩ
pin 9
1,5 mA max
2,7 nF
10 kΩ
15 kΩ
10 kΩ
33 kΩ
PHASE ADJUSTOR (optional)
4,7 μF (16V)
270 kΩ
6,8 nF
5,6 kΩ
150 kΩ
150 kΩ
feedback and over-voltage protection
5,6 kΩ
4,7 μF (16 V)
2,2 kΩ
560 Ω
560 kΩ
ripple compensation
270 kΩ
47 μF (25 V)
220 Ω
220 Ω
100 Ω
current protection
flyback pulse
deflection current zero-crossing detector
7Z76077.3

The TDA2571 and TDA2581 controlling an SMPS driver stage.

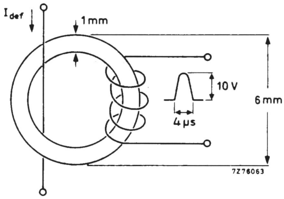
**The function is quoted against the corresponding pin number**

1. Phase detector output

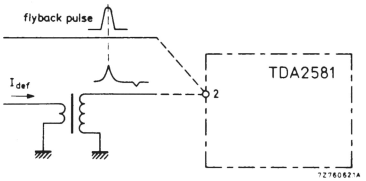
   The output circuit consists of a bidirectional current source which is active for the time that the signal on pin 2 exceeds 1 V.
   The current values are chosen such that the correct phase relation is obtained when the reference signal on pin 3 is delivered by the TDA2571.
   With a resistor of 18 kΩ and a capacitor of 2,7 nF the control steepness is 0,55 V/µs.

2. Flyback pulse input

   The signal applied to pin 2 is normally a flyback pulse with a duration of about 12 µs. However, the phase detector system also accepts a signal derived by differentiating the deflection current by means of a small toroidal core (pulse duration > 3 µs).



(a)



(b)

The toroidal transformer in (a) is for obtaining a pulse representing the mid-flyback from the deflection current. The connection of the picture phase information is shown in (b).

3. Reference frequency input

   The input circuit can be driven directly by the square-wave output voltage from pin 8 of the TDA2571.
   The negative-going transient switches the current source connected to pin 1 from positive to negative. The input circuit is made such that a differentiated signal of the square-wave from the TDA2571 is also accepted (this enables mains isolation). The input circuit switching level is about 3 V and the input impedance is about 10 kΩ.

4. Re-start count capacitor/remote control input

   *Counting*

   An external capacitor (C4 = 47 µF) is connected between pins 4 and 16. This capacitor controls the characteristics of the protection circuits as follows.
   If the protection circuits are required to operate, e.g. over-current at pin 6, the duty factor will be set to zero thus turning off the power supply.
   After a short interval (determined by the time constant on pin 5) the power supply will be restarted via the slow start circuit.
   If the fault condition has cleared, then normal operation will be resumed. If the fault condition is persistent, the duty factor of the pulses is again reduced to zero and the protection cycle is repeated.

   The number of times this action is repeated (n) for a persisting fault condition is now determined by: n = C4/C5.

## APPLICATION INFORMATION (continued)

*Remote control input*

For this application the capacitor on pin 4 has to be replaced by a resistor with a value between 4,7 and 18 kΩ. When the externally applied voltage $V_{4\text{-}16} > 5{,}8$ V, the circuit switches off; switching on occurs when $V_{4\text{-}16} < 4{,}5$ V and the normal starting-up procedure is followed. Pin 4 is internally connected to an emitter-follower, with an emitter voltage of 1,5 V.

5. Slow start and transfer characteristics for low feedback voltages

*Slow start*

An external shunt capacitor (C5 = 4,7 μF) and resistor (R5 = 270 kΩ) are connected between pins 5 and 16. The network controls the rate at which the duty factor increases from zero to its steady-state value after switch-on. It provides protection against surges in the power transistor.

*Transfer characteristic for low feedback voltages*

The duty factor transfer characteristic for low feedback voltages can be influenced by R5. The transfer for three different resistor values is given in the graph on page 10.

6. Over-current protection input

A voltage proportional to the current in the power switching device is applied to the integrated circuit between pins 6 and 16. The circuit trips on both positive and negative polarity.

7. Over-voltage protection input

When the voltage applied to this pin exceeds the threshold level, the protection circuit will operate. When this function is not used, pin 7 should be connected to pin 16.

8. Feedback voltage input

The control loop input is applied to pin 8. This pin is internally connected to one input of a differential amplifier, functioning as an amplitude comparator, the other input of which is connected to the reference source on pin 10.
Under normal operating conditions, the voltage on pin 8 will be about equal to the reference voltage on pin 10. For further information refer to the graphs on pages 10 and 11.

9. 12 V positive supply

The maximum voltage that may be applied is 14 V. Where this is derived from an unstabilized supply rail, a regulator diode (12 V) should be connected between pins 9 and 16 to ensure that the maximum voltage does not exceed 14 V. When the voltage on this pin falls below a minimum of 8,6 V (typically 9,4 V), the protection circuit will switch-off the power supply.

10. Reference input

An external reference diode must be connected between this pin and pin 16.
The reference voltage must be between 5,6 and 7,5 V. The IC delivers about 1 mA into the external regulator diode. When the external load on the regulator diode approaches this current, replenishment of the current can be obtained by connecting a suitable resistor between pins 9 and 10.

11. Output

An external resistor determines the output current fed into the base of the driver transistor. The output circuit uses an n-p-n transistor with 3 series-connected clamping diodes to the internal 12 V supply rail. This provides a low impedance in the "ON" state, that is with the drive transistor turned-off.

12. Maximum duty factor adjustment/smoothing

*Maximum duty factor adjustment*

Pin 12 is connected to the output voltage of the amplitude comparator ($V_{10\text{-}8}$). This voltage is internally connected to one input of a differential amplifier, the other input of which is connected to the sawtooth voltage of the horizontal oscillator. A low voltage on pin 12 results in a low duty factor. This enables the maximum duty factor to be adjusted by limiting the voltage by connecting pin 12 to the emitter of a p-n-p transistor used as a voltage source.
The graph on page 10 plots the maximum duty factor as a function of the voltage applied to pin 12. If some spread is acceptable the maximum duty factor can also be limited by connecting a resistor from pin 12 to pin 16. A resistor of 12 kΩ limits the maximum duty factor to about 50%.
This application also reduces the total IC gain.

*Smoothing*

Any double pulsing of the IC due to circuit layout can be suppressed by connecting a capacitor of about 470 pF between pins 12 and 16.

13. Oscillator timing network

The timing network comprises a capacitor between pins 13 and 16, and a resistor between pin 13 and the reference voltage on pin 10.
The charging current for the capacitor (C13) is derived from the voltage reference diode connected to pin 10 and discharged via an internal resistor of about 330 Ω.

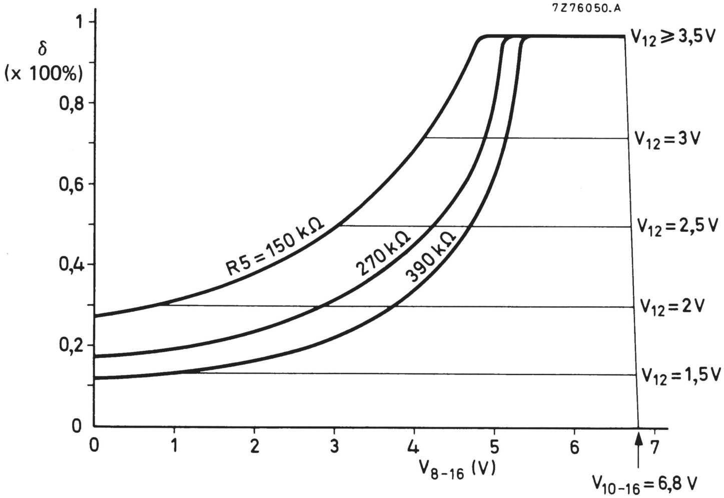
14. Reactance stage reference voltage

This pin is connected to an emitter follower which determines the nominal reference voltage for the reactance stage (1,5 V for reference voltage $V_{10\text{-}16} = 6{,}7$ V). Free-running frequency is obtained when pins 14 and 15 are short-circuited.

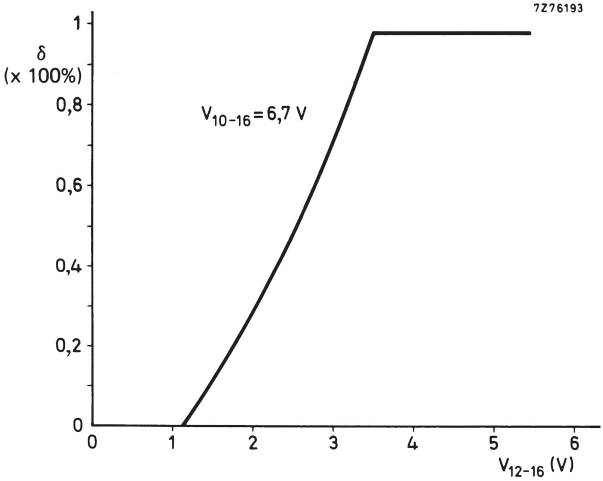
15. Reactance stage input

The output voltage of the phase detector (pin 1) is connected to pin 15 via a resistor. The voltage applied to pin 15 shifts the upper level of the voltage sensor of the oscillator thus changing the oscillator frequency and phase. The time constant network is connected between 14 and 15. Control sensitivity is typically 4,5 kHz/V.

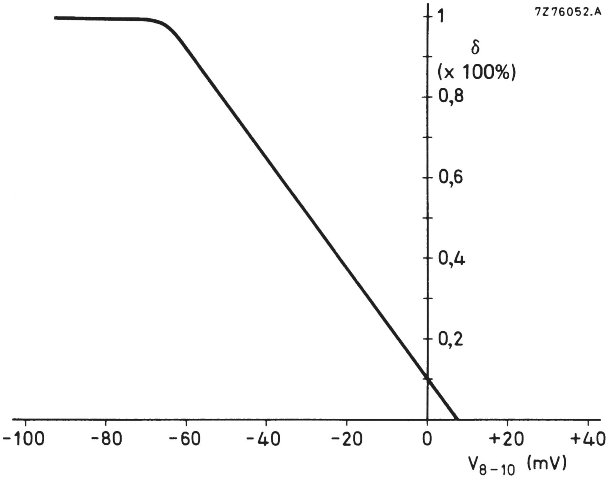
16. Negative supply (ground)



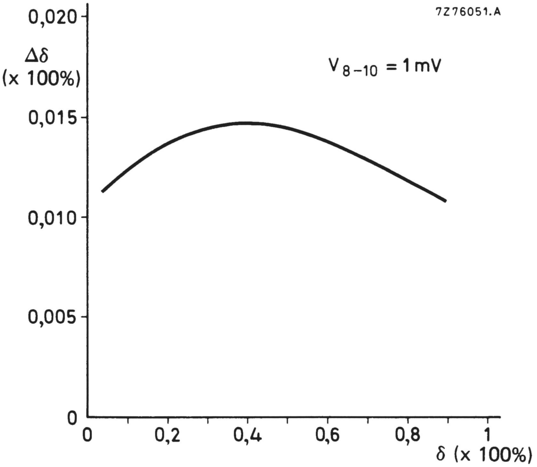
Duty factor of output pulses as a function of $V_{8\text{-}16}$ with R5 as a parameter, and with $V_{12}$ as a limiting value; $V_{10\text{-}16}$ = 6,8 V.



Maximum duty factor limitation as a function of $V_{12\text{-}16}$.



Duty factor of output pulses as a function of error amplifier input ($V_{8-10}$).



Change in duty factor of output pulses for a 1 mV error amplifier input change ($V_{8-10}$) as a function of initial duty factor.

# CONTROL CIRCUIT FOR POWER SUPPLIES

The TDA2582 is a monolithic integrated circuit for controlling power supplies which are provided with the drive for the horizontal deflection stage.
The circuit features the following:

- Voltage controlled horizontal oscillator.
- Phase detector.
- Duty factor control for the negative-going transient of the output signal.
- Duty factor increases from zero to its normal operation value.
- Adjustable maximum duty factor.
- Over-voltage and over-current protection with automatic re-start after switch-off.
- Counting circuit for permanent switch-off when n-times over-current or over-voltage is sensed.
- Protection for open-reference voltage.
- Protection for too low supply voltage.
- Protection against loop faults.
- Positive tracking of duty factor and feedback voltage when the feedback voltage is smaller than the reference voltage minus 1,5 V.
- Normal and 'smooth' remote ON/OFF possibility.

## QUICK REFERENCE DATA

| | | | | |
|---|---|---|---|---|
| Supply voltage | $V_{9\text{-}16}$ | typ. | 12 | V |
| Supply current | $I_9$ | typ. | 14 | mA |
| **Input signals** | | | | |
| Horizontal drive pulse (peak-to-peak value) | $V_{3\text{-}16(p\text{-}p)}$ | | 5 to 11 | V |
| Flyback pulse (differentiated deflection current); peak-to-peak value | $V_{2\text{-}16(p\text{-}p)}$ | | 1 to 5 | V |
| External reference voltage | $V_{10\text{-}16}$ | typ. | 6,1 | V |
| **Output signals** | | | | |
| Duty factor of output pulse | $\delta$ | ><br><| 0<br>98 ± 0,8 | %<br>% |
| Output voltage at $I_o < 20$ mA (peak value) | $V_{11\text{-}16M}$ | typ. | 11,8 | V |
| Output current (peak value) | $I_{11M}$ | < | 40 | mA |

## PACKAGE OUTLINES

TDA2582 : 16-lead DIL; plastic (SOT-38).
TDA2582Q: 16-lead QIL; plastic (SOT-58).

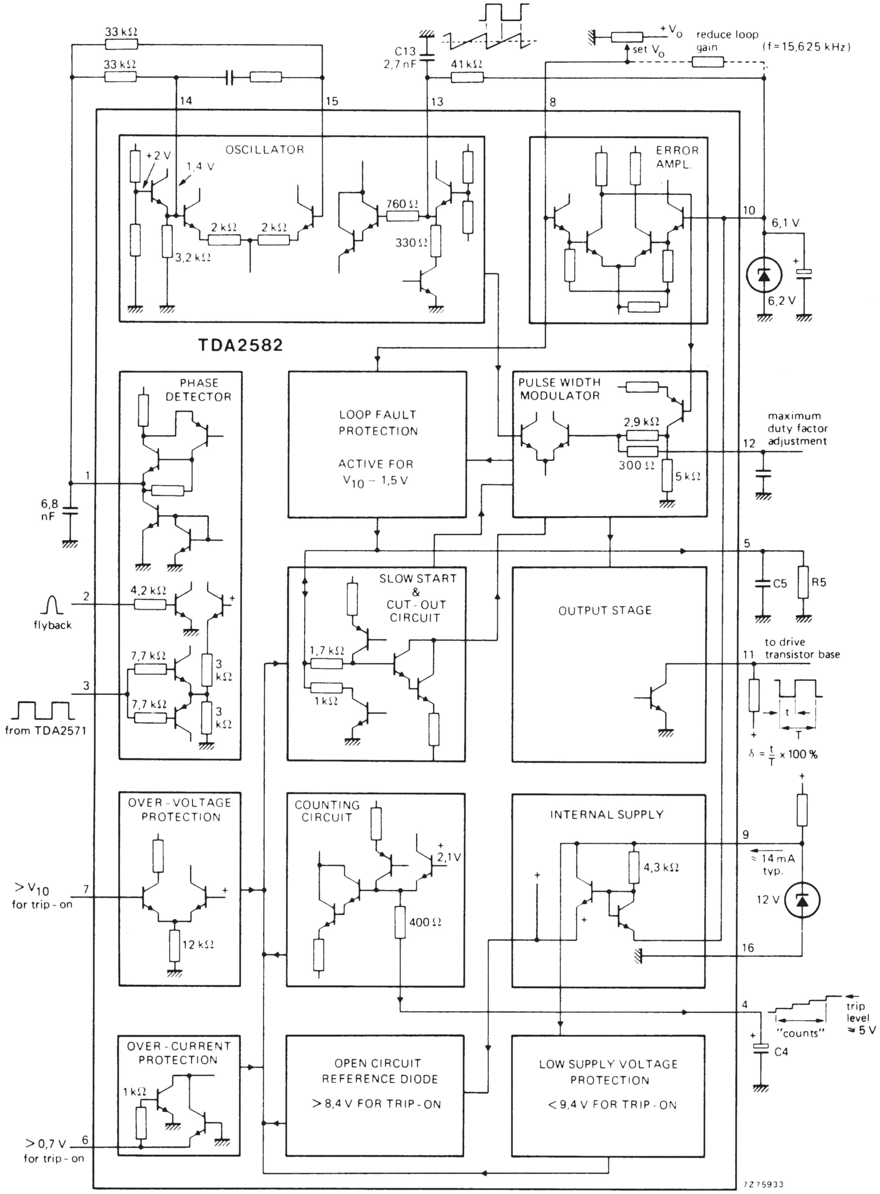

33 kΩ
33 kΩ
C13
2,7 nF
41 kΩ
+V$_O$
set V$_O$
reduce loop gain
(f = 15,625 kHz)
14
15
13
8
OSCILLATOR
+2 V
1,4 V
3,2 kΩ
2 kΩ
2 kΩ
760 Ω
330 Ω
ERROR AMPL.
10
6,1 V
6,2 V
TDA2582
PHASE DETECTOR
LOOP FAULT PROTECTION
ACTIVE FOR V$_{10}$ − 1,5 V
PULSE WIDTH MODULATOR
2,9 kΩ
300 Ω
5 kΩ
maximum duty factor adjustment
12
1
6,8 nF
5
C5
R5
2
4,2 kΩ
flyback
SLOW START & CUT-OUT CIRCUIT
1,7 kΩ
1 kΩ
OUTPUT STAGE
to drive transistor base
11
7,7 kΩ
7,7 kΩ
3 kΩ
3 kΩ
3
from TDA2571
t
T
δ = $\frac{t}{T}$ × 100 %
OVER-VOLTAGE PROTECTION
12 kΩ
7
> V$_{10}$ for trip-on
COUNTING CIRCUIT
2,1 V
400 Ω
INTERNAL SUPPLY
4,3 kΩ
9
≈ 14 mA typ.
12 V
16
4
"counts"
trip level ≈ 5 V
C4
OVER-CURRENT PROTECTION
1 kΩ
> 0,7 V for trip-on
6
OPEN CIRCUIT REFERENCE DIODE
> 8,4 V FOR TRIP-ON
LOW SUPPLY VOLTAGE PROTECTION
< 9,4 V FOR TRIP-ON
7Z75933

Fig. 1 Block diagram.

Note: trip levels are nominal values.

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | | |
|---|---|---|---|---|
| Supply voltage at pin 9 | $V_{9-16}$ | max. | 14 | V |
| Voltage at pin 11 | $V_{11-16}$ | | 0 to 14 | V |
| Output current (peak value) | $I_{11M}$ | max. | 40 | mA |
| Total power dissipation | $P_{tot}$ | max. | 280 | mW |
| Storage temperature | $T_{stg}$ | | −25 to + 125 | °C |
| Operating ambient temperature | $T_{amb}$ | | −25 to + 80 | °C |

## CHARACTERISTICS

$V_{9-16}$ = 12 V; $V_{10-16}$ = 6,1 V; $T_{amb}$ = 25 °C; measured in Fig. 4

| | | | | |
|---|---|---|---|---|
| Supply voltage range | $V_{9-16}$ | typ. | 12 | V |
| | | | 10 to 14 | V |
| Protection voltage too low supply voltage | $V_{9-16}$ | typ. | 9,4 | V |
| | | | 8,6 to 9,9 | V |
| Supply current at $\delta$ = 50% | $I_9$ | typ. | 14 | mA |
| Supply current during protection | $I_9$ | typ. | 14 | mA |
| Minimum required supply current (note 1) | $I_9$ | $<$ | 17 | mA |
| Power consumption | P | typ. | 170 | mW |
| **Required input signals** | | | | |
| Reference voltage (note 2) | $V_{10-16}$ | typ. | 6,1 | V |
| | | | 5,6 to 6,6 | V |
| Feedback input impedance | $\lvert Z_{8-16} \rvert$ | typ. | 200 | kΩ |
| High reference voltage protection: threshold voltage | $V_{10-16}$ | typ. | 8,4 | V |
| | | | 7,9 to 8,9 | V |
| Horizontal reference signal (square-wave or differentiated; negative transient is reference) | | | | |
| Voltage driven (peak-to-peak value) | $V_{3-16(p-p)}$ | | 5 to 12 | V |
| Current driven (peak value) | $I_{3M}$ | | −1 to + 1,5 | mA |
| Switching level current | $\pm I_3$ | $<$ | 100 | μA |
| Flyback pulse or differential deflection current | $V_{2-16}$ | | 1 to 5 | V |
| Flyback pulse current (peak value) | $I_{2M}$ | $<$ | 1,5 | mA |
| Over-current protection: (note 3) threshold voltage | $-V_{6-16}$ | typ. | 640 | mV |
| | | | 600 to 695 | mV |
| | $+V_{6-16}$ | typ. | 680 | mV |
| | | | 640 to 735 | mV |

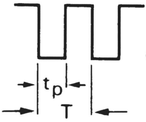
Notes

1. This value refers to the minimum required supply current that will start all devices under the following conditions: $V_{9-16}$ = 10 V; $V_{10-16}$ = 6,2 V; $\delta$ = 50%.
2. Voltage obtained via an external reference diode. Specified voltages do not refer to the nominal voltages of reference diodes.
3. This spread is inclusive temperature rise of the IC due to warming up. For other ambient temperatures the values must be corrected by using a temperature coefficient of typical −1,85 mV/°C.

**CHARACTERISTICS** (continued)

| | | | | |
|---|---|---|---|---|
| Over-voltage protection: ($V_{ref} = V_{10\text{-}16}$) threshold voltage | $V_{7\text{-}16}$ | typ. | $V_{ref}-60$ | mV |
| | | | $V_{ref}-130$ to $V_{ref}-0$ | mV |
| Remote control voltage; switch-off (note 1) | $V_{4\text{-}16}$ | > | 5,6 | V |
| Remote control voltage; switch-on | $V_{4\text{-}16}$ | < | 4,5 | V |
| 'Smooth' remote control; switch-off (note 2) | $V_{5\text{-}16}$ | > | 4,5 | V |
| 'Smooth' remote control; switch-on | $V_{5\text{-}16}$ | < | 3 | V |
| Remote control switch-off current | $I_4$ | < | 1 | mA |
| **Delivered output signals** | | | | |
| Horizontal drive pulse (loaded with a resistor of 560 Ω to + 12 V peak-to-peak value | $V_{11\text{-}16(p\text{-}p)}$ | > | 11,6 | V |
| Output current; peak value | $I_{11M}$ | < | 40 | mA |
| Saturation voltage of output transistor at $I_{11} = 20$ mA | $V_{CEsat}$ | typ. | 200 | mV |
| | | < | 400 | mV |
| at $I_{11} = 40$ mA | $V_{CEsat}$ | < | 525 | mV |
| Duty factor of output pulse (note 3) | $\delta$ | > | 0 | % |
| | | < | 98 ± 0,8 | % |
| Charge current for capacitor on pin 4 | $I_4$ | typ. | 110 | μA |
| Charge current for capacitor on pin 5 | $I_5$ | typ. | 120 | μA |
| Supply current for reference | $I_{10}$ | typ. | 1 | mA |
| | | | 0,6 to 1,45 | mA |
| **Oscillator** | | | | |
| Temperature coefficient | | typ. | 0,0003 | $^{o}C^{-1}$ |
| | | < | 0,0004 | $^{o}C^{-1}$ |
| Relative frequency deviation for $V_{10\text{-}16}$ changing from 5,6 to 6,6 V | | typ. | −1,4 | % |
| | | < | −2 | % |
| Oscillator frequency spread (with fixed external components) | | < | 3 | % |
| Frequency control sensitivity at pin 15 $f_{nom} = 15{,}625$ kHz | | typ. | 5 | kHz/V |

Notes
1. See function description pin 4 (pages 9 and 10).
2. See function description pin 5 (page 10).
3. The duty factor is specified as follows: $\delta = \frac{t_p}{T} \times 100\%$ (see Fig. 2). After switch-on the duty factor rises gradually from 0% to the steady value. The relationship between $V_{8\text{-}16}$ and the duty factor is given in Fig. 7 and the relationship between $V_{12\text{-}16}$ and the duty factor is shown in Fig. 9.



$$\delta = \frac{t_p}{T} \times 100\%.$$

Fig. 2.

**Phase control loop**

| | | | | |
|---|---|---|---|---|
| Loop gain of APC-system (automatic phase control) * | | typ. | 5 | kHz/μs |
| Catching range ($f_{nom}$ = 15,625 kHz) | Δf | ><br><<br> | 1300<br>2100 | Hz<br>Hz |
| Phase relation between negative transient of sync pulse and middle of flyback | t | typ. | 1 | μs |
| Tolerance of phase relation | Δt | ⩽ | ± 0,4 | μs |

## PINNING

1. Phase detector output
2. Flyback pulse position input
3. Reference frequency input
4. Re-start count capacitor/remote control input
5. Slow start and transfer characteristic for low feedback voltages
6. Over-current protection input
7. Over-voltage protection input
8. Feedback voltage input
9. Positive supply
10. Reference input
11. Output
12. Maximum duty factor adjustment/smoothing
13. Oscillator timing network
14. Reactance stage reference voltage
15. Reactance stage input
16. Negative supply (ground)

---

* For component values see Fig. 1.

## APPLICATION INFORMATION

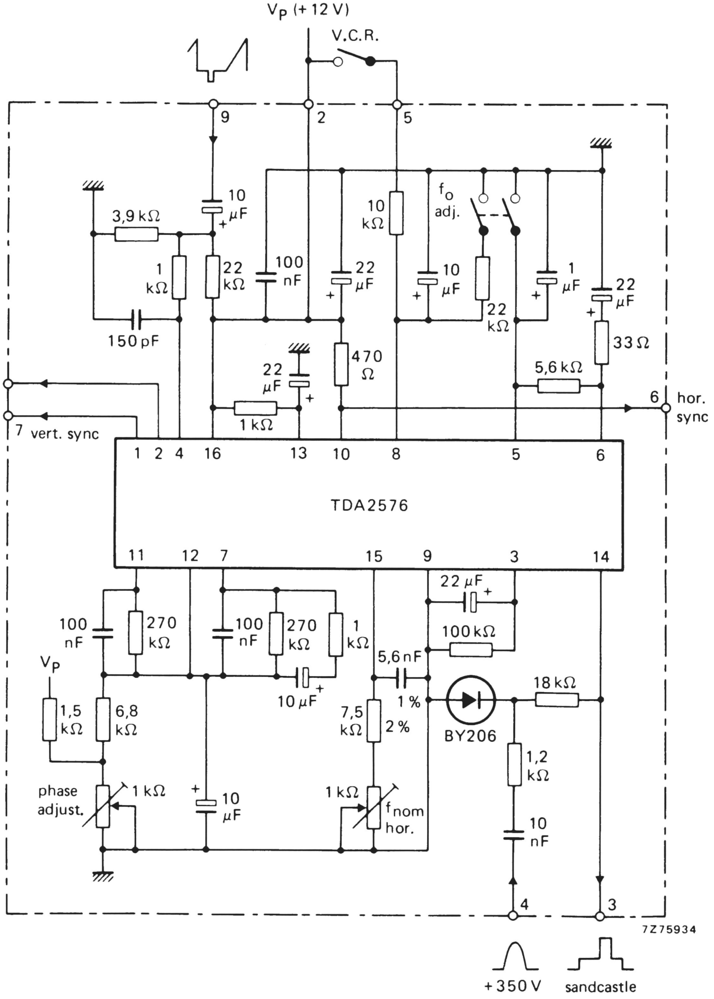

VP (+12 V)
V.C.R.
9
2
5
10 µF
3,9 kΩ
1 kΩ
22 kΩ
100 nF
22 µF
10 kΩ
fo adj.
10 µF
22 kΩ
1 µF
22 µF
33 Ω
150 pF
22 µF
470 Ω
5,6 kΩ
1 kΩ
6 hor. sync
7 vert. sync
TDA2576
1
2
4
16
13
10
8
5
6
11
12
7
15
9
3
14
22 µF
100 kΩ
100 nF
270 kΩ
100 nF
270 kΩ
1 kΩ
5,6 nF 1%
10 µF
VP
1,5 kΩ
6,8 kΩ
7,5 kΩ 2%
BY206
18 kΩ
1,2 kΩ
phase adjust.
1 kΩ
10 µF
1 kΩ
fnom hor.
10 nF
4
3
+350 V
sandcastle
7Z75934

Fig. 3a.

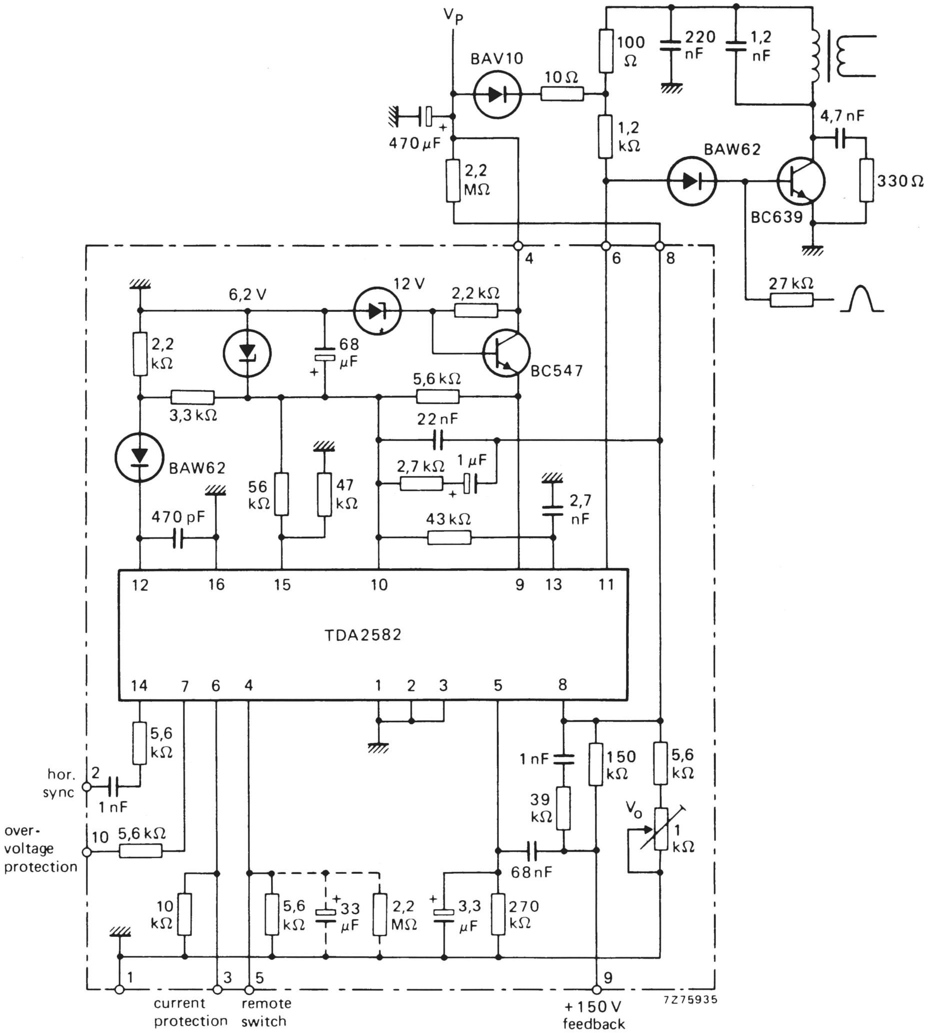
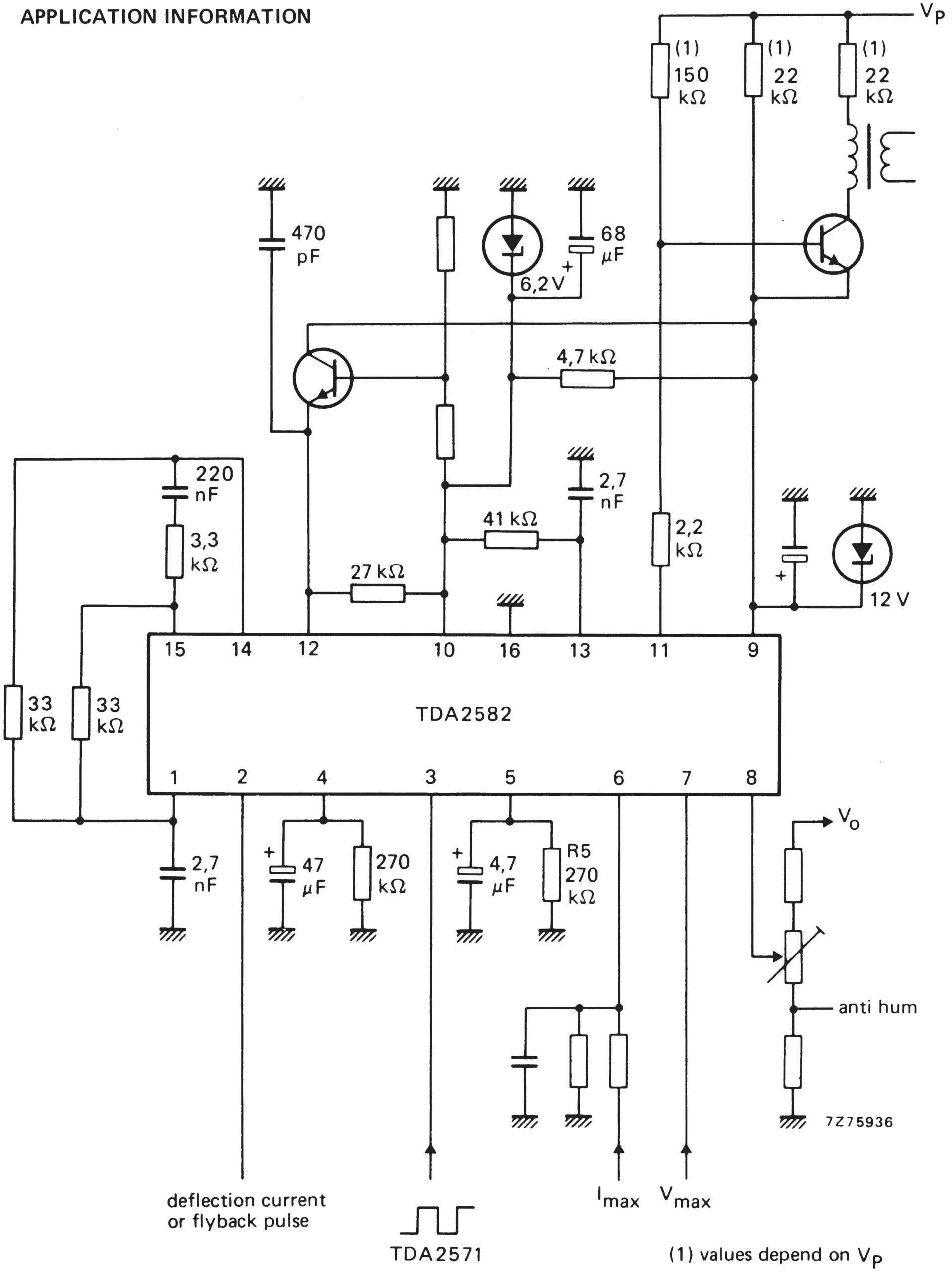

V_P
BAV10
10 Ω
470 µF
2,2 MΩ
100 Ω
220 nF
1,2 nF
1,2 kΩ
BAW62
4,7 nF
BC639
330 Ω
27 kΩ
4
6
8
6,2 V
12 V
2,2 kΩ
2,2 kΩ
68 µF
BC547
3,3 kΩ
5,6 kΩ
22 nF
BAW62
2,7 kΩ
1 µF
56 kΩ
47 kΩ
470 pF
2,7 nF
43 kΩ
12
16
15
10
9
13
11
TDA2582
14
7
6
4
1
2
3
5
8
5,6 kΩ
hor. sync
2
1 nF
over-voltage protection
10
5,6 kΩ
1 nF
150 kΩ
5,6 kΩ
39 kΩ
V_o
1 kΩ
68 nF
10 kΩ
5,6 kΩ
33 µF
2,2 MΩ
3,3 µF
270 kΩ
1
3
5
9
current protection
remote switch
+150 V feedback
7Z75935

Fig. 3b.

Lead 6 (pin 10) of circuit TDA2576 connected to lead 2 (pin 14) of circuit TDA2582.

## APPLICATION INFORMATION


V_P
(1)
150
kΩ
(1)
22
kΩ
(1)
22
kΩ
470
pF
6,2 V
68
μF
+
4,7 kΩ
220
nF
3,3
kΩ
2,7
nF
41 kΩ
27 kΩ
2,2
kΩ
+
12 V
15
14
12
10
16
13
11
9
TDA2582
33
kΩ
33
kΩ
1
2
4
3
5
6
7
8
2,7
nF
+
47
μF
270
kΩ
+
4,7
μF
R5
270
kΩ
V_o
anti hum
7Z75936
deflection current
or flyback pulse
TDA2571
I_max
V_max

(1) values depend on $V_P$

Fig. 4 Circuit diagram.

**The function is described against the corresponding pin number**

### 1. Phase detector output

The output circuit consists of a bidirectional current source which is active for the time that the signal on pin 2 exceeds 1 V.
The current values are chosen such that the correct phase relation is obtained when the output signal of the TDA2571 is applied to pin 3.
With a resistor of 2 x 33 kΩ and a capacitor of 2,7 nF the control steepness is 0,55 V/µs (Fig. 4).

### 2. Flyback pulse input

The signal applied to pin 2 is normally a flyback pulse with a duration of about 12 µs. However, the phase detector system also accepts a signal derived by differentiating the deflection current by means of a small toroidal core (pulse duration > 3 µs).

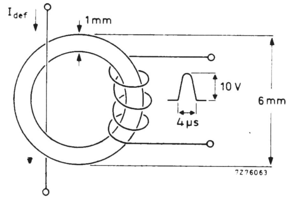


Fig. 5a.

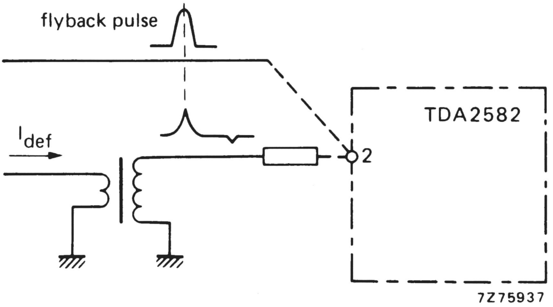


Fig. 5b.

The toroidal transformer in Fig. 5a is for obtaining a pulse representing the mid-flyback from the deflection current. The connection of the picture phase information is shown in Fig. 5b.

### 3. Reference frequency input

The input circuit can be driven directly by the square-wave output voltage from pin 8 of the TDA2571.
The negative-going transient switches the current source connected to pin 1 from positive to negative.
The input circuit is made such that a differentiated signal of the square-wave from the TDA2571 is also accepted (this enables mains isolation). The input circuit switching level is about 3 V and the input impedance is about 8 kΩ.

### 4. Re-start count capacitor/remote control input

*Counting*

An external capacitor (C4 = 47 µF) is connected between pins 4 and 16. This capacitor controls the characteristics of the protection circuits as follows.
If the protection circuits are required to operate, e.g. over-current at pin 6, the duty factor will be set to zero thus turning off the power supply.
After a short interval (determined by the time constant on pin 5) the power supply will be restarted via the slow start circuit.
If the fault condition has cleared, then normal operation will be resumed. If the fault condition is persistent, the duty factor of the pulses is again reduced to zero and the protection cycle is repeated.

The number of times this action is repeated (n) for a persisting fault condition is now determined by: n = C4/C5.

## APPLICATION INFORMATION (continued)

*Remote control input*

For this application the capacitor on pin 4 has to be replaced by a resistor with a value between 4,7 and 18 kΩ. When the externally applied voltage $V_{4\text{-}16} > 5,6$ V, the circuit switches off; switching on occurs when $V_{4\text{-}16} < 4,5$ V and the normal starting-up procedure is followed. Pin 4 is internally connected to an emitter-follower, with an emitter voltage of 1,5 V.

### 5. Slow start and transfer characteristics for low feedback voltages

*Slow start*

An external shunt capacitor (C5 = 4,7 μF) and resistor (R5 = 270 kΩ) are connected between pins 5 and 16. The network controls the rate at which the duty factor increases from zero to its steady-state value after switch-on. It provides protection against surges in the power transistor.

*Transfer characteristic for low feedback voltages*

The duty factor transfer characteristic for low feedback voltages can be influenced by R5.
The transfer for three different resistor values is given in Fig. 7.

*'Smooth' remote ON/OFF*

The ON/OFF information should be applied to pin 5 via a high ohmic resistor, a high OFF-level gives a slow rising voltage at pin 5, which results in a slowly decreasing duty factor.

### 6. Over-current protection input

A voltage proportional to the current in the power switching device is applied to the integrated circuit between pins 6 and 16. The circuit trips on both positive and negative polarity. When the tripping level is reached, the output pulse is immediately blocked and the starting circuit is activated again.

### 7. Over-voltage protection input

When the voltage applied to this pin exceeds the threshold level the protection circuit will operate. The tripping level is about the same as the reference voltage on pin 10.

### 8. Feedback voltage input

The control loop input is applied to pin 8. This pin is internally connected to one input of a differential amplifier, functioning as an amplitude comparator, the other input of which is connected to the reference source on pin 10.
Under normal operating conditions, the voltage on pin 8 will be about equal to the reference voltage on pin 10. For further information refer to the Figs 7 and 8.

### 9. 12 V positive supply

The maximum voltage that may be applied is 14 V. Where this is derived from an unstabilized supply rail, a regulator diode (12 V) should be connected between pins 9 and 16 to ensure that the maximum voltage does not exceed 14 V. When the voltage on this pin falls below a minimum of 8,6 V (typically 9,4 V), the protection circuit will switch-off the power supply.

### 10. Reference input

An external reference diode must be connected between this pin and pin 16.
The reference voltage must be between 5,6 and 6,6 V. The IC delivers about 1 mA into the external regulator diode. When the external load on the regulator diode approaches this current, replenishment of the current can be obtained by connecting a suitable resistor between pins 9 and 10. A higher reference voltage value up to 7,5 V is allowed when use is made of a duty factor limiting resistor < 27 kΩ between pins 12 and 16.

### 11. Output

An external resistor determines the output current fed into the base of the driver transistor. The output circuit uses an n-p-n transistor with 3 series-connected clamping diodes to the internal 12 V supply rail. This provides a low impedance in the "ON" state, that is with the drive transistor turned-off.

### 12. Maximum duty factor adjustment/smoothing

*Maximum duty factor adjustment*

Pin 12 is connected to the output voltage of the amplitude comparator ($V_{10\text{-}8}$). This voltage is internally connected to one input of a differential amplifier, the other input of which is connected to the sawtooth voltage of the horizontal oscillator. A high voltage on pin 12 results in a low duty factor. This enables the maximum duty factor to be adjusted by limiting the voltage by connecting pin 12 to the emitter of an n-p-n transistor used as a voltage source.
Fig. 9 plots the maximum duty factor as a function of the voltage applied to pin 12. If some spread is acceptable the maximum duty factor can also be limited by connecting a resistor from pin 12 to pin 16. A resistor of 12 kΩ limits the maximum duty factor to about 50%. This application also reduces the total IC gain.

*Smoothing*

Any double pulsing of the IC due to circuit layout can be suppressed by connecting a capacitor of about 470 pF between pins 12 and 16.

### 13. Oscillator timing network

The timing network comprises a capacitor between pins 13 and 16, and a resistor between pin 13 and the reference voltage on pin 10.
The charging current for the capacitor (C13) is derived from the voltage reference diode connected to pin 10 and discharged via an internal resistor of about 330 Ω.

### 14. Reactance stage reference voltage

This pin is connected to an emitter follower which determines the nominal reference voltage for the reactance stage (1,4 V for reference voltage $V_{10\text{-}16}$ = 6,1 V). Free-running frequency is obtained when pins 14 and 15 are short-circuited.

### 15. Reactance stage input

The output voltage of the phase detector (pin 1) is connected to pin 15 via a resistor. The voltage applied to pin 15 shifts the upper level of the voltage sensor of the oscillator thus changing the oscillator frequency and phase. The time constant network is connected between 14 and 15. Control sensitivity is typically 5 kHz/V.

### 16. Negative supply (ground)

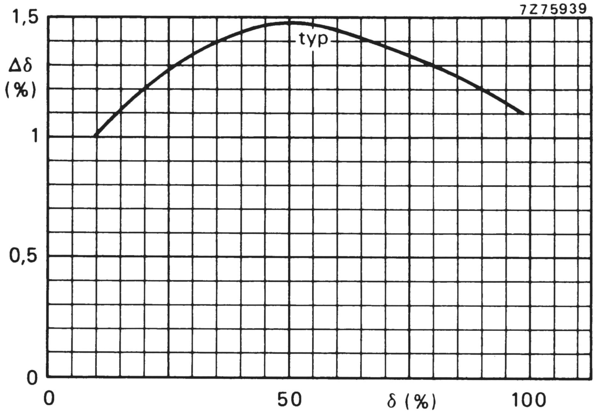


Fig. 6 Duty factor change as a function of initial duty factor; at 1 mV error amplifier input change; $\Delta V_{8\text{-}10(p\text{-}p)} = 1$ mV.

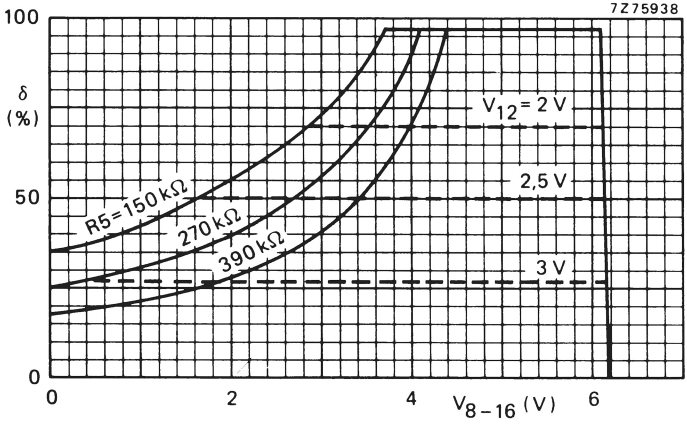


Fig. 7 Duty factor of output pulses as a function of feedback input voltage ($V_{8\text{-}16}$) with R5 as a parameter and $V_{12\text{-}16}$ as a limiting value; $V_{10\text{-}16} = 6{,}1$ V.

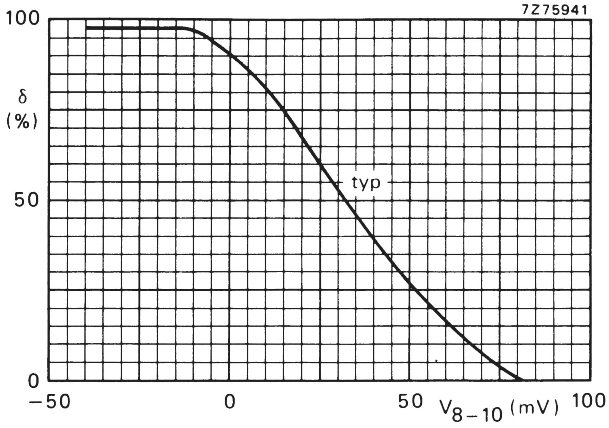


Fig. 8 Duty factor of output pulses as a function of error amplifier input ($V_{8-10}$); $V_{10-16}$ = 6,1 V.

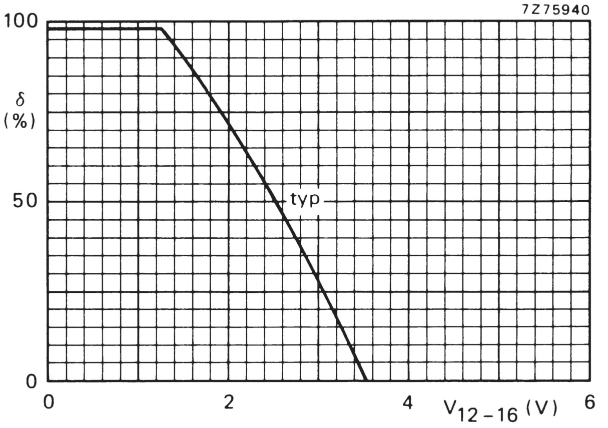


Fig. 9 Maximum duty factor limitation as a function of the voltage applied to pin 12; $V_{10-16}$ = 6,1 V.

# HORIZONTAL COMBINATION

The TDA2593 is a monolithic integrated circuit intended for use in colour television receivers in combination with TDA2510, TDA2520, TDA2560 as well as with TDA3500, TDA3510 and TDA3520. The circuit incorporates the following functions:

- horizontal oscillator based on the threshold switching principle
- phase comparison between sync pulse and oscillator voltage ($\varphi_1$)
- internal key pulse for phase detector ($\varphi_1$) (additional noise limiting)
- phase comparison between line flyback pulse and oscillator voltage ($\varphi_2$)
- larger catching range obtained by coincidence detector ($\varphi_3$; between sync and key pulse)
- switch for changing the filter characteristic and the gate circuit (VCR-operation)
- sync separator
- noise separator
- vertical sync separator and output stage
- colour burst keying and line flyback blanking pulse generator
- phase shifter for the output pulse
- output pulse duration switching
- output stage with separate supply voltage for direct drive of thyristor deflection circuits
- low supply voltage protection

## QUICK REFERENCE DATA

| | | | | |
|---|---|---|---|---|
| Supply voltage | $V_{1\text{-}16}$ | typ. | 12 | V |
| Supply current | $I_1$ | typ. | 30 | mA |
| **Input signals** | | | | |
| Sync separator input voltage (peak-to-peak value) | $V_{9\text{-}16(p\text{-}p)}$ | | 3 to 4 | V |
| Noise separator input voltage (peak-to-peak value) | $V_{10\text{-}16(p\text{-}p)}$ | | 3 to 4 | V |
| Pulse duration switch input voltage | | | | |
| at t = 7 μs (thyristor driving) | $V_{4\text{-}16}$ | | 9,4 to $V_{1\text{-}16}$ | V |
| at t = 14 μs + $t_d$ (transistor driving) | $V_{4\text{-}16}$ | | 0 to 3,5 | V |
| at t = 0 (input 4 open or $V_{3\text{-}16} = 0$) | $V_{4\text{-}16}$ | | 5,4 to 6,6 | V |
| **Output signals** | | | | |
| Vertical sync output pulse (peak-to peak value) | $V_{8\text{-}16(p\text{-}p)}$ | typ. | 11 | V |
| Burst gating output pulse (peak-to-peak value) | $V_{7\text{-}16(p\text{-}p)}$ | typ. | 11 | V |
| Line drive pulse (peak-to-peak value) | $V_{3\text{-}16(p\text{-}p)}$ | typ. | 10,5 | V |

## PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).

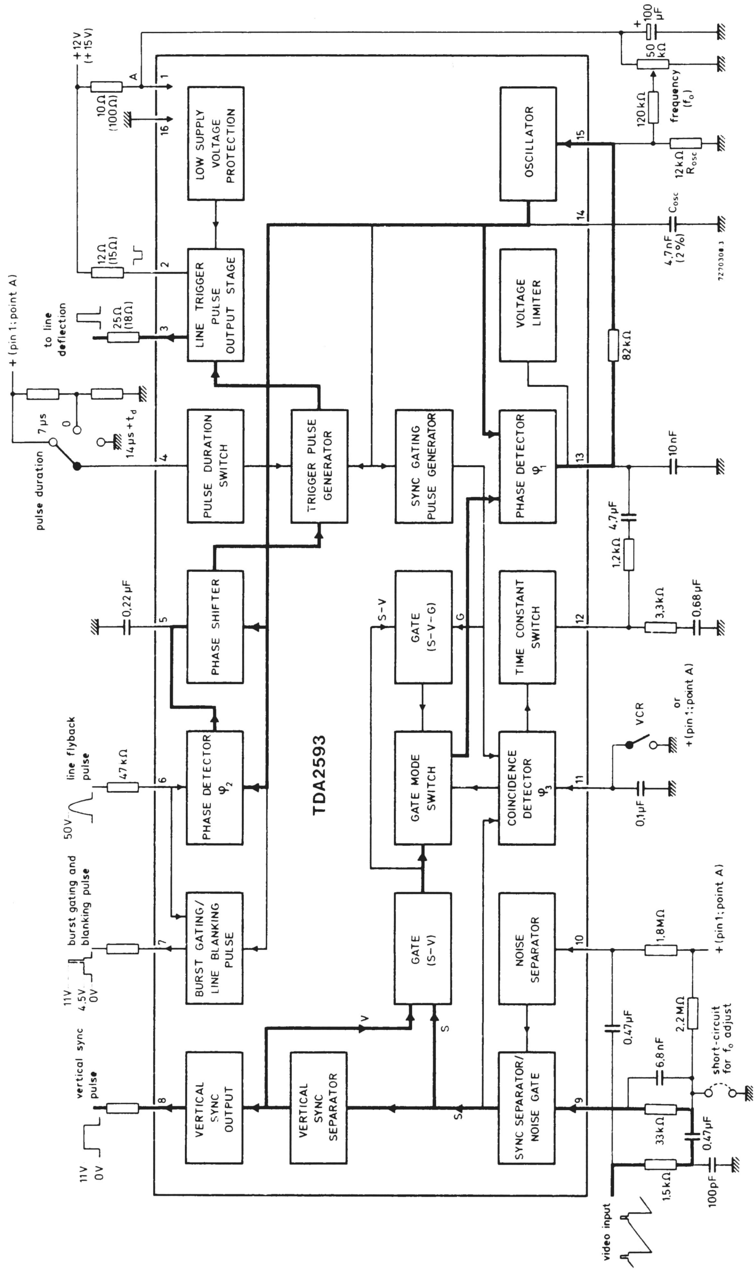

TDA2593
LOW SUPPLY VOLTAGE PROTECTION
LINE TRIGGER PULSE OUTPUT STAGE
PULSE DURATION SWITCH
TRIGGER PULSE GENERATOR
PHASE SHIFTER
PHASE DETECTOR φ2
BURST GATING/ LINE BLANKING PULSE
VERTICAL SYNC OUTPUT
VERTICAL SYNC SEPARATOR
GATE (S-V)
GATE MODE SWITCH
GATE (S-V-G)
SYNC GATING PULSE GENERATOR
OSCILLATOR
VOLTAGE LIMITER
PHASE DETECTOR φ1
TIME CONSTANT SWITCH
COINCIDENCE DETECTOR φ3
NOISE SEPARATOR
SYNC SEPARATOR/ NOISE GATE
+12V (+15V)
10Ω (100Ω)
A
1
16
12Ω (15Ω)
2
25Ω (18Ω)
3
to line deflection
+ (pin 1; point A)
pulse duration
7µs
0
14µs + td
4
0,22µF
5
47kΩ
6
line flyback pulse
50V
burst gating and blanking pulse
11V
4.5V
0V
7
vertical sync pulse
11V
0V
8
S-V
G
V
S
S
100 µF
50 kΩ
120kΩ
frequency (fo)
15
12kΩ Rosc
14
Cosc
4,7nF (2%)
82kΩ
13
10nF
4,7µF
1,2kΩ
12
3,3kΩ
0,68µF
VCR
or + (pin 1; point A)
11
0,1µF
10
1,8MΩ
+ (pin 1; point A)
0,47µF
2,2MΩ
6,8nF
short-circuit for fo adjust
9
33kΩ
0,47µF
1,5kΩ
100pF
video input
7Z70308.3

Fig. 1 Block diagram.

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | | |
|---|---|---|---|---|
| Supply voltage | | | | |
| at pin 1 (voltage source) | $V_{1\text{-}16}$ | max. | 13,2 | V |
| at pin 2 | $V_{2\text{-}16}$ | max. | 18 | V |
| Voltages | | | | |
| Pin 4 | $V_{4\text{-}16}$ | max. | 13,2 | V |
| Pin 9 | $\pm V_{9\text{-}16}$ | max. | 6 | V |
| Pin 10 | $\pm V_{10\text{-}16}$ | max. | 6 | V |
| Pin 11 | $V_{11\text{-}16}$ | max. | 13,2 | V |
| Currents | | | | |
| Pins 2 and 3 (thyristor driving) (peak value) | $I_{2M}, -I_{3M}$ | max. | 650 | mA |
| Pins 2 and 3 (transistor driving) (peak value) | $I_{2M}, -I_{3M}$ | max. | 400 | mA |
| Pin 4 | $I_4$ | max. | 1 | mA |
| Pin 6 | $\pm I_6$ | max. | 10 | mA |
| Pin 7 | $-I_7$ | max. | 10 | mA |
| Pin 11 | $I_{11}$ | max. | 2 | mA |
| Total power dissipation | $P_{tot}$ | max. | 800 | mW |
| Storage temperature | $T_{stg}$ | | −25 to + 125 | °C |
| Operating ambient temperature | $T_{amb}$ | | −20 to + 70 | °C |

**CHARACTERISTICS** at $V_{1\text{-}16} = 12$ V; $T_{amb} = 25$ °C; measured in Fig. 1

**Sync separator**

| | | | | |
|---|---|---|---|---|
| Input switching voltage | $V_{9\text{-}16}$ | typ. | 0,8 | V |
| Input keying current | $I_9$ | | 5 to 100 | μA |
| Input leakage current at $V_{9\text{-}16} = -5$ V | $I_9$ | $<$ | 1 | μA |
| Input switching current | $I_9$ | $\leqslant$ | 5 | μA |
| Switch off current | $I_9$ | $>$ | 100 | μA |
| | | typ. | 150 | μA |
| Input signal (peak-to-peak value) | $V_{9\text{-}16(p\text{-}p)}$ | | 3 to 4 | V* |

---

* Permissible range 1 to 7 V.

**Noise separator**

| | | | | |
|---|---|---|---|---|
| Input switching voltage | $V_{10-16}$ | typ. | 1,4 | V |
| Input keying current | $I_{10}$ | | 5 to 100 | μA |
| Input switching current | $I_{10}$ | > | 100 | μA |
| | | typ. | 150 | μA |
| Input leakage current at $V_{10-16} = -5$ V | $I_{10}$ | < | 1 | μA |
| Input signal (peak-to-peak value) | $V_{10-16(p-p)}$ | | 3 to 4 | V * |
| Permissible superimposed noise signal (peak-to-peak value) | $V_{10-16(p-p)}$ | < | 7 | V |

**Line flyback pulse**

| | | | | |
|---|---|---|---|---|
| Input current | $I_6$ | typ. | 1 | mA |
| | | | 0,02 to 2 | mA |
| Input switching voltage | $V_{6-16}$ | typ. | 1,4 | V |
| Input limiting voltage | $V_{6-16}$ | | −0,7 to + 1,4 | V |

**Switching on VCR**

| | | | | |
|---|---|---|---|---|
| Input voltage | $V_{11-16}$ | | 0 to 2,5 | V |
| | $V_{11-16}$ | | 9 to $V_{1-16}$ | V |
| Input current | $-I_{11}$ | < | 200 | μA |
| | $I_{11}$ | < | 2 | mA |

**Pulse duration switch**

| | | | | |
|---|---|---|---|---|
| For t = 7 μs (thyristor driving) | | | | |
| Input voltage | $V_{4-16}$ | | 9,4 to $V_{1-16}$ | V |
| Input current | $I_4$ | > | 200 | μA |
| For $t = 14\ \mu s + t_d$ (transistor driving) | | | | |
| Input voltage | $V_{4-16}$ | | 0 to 3,5 | V |
| Input current | $-I_4$ | > | 200 | μA |
| For t = 0; $V_{3-16} = 0$ or input pin 4 open | | | | |
| Input voltage | $V_{4-16}$ | | 5,4 to 6,6 | V |
| Input current | $I_4$ | typ. | 0 | μA |

---

* Permissible range 1 to 7 V.

| | | | | |
|---|---|---|---|---|
| **Vertical sync pulse** (positive-going) | | | | |
| Output voltage (peak-to-peak value) | $V_{8\text{-}16(p\text{-}p)}$ | ><br>typ. | 10<br>11 | V<br>V |
| Output resistance | $R_8$ | typ. | 2 | kΩ |
| Delay between leading edge of input and output signal | $t_{on}$ | typ. | 15 | µs |
| Delay between trailing edge of input and output signal | $t_{off}$ | typ. | $t_{on}$ | µs |
| **Burst gating pulse** (positive-going) | | | | |
| Output voltage (peak-to-peak value) | $V_{7\text{-}16(p\text{-}p)}$ | ><br>typ. | 10<br>11 | V<br>V |
| Output resistance | $R_7$ | typ. | 70 | Ω |
| Pulse duration; $V_{7\text{-}16} = 7$ V | $t_p$ | typ. | 4<br>3,7 to 4,3 | µs<br>µs |
| Phase relation between middle of sync pulse at the input and the leading edge of the burst gating pulse; $V_{7\text{-}16} = 7$ V | t | typ. | 2,65<br>2,15 to 3,15 | µs<br>µs |
| Output trailing edge current | $I_7$ | typ. | 2 | mA |
| **Line flyback-blanking pulse** (positive-going) | | | | |
| Output voltage (peak-to-peak value) | $V_{7\text{-}16(p\text{-}p)}$ | | 4 to 5 | V |
| Output resistance | $R_7$ | typ. | 70 | Ω |
| Output trailing edge current | $I_7$ | typ. | 2 | mA |
| **Line drive pulse** (positive-going) | | | | |
| Output voltage (peak-to-peak value) | $V_{3\text{-}16(p\text{-}p)}$ | typ. | 10,5 | V |
| Output resistance | | | | |
| for leading edge of line pulse | $R_3$ | typ. | 2,5 | Ω |
| for trailing edge of line pulse | $R_3$ | typ. | 20 | Ω |
| Pulse duration (thyristor driving) $V_{4\text{-}16} = 9{,}4$ to $V_{1\text{-}16}$ V | $t_p$ | typ. | 7<br>5,5 to 8,5 | µs<br>µs |
| Pulse duration (transistor driving) $V_{4\text{-}16} = 0$ to 4 V; $t_{fp} = 12$ µs | $t_p$ | | 14 + $t_d$ | µs* |
| Supply voltage for switching off the output pulse | $V_{1\text{-}16}$ | typ. | 4 | V |
| **Overall phase relation** | | | | |
| Phase relation between middle of sync pulse and the middle of the flyback pulse | t | typ. | 2,6 | µs** |
| Tolerance of phase relation | $\lvert \Delta t \rvert$ | < | 0,7 | µs |

---

* $t_d$ = switch-off delay of line output stage.

** Line flyback pulse duration $t_{fp} = 12$ µs.

The adjustment of the overall phase relation and consequently the leading edge of the line drive pulse occurs automatically by phase control $\varphi_2$.

| | | | | |
|---|---|---|---|---|
| If additional adjustment is applied it can be arranged by current supply at pin 5 such that | $\Delta I_5/\Delta t$ | typ. | 30 | μA/μs |

### Oscillator

| | | | | |
|---|---|---|---|---|
| Threshold voltage low level | $V_{14\text{-}16}$ | typ. | 4,4 | V |
| Threshold voltage high level | $V_{14\text{-}16}$ | typ. | 7,6 | V |
| Discharge current | $\pm I_{14}$ | typ. | 0,47 | mA |
| Frequency; free running ($C_{osc}$ = 4,7 nF; $R_{osc}$ = 12 kΩ) | $f_o$ | typ. | 15,625 | kHz |
| Spread of frequency | $\Delta f_o/f_o$ | < | ± 5 | %* |
| Frequency control sensitivity | $\Delta f_o/\Delta I_{15}$ | typ. | 31 | Hz/μA |
| Adjustment range of network in circuit (Fig. 1) | $\Delta f_o/f_o$ | typ. | ± 10 | % |
| Influence of supply voltage on frequency | $\frac{\Delta f_o/f_o}{\Delta V/V_{nom}}$ | < | ± 0,05 | %* |
| Change of frequency when $V_{1\text{-}16}$ drops to 5 V | $\Delta f_o$ | < | ± 10 | %* |
| Temperature coefficient of oscillator frequency | | < | $\pm 10^{-4}$ | Hz/K* |

### Phase comparison $\varphi_1$

| | | | | |
|---|---|---|---|---|
| Control voltage range | $V_{13\text{-}16}$ | | 3,8 to 8,2 | V |
| Control current (peak value) | $\pm I_{13M}$ | | 1,9 to 2,3 | mA |
| Output leakage current at $V_{13\text{-}16}$ = 4 to 8 V | $I_{13}$ | < | 1 | μA |
| Output resistance at $V_{13\text{-}16}$ = 4 to 8 V | $R_{13}$ | high ohmic | | ** |
| at $V_{13\text{-}16}$ < 3,8 V or > 8,2 V | $R_{13}$ | low ohmic | | ▲ |
| Control sensitivity | | typ. | 2 | kHz/μs |
| Catching and holding range (82 kΩ beteeen pins 13 and 15) | $\Delta f$ | typ. | ± 780 | Hz |
| Spread of catching and holding range | $\Delta(\Delta f)$ | typ. | ± 10 | %* |

---

* Excluding external component tolerances.

** Current source.

▲ Emitter follower.

### Phase comparison $\varphi_2$ and phase shifter

| | | | | |
|---|---|---|---|---|
| Control voltage range | $V_{5\text{-}16}$ | | 5,4 to 7,6 | V |
| Control current (peak value) | $\pm I_{5M}$ | typ. | 1 | mA |
| Output resistance | | | | |
| at $V_{5\text{-}16} = 5{,}4$ to $7{,}6$ V | | high ohmic | | * |
| at $V_{5\text{-}16} < 5{,}4$ V or $> 7{,}6$ V | $R_5$ | typ. | 8 | kΩ |
| Input leakage current | | | | |
| $V_{5\text{-}16} = 5{,}4$ to $7{,}6$ V | $I_5$ | < | 5 | μA |
| Permissible delay between leading edge of output pulse and leading edge of flyback pulse ($t_{fp} = 12$ μs) | $t_d$ | < | 15 | μs |
| Static control error | $\Delta t/\Delta t_d$ | < | 0,2 | % |

### Coincidence detector $\varphi_3$

| | | | | |
|---|---|---|---|---|
| Output voltage | $V_{11\text{-}16}$ | | 0,5 to 6 | V |
| Output current (peak value) | | | | |
| without coincidence | $I_{11M}$ | typ. | 0,1 | mA |
| with coincidence | $-I_{11M}$ | typ. | 0,5 | mA |

### Time constant switch

| | | | | |
|---|---|---|---|---|
| Output voltage | $V_{12\text{-}16}$ | typ. | 6 | V |
| Output current (limited) | $\pm I_{12}$ | < | 1 | mA |
| Output resistance | | | | |
| at $V_{11\text{-}16} = 2{,}5$ to $7$ V | $R_{12}$ | typ. | 0,1 | kΩ |
| at $V_{11\text{-}16} < 1{,}5$ V or $> 9$ V | $R_{12}$ | typ. | 60 | kΩ |

### Internal gating pulse

| | | | | |
|---|---|---|---|---|
| Pulse duration | $t_p$ | typ. | 7,5 | μs |

---

* Current source.

# HORIZONTAL COMBINATION

The TDA2594 is a monolithic integrated circuit intended for use in colour television receivers. The circuit incorporates the following functions:

- Horizontal oscillator based on the threshold switching principle.
- Phase comparison between sync pulse and oscillator voltage ($\varphi_1$).
- Internal key pulse for phase detector ($\varphi_1$) (additional noise limiting).
- Phase comparison between line flyback pulse and oscillator voltage ($\varphi_2$).
- Larger catching range obtained by coincidence detector ($\varphi_3$; between sync and key pulse).
- Switch for changing the filter characteristic and the gate circuit (VCR-operation).
- Sync separator.
- Noise separator.
- Vertical sync separator and output stage.
- Colour burst keying and line flyback blanking pulse generator and clamp circuit for vertical blanking.
- Phase shifter for the output pulse.
- Output pulse duration for transistor deflection systems.
- External switching off of the line trigger pulse.
- Output stage with separate supply voltage.
- Low supply voltage protection.
- Transmitter identification and muting circuit, and vertical sync switch-off.

## QUICK REFERENCE DATA

| | | | | |
|---|---|---|---|---|
| Supply voltage | $V_{1\text{-}18} = V_S$ | typ. | 12 | V |
| Supply current | $I_1$ | typ. | 30 | mA |
| **Input signals** | | | | |
| Sync separator input voltage (peak-to-peak value) | $V_{11\text{-}18(p\text{-}p)}$ | typ. | 3 | V* |
| Noise separator input voltage (peak-to-peak value) | $V_{12\text{-}18(p\text{-}p)}$ | typ. | 3 | V* |
| Pulse duration switch input voltage | | | | |
| at t = 14 µs + $t_d$ (transistor driving) | $V_{4\text{-}18}$ | | 0 to 3,5 | V |
| at t = 0 ($V_{3\text{-}18}$ = 0); input 4 open ($I_4$ = 0) | $V_{4\text{-}18}$ | | 5,4 to 6,6 | V |
| **Output signals** | | | | |
| Vertical sync output pulse (peak-to-peak value) | $V_{8\text{-}18(p\text{-}p)}$ | typ. | 11 | V |
| Burst key output pulse (peak-to-peak value) | $V_{7\text{-}18(p\text{-}p)}$ | typ. | 11 | V |
| Line drive-pulse (peak-to-peak value) | $V_{3\text{-}18(p\text{-}p)}$ | typ. | 10 | V |

* Permissible range: 1 to 7 V.

## PACKAGE OUTLINE

18-lead DIL; plastic (SOT-102DS).

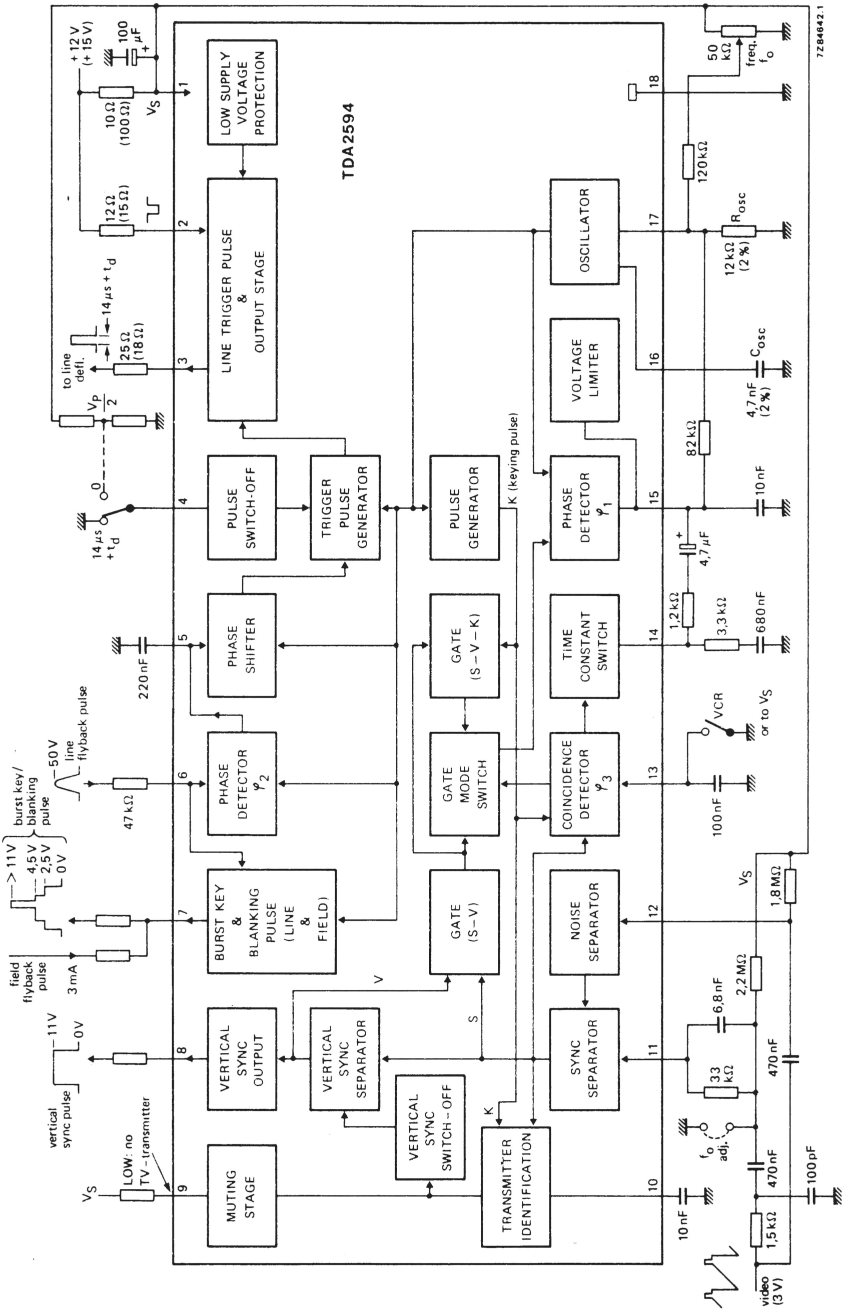

TDA2594
LOW SUPPLY VOLTAGE PROTECTION
LINE TRIGGER PULSE & OUTPUT STAGE
PULSE SWITCH-OFF
TRIGGER PULSE GENERATOR
PHASE SHIFTER
PHASE DETECTOR φ2
BURST KEY & BLANKING PULSE (LINE & FIELD)
VERTICAL SYNC OUTPUT
VERTICAL SYNC SEPARATOR
VERTICAL SYNC SWITCH-OFF
MUTING STAGE
TRANSMITTER IDENTIFICATION
PULSE GENERATOR
K (keying pulse)
GATE (S – V – K)
GATE MODE SWITCH
GATE (S – V)
OSCILLATOR
VOLTAGE LIMITER
PHASE DETECTOR φ1
TIME CONSTANT SWITCH
COINCIDENCE DETECTOR φ3
NOISE SEPARATOR
SYNC SEPARATOR
V
S
K
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
+12 V (+15 V)
100 μF
10 Ω (100 Ω)
V_S
12 Ω (15 Ω)
14 μs + t_d
25 Ω (18 Ω)
to line defl.
V_P/2
0
14 μs + t_d
220 nF
line flyback pulse
−50 V
47 kΩ
burst key/ blanking pulse
> 11 V
4,5 V
2,5 V
0 V
field flyback pulse
3 mA
11 V
0 V
vertical sync pulse
LOW: no TV-transmitter
V_S
7Z84642.1
50 kΩ
freq. f_o
120 kΩ
R_osc
12 kΩ (2 %)
C_osc
4,7 nF (2 %)
82 kΩ
10 nF
4,7 μF
1,2 kΩ
3,3 kΩ
680 nF
VCR
or to V_S
100 nF
V_S
1,8 MΩ
2,2 MΩ
6,8 nF
33 kΩ
470 nF
f_o adj.
470 nF
100 pF
10 nF
1,5 kΩ
video (3 V)

Fig. 1 Block diagram.

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | | |
|---|---|---|---|---|
| Supply voltage | | | | |
| at pin 1 (voltage source) | $V_{1\text{-}18} = V_S$ | max. | 13,2 | V |
| at pin 2 | $V_{2\text{-}18}$ | max. | 18 | V |
| Voltages | | | | |
| Pin 4 | $V_{4\text{-}18}$ | max. | 13,2 | V |
| Pin 9 | $V_{9\text{-}18}$ | max. | 18 | V |
| | $-V_{9\text{-}18}$ | max. | 0,5 | V |
| Pin 11 | $\pm V_{11\text{-}18}$ | max. | 6 | V |
| Pin 12 | $\pm V_{12\text{-}18}$ | max. | 6 | V |
| Pin 13 | $V_{13\text{-}18}$ | max. | 13,2 | V |
| Currents | | | | |
| Pins 2 and 3 (transistor driving) (peak value) | $I_{2M}, -I_{3M}$ | max. | 400 | mA |
| Pin 4 | $I_4$ | max. | 1 | mA |
| Pin 6 | $\pm I_6$ | max. | 10 | mA |
| Pin 7 | $-I_7$ | max. | 5 | mA |
| Pin 9 | $I_9$ | max. | 10 | mA |
| Pin 13 | $I_{13}$ | max. | 2 | mA |
| Total power dissipation | $P_{tot}$ | max. | 800 | mW |
| Storage temperature range | $T_{stg}$ | −25 to | +125 | °C |
| Operating ambient temperature range | $T_{amb}$ | −20 to | +70 | °C |

**CHARACTERISTICS** at $V_{1\text{-}18} = 12$ V; $T_{amb} = 25$ °C; measured in Fig. 1

**Sync separator** (pin 11)

| | | | | |
|---|---|---|---|---|
| Input switching voltage | $V_{11\text{-}18}$ | typ. | 0,8 | V |
| Input keying current | $I_{11}$ | | 5 to 100 | μA |
| Input leakage current at $V_{11\text{-}18} = -5$ V | $I_{11}$ | ⩽ | 1 | μA |
| Input switching current | $I_{11}$ | ⩽ | 5 | μA |
| Switch off current | $I_{11}$ | ⩾ | 100 | μA |
| | | typ. | 150 | μA |
| Input signal (peak-to-peak value) | $V_{11\text{-}18(p\text{-}p)}$ | | 3 to 4 | V* |

* Permissible range 1 to 7 V.

**Noise separator** (pin 12)

| | | | | |
|---|---|---|---|---|
| Input switching voltage | $V_{12-18}$ | typ. | 1,4 | V |
| Input keying current | $I_{12}$ | | 5 to 100 | μA |
| Input switching current | $I_{12}$ | ≥<br>typ. | 100<br>150 | μA<br>μA |
| Input leakage current at $V_{12-18} = -5$ V | $I_{12}$ | ≤ | 1 | μA |
| Input signal (peak-to-peak value) | $V_{12-18(p-p)}$ | | 3 to 4 | V* |
| Permissible superimposed noise signal (peak-to-peak value) | $V_{12-18(p-p)}$ | ≤ | 7 | V |

**Line flyback pulse** (pin 6)

| | | | | |
|---|---|---|---|---|
| Input current | $I_6$ | ≥<br>typ. | 0,02<br>1 | mA<br>mA |
| Input switching voltage | $V_{6-18}$ | typ. | 1,4 | V |
| Input limiting voltage | $V_{6-18}$ | | −0,7 to +1,4 | V |

**Switching on VCR** (pin 13)

| | | | | |
|---|---|---|---|---|
| Input voltage | $V_{13-18}$<br>or: $V_{13-18}$ | | 0 to 2,5<br>9 to $V_S$ | V<br>V |
| Input current | $-I_{13}$<br>or: $I_{13}$ | ≤<br>≤ | 200<br>2 | μA<br>mA |

**Pulse switching off** (pin 4)

For t = 0; input pin 4 open or $V_{3-18} = 0$

| | | | | |
|---|---|---|---|---|
| Input voltage | $V_{4-18}$ | | 5,4 to 6,6 | V |
| Input current | $I_4$ | typ. | 0 | μA |

**Vertical sync pulse** (positive-going) (pin 8)

| | | | | |
|---|---|---|---|---|
| Output voltage (peak-to-peak value) | $V_{8-18(p-p)}$ | ≥<br>typ. | 10<br>11 | V<br>V |
| Output resistance | $R_8$ | typ. | 2 | kΩ |
| Delay between leading edge of input and output signal | $t_{on}$ | typ. | 15 | μs |
| Delay between trailing edge of input and output signal | $t_{off}$ | ≥ | $t_{on}$ | μs |
| Switching off the vertical sync pulse | $V_{10-18}$ | ≤ | 3 | V |

**Burst key pulse** (positive-going) (pin 7)

| | | | | |
|---|---|---|---|---|
| Output voltage | $V_{7-18}$ | ≥<br>typ. | 10<br>11 | V<br>V |
| Output resistance | $R_7$ | typ. | 70 | Ω |
| Pulse duration; $V_{7-18} = 7$ V | $t_p$ | typ. | 4<br>3,7 to 4,3 | μs<br>μs |
| Phase relation between middle of sync pulse at the input and the leading edge of the burst key pulse; $V_{7-18} = 7$ V | t | typ. | 2,65<br>2,15 to 3,15 | μs<br>μs |
| Output trailing edge current | $I_7$ | typ. | 2 | mA |
| Saturation voltage during line scan | $V_{7-18}$ | ≤ | 1 | V |

* Permissible range 1 to 7 V.

**Line flyback-blanking pulse** (positive-going) (pin 7)

| | | | |
|---|---|---|---|
| Output voltage | $V_{7\text{-}18}$ | | 4,1 to 4,9 V |
| Output resistance | $R_7$ | typ. | 70 Ω |
| Output trailing edge current | $I_7$ | typ. | 2 mA |

**Field flyback/blanking pulse** (pin 7)

| | | | |
|---|---|---|---|
| Output voltage with externally forced in current $I_7$ = 2,4 to 3,6 mA | $V_{7\text{-}18}$ | | 2 to 3 V |
| Output resistance at $I_7$ = 3 mA | $R_7$ | typ. | 70 Ω |

**TV-transmitter identification output** (pin 9; open collector)

| | | | |
|---|---|---|---|
| Output voltage at $I_9$ = 3 mA; no TV-transmitter | $V_{9\text{-}18}$ | $\leqslant$ | 0,5 V |
| Output resistance at $I_9$ = 3 mA; no TV-transmitter | $R_9$ | $\leqslant$ | 100 Ω |
| Output current at $V_{10\text{-}18} \geqslant 3$ V; TV-transmitter identified | $I_9$ | $\leqslant$ | 5 μA |

**TV-transmitter identification** (pin 10)

When receiving a TV signal the voltage $V_{10\text{-}18}$ will change from $\leqslant 1$ V to $\geqslant 7$ V.

**Line drive pulse** (positive-going)

| | | | |
|---|---|---|---|
| Output voltage (peak-to-peak value) | $V_{3\text{-}18(p\text{-}p)}$ | typ. | 10 V |
| Output resistance | | | |
| for leading edge of line pulse | $R_3$ | typ. | 2,5 Ω |
| for trailing edge of line pulse | $R_3$ | typ. | 20 Ω |
| Pulse duration (transistor driving) $V_{4\text{-}18}$ = 0 to 3,5 V; $-I_4 \geqslant 200$ μA; $t_{fp}$ = 12 μs | $t_p$ | | $14 + t_d$ μs* |
| Supply voltage for switching off the output pulse | $V_{1\text{-}18}$ | typ. | 4 V |

**Overall phase relation**

| | | | |
|---|---|---|---|
| Phase relation between middle of sync pulse and the middle of the flyback pulse | $\Delta t$ | typ. | 2,6 ± 0,7 μs** |

The adjustment of the overall phase relation and consequently the leading edge of the line drive pulse occurs automatically by phase control $\varphi_2$.

If additional adjustment is applied it can be arranged by current supply at pin 5, such that:

| | | | |
|---|---|---|---|
| Supplying current | $\Delta I/\Delta t$ | typ. | 30 μA/μs |

---

* $t_d$ = switch-off delay of line output stage.

** Line flyback pulse duration $t_{fp}$ = 12 μs.

**Oscillator** (pins 16 and 17)

| | | | | |
|---|---|---|---|---|
| Threshold voltage low level | $V_{16\text{-}18}$ | typ. | 4,4 | V |
| Threshold voltage high level | $V_{16\text{-}18}$ | typ. | 7,6 | V |
| Charging current | $\pm I_{16}$ | typ. | 0,47 | mA |
| Frequency; free running ($C_{osc}$ = 4,7 nF; $R_{osc}$ = 12 kΩ) | $f_o$ | typ. | 15,625 | kHz |
| Spread of frequency | $\Delta f_o$ | ≤ | ± 5 | %▲ |
| Frequency control sensitivity | $\Delta f_o/\Delta_{17}$ | typ. | 31 | Hz/µA |
| Adjustment range of network in circuit (Fig. 1) | $\Delta f_o$ | typ. | ± 10 | % |
| Influence of supply voltage on frequency; reference at $V_S$ = 12 V | $\frac{\Delta f_o/f_o}{\Delta V/V_{nom}}$ | ≤ | ± 0,05 | %▲ |
| Change of frequency when $V_S$ drops to 5 V; reference at $V_S$ = 12 V | $\Delta f_o$ | ≤ | ± 10 | %▲ |
| Temperature coefficient of oscillator frequency | TC | ≤ | $\pm 10^{-4}$ | $K^{-1}$ ▲ |

**Phase comparison** $\varphi 1$ (pin 15)

| | | | | |
|---|---|---|---|---|
| Control voltage range | $V_{15\text{-}18}$ | | 4,1 to 7,9 | V |
| Control current (peak value) | $\pm I_{15M}$ | | 1,8 to 2,2 | mA |
| Output leakage current at $V_{15\text{-}18}$ = 4,3 to 7,7 V | $I_{15}$ | ≤ | 1 | µA |
| Output resistance | | | | |
| at $V_{15\text{-}18}$ = 4,3 to 7,7 V | $R_{13}$ | high ohmic | | * |
| at $V_{15\text{-}18} \leq 4{,}1$ V or $\geq 7{,}9$ V | $R_{13}$ | low ohmic | | ** |
| Control sensitivity | | typ. | 2 | kHz/µs |
| Catching and holding range (82 kΩ between pins 15 and 17) | $\Delta f$ | typ. | ± 680 | Hz |
| Spread of catching and holding range | $\Delta(\Delta f)$ | typ. | ± 12 | %▲ |

**Phase comparison** $\varphi 2$ **and phase shifter** (pin 5)

| | | | | |
|---|---|---|---|---|
| Control voltage range | $V_{5\text{-}18}$ | | 5,4 to 7,6 | V |
| Control current (peak value) | $\pm I_{5M}$ | typ. | 1 | mA |
| Output resistance at $V_{5\text{-}18}$ = 5,4 to 7,6 V | $R_5$ | high ohmic | | * |
| Input leakage current at $V_{5\text{-}18}$ = 5,4 to 7,6 V | $I_5$ | ≤ | 5 | µA |
| Permissible delay between leading edge of output pulse and leading edge of flyback pulse ($t_{fp}$ = 12 µs) | $t_d$ | ≤ | 15,5 | µs |
| Static control error | $\Delta t/\Delta t_d$ | ≤ | 0,2 | % |

**Coincidence detector** $\varphi 3$ (pin 13)

| | | | | |
|---|---|---|---|---|
| Output voltage | $V_{13\text{-}18}$ | | 0,5 to 6 | V |
| Output current (peak value) | | | | |
| without coincidence | $I_{13M}$ | typ. | 0,1 | mA |
| with coincidence | $-I_{13M}$ | typ. | 0,5 | mA |

* Current source.

** Emitter follower.

▲ Excluding external component tolerances.

**Time constant switch** (pin 14)

| | | | |
|---|---|---|---|
| Output voltage | $V_{14\text{-}18}$ | typ. | 6 V |
| Output current (limited) | $\pm I_{14}$ | typ. | 1 mA |
| Output resistance | | | |
| at $V_{13\text{-}18} = 3{,}5$ to 7 V | $R_{14}$ | typ. | 0,1 kΩ |
| at $V_{13\text{-}18} \leqslant 2{,}5$ V or $\geqslant 9$ V | $R_{14}$ | typ. | 60 kΩ |

**Internal keying pulse**

| | | | |
|---|---|---|---|
| Pulse duration | $t_p$ | typ. | 7,5 µs |

# HORIZONTAL COMBINATION

## GENERAL DESCRIPTION

The TDA2595 is a monolithic integrated circuit intended for use in colour television receivers. The circuit incorporates the following functions:

- Positive video input; capacitively coupled (source impedance $< 200\ \Omega$)
- Adaptive sync separator; slicing level at 50% of sync amplitude
- Internal vertical pulse separator with double slope integrator
- Output stage for vertical sync pulse or composite sync depending on the load; both are switched off at muting
- $\varphi_1$ phase control between horizontal sync and oscillator
- Coincidence detector $\varphi_3$ for automatic time-constant switching; overruled by the VCR switch
- Time-constant switch between two external time-constants or loop-gain; both controlled by the coincidence detector $\varphi_3$
- $\varphi_1$ gating pulse controlled by coincidence detector $\varphi_3$
- Mute circuit depending on TV transmitter identification
- $\varphi_2$ phase control between line flyback and oscillator; the slicing levels for $\varphi_2$ control and horizontal blanking can be set separately
- Burst keying and horizontal blanking pulse generation, in combination with clamping of the vertical blanking pulse (three-level sandcastle)
- Horizontal drive output with constant duty cycle inhibited by the protection circuit or the supply voltage sensor
- Detector for too low supply voltage
- Protection circuit for switching off the horizontal drive output continuously if the input voltage is below 4 V or higher than 8 V
- Line flyback control causing the horizontal blanking level at the sandcastle output continuously in case of a missing flyback pulse
- Spot-suppressor controlled by the line flyback control

## QUICK REFERENCE DATA

| | | | |
|---|---|---|---|
| Supply voltage (pin 15) | $V_{15\text{-}5} = V_P$ | typ. | 12 V |
| Sync pulse amplitude (positive video) | $V_{i(p\text{-}p)}$ | min. | 50 mV |
| Horizontal output current | $I_4$ | max. | 30 mA |

## PACKAGE OUTLINE

18-lead DIL; plastic (SOT-102CS).

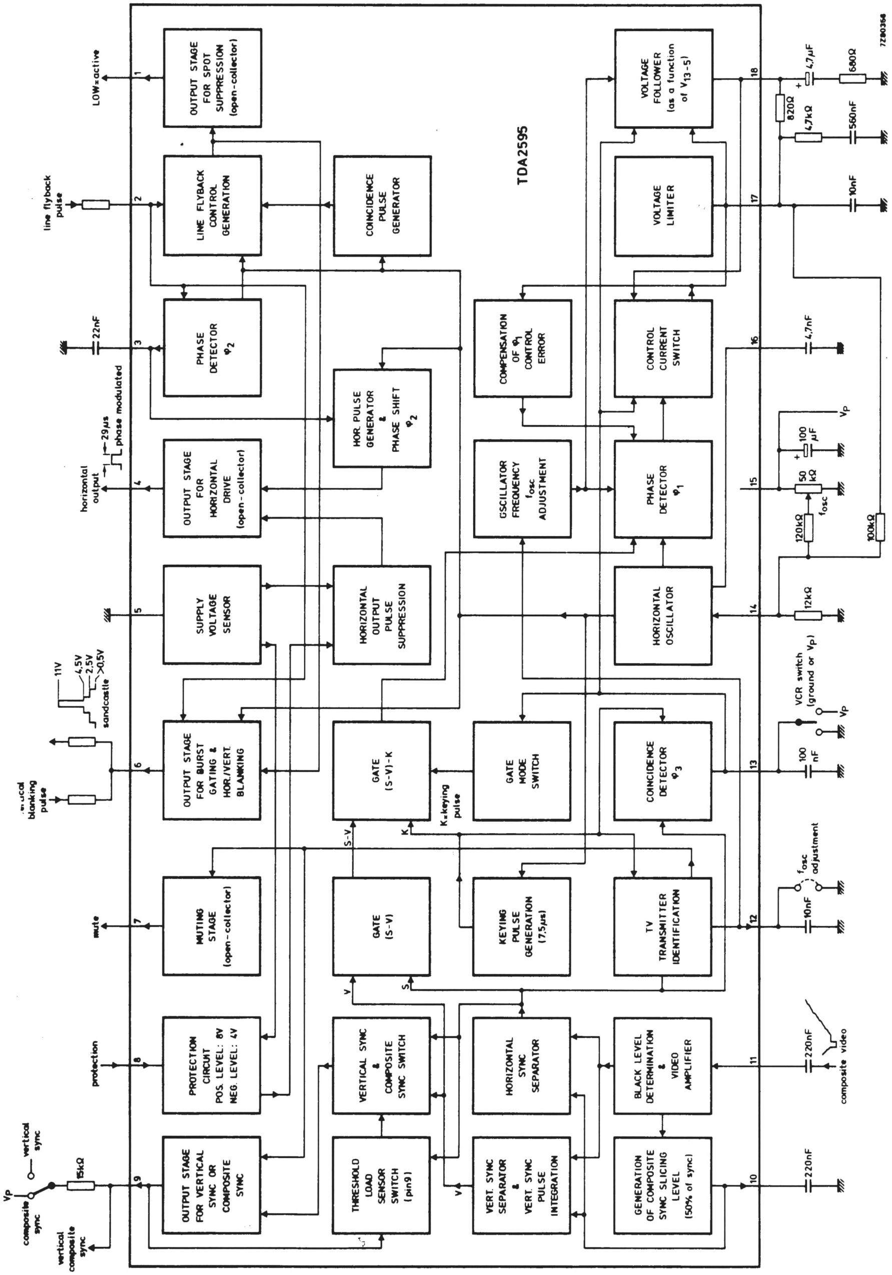

TDA2595
7Z80364
OUTPUT STAGE FOR SPOT SUPPRESSION (open-collector)
LINE FLYBACK CONTROL GENERATION
COINCIDENCE PULSE GENERATOR
PHASE DETECTOR φ2
HOR. PULSE GENERATOR & PHASE SHIFT φ2
OUTPUT STAGE FOR HORIZONTAL DRIVE (open-collector)
SUPPLY VOLTAGE SENSOR
HORIZONTAL OUTPUT PULSE SUPPRESSION
OUTPUT STAGE FOR BURST GATING & HOR./VERT. BLANKING
GATE (S-V)-K
GATE MODE SWITCH
MUTING STAGE (open-collector)
GATE (S-V)
KEYING PULSE GENERATION (7,5μs)
PROTECTION CIRCUIT POS. LEVEL: 8V NEG. LEVEL: 4V
VERTICAL SYNC & COMPOSITE SYNC SWITCH
HORIZONTAL SYNC SEPARATOR
OUTPUT STAGE FOR VERTICAL SYNC OR COMPOSITE SYNC
THRESHOLD LOAD SENSOR SWITCH (pin9)
VERT. SYNC SEPARATOR & VERT. SYNC PULSE INTEGRATION
VOLTAGE FOLLOWER (as a function of V13-5)
VOLTAGE LIMITER
COMPENSATION OF φ1 CONTROL ERROR
CONTROL CURRENT SWITCH
OSCILLATOR FREQUENCY fosc ADJUSTMENT
PHASE DETECTOR φ1
HORIZONTAL OSCILLATOR
COINCIDENCE DETECTOR φ3
TV TRANSMITTER IDENTIFICATION
BLACK LEVEL DETERMINATION & VIDEO AMPLIFIER
GENERATION OF COMPOSITE SYNC SLICING LEVEL (50% of sync)
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
LOW=active
line flyback pulse
22nF
horizontal output
29μs
phase modulated
11V
4,5V
2,5V
0,5V
sandcastle
vertical blanking pulse
mute
protection
Vp
vertical sync
composite sync
15kΩ
vertical composite sync
S-V
K
K=keying pulse
V
S
4,7μF
680Ω
820Ω
4,7kΩ
560nF
10nF
4,7nF
Vp
100 μF
50 kΩ
fosc
120kΩ
100kΩ
12kΩ
VCR switch (ground or Vp)
100 nF
fosc adjustment
10nF
220nF
composite video
220nF

Fig. 1 Block diagram.

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | | |
|---|---|---|---|---|
| Supply voltage (pin 15) | $V_{15\text{-}5} = V_P$ | max. | 13,2 | V |
| Voltages at: | | | | |
| pins 1, 4 and 7 | $V_{1;4;7\text{-}5}$ | max. | 18 | V |
| pins 8, 13 and 18 | $V_{8;13;18\text{-}5}$ | max. | $V_P$ | V |
| pin 11 (range) | $V_{11\text{-}5}$ | | −0,5 to + 6 | V |
| Currents at: | | | | |
| pin 1 | $I_1$ | max. | 10 | mA |
| pin 2 (peak value) | $\pm I_{2M}$ | max. | 10 | mA |
| pin 4 | $I_4$ | max. | 100 | mA |
| pin 6 (peak value) | $\pm I_{6M}$ | max. | 6 | mA |
| pin 7 | $I_7$ | max. | 10 | mA |
| pin 8 (range) | $I_8$ | | −5 to + 1 | mA |
| pin 9 (range) | $I_9$ | | −10 to + 3 | mA |
| pin 18 | $\pm I_{18}$ | max. | 10 | mA |
| Total power dissipation | $P_{tot}$ | max. | 800 | mW |
| Storage temperature range | $T_{stg}$ | | −25 to + 125 | °C |
| Operating ambient temperature range | $T_{amb}$ | | −20 to + 70 | °C |

DEVELOPMENT SAMPLE DATA

## CHARACTERISTICS

$V_P = 12$ V; $T_{amb} = 25$ °C; measured in Fig. 1; unless otherwise specified

| parameter | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| **Composite video input and sync separator** (pin 11)<br>(internal black level determination) | | | | | |
| Input signal (positive video; standard signal; peak-to-peak value) | $V_{11\text{-}5(p\text{-}p)}$ | 0,2 | 1 | 3 | V |
| Sync pulse amplitude (independent of video content) | $V_{11\text{-}5(p\text{-}p)}$ | 50 | – | – | mV |
| Generator resistance | $R_G$ | – | – | 200 | Ω |
| Input current during: | | | | | |
| video | $I_{11}$ | – | 5 | – | µA |
| sync pulse | $-I_{11}$ | – | 40 | – | µA |
| black level | $-I_{11}$ | – | 30 | – | µA |
| **Composite sync generation** (pin 10)<br>horizontal slicing level at 50% of the sync pulse amplitude | | | | | |
| Capacitor current during: | | | | | |
| video | $I_{10}$ | – | 12 | – | µA |
| sync pulse | $-I_{10}$ | – | 170 | – | µA |
| **Vertical sync pulse generation**<br>slicing level at 25% (50% between black level and horizontal slicing level); pin 9 | | | | | |
| Output voltage | $V_{9\text{-}5}$ | 10 | – | – | V |
| Pulse duration | $t_p$ | – | 190 | – | µs |
| Delay with respect to the vertical sync pulse (leading edge) | $t_d$ | – | 45 | – | µs |
| Pulse-mode control | | | | | |
| output current for vertical sync pulse (dual integrated) | | no current applied at pin 9 | | | |
| output current for horizontal and vertical sync pulse (non-integrated separated signal) | | current applied via a resistor of 15 kΩ from $V_P$ to pin 9 | | | |

| parameter | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| **Horizontal oscillator** (pins 14 and 16) | | | | | |
| Frequency; free running | $f_{osc}$ | – | 15 625 | – | Hz |
| Reference voltage for $f_{osc}$ | $V_{14\text{-}5}$ | – | 6 | – | V |
| Frequency control sensitivity | $\Delta f_{osc}/\Delta I_{14}$ | – | 31 | – | Hz/µA |
| Adjustment range of circuit Fig. 1 | $\Delta f_{osc}$ | – | ± 10 | – | % |
| Spread of frequency | $\Delta f_{osc}$ | – | – | 5 | % |
| Frequency dependency (excluding tolerance of external components) | | | | | |
| with supply voltage ($V_P$ = 12 V) | $\frac{\Delta f_{osc}/f_{osc}}{\Delta V_{15\text{-}5}/V_{15\text{-}5}}$ | – | ± 0,05 | – | |
| with supply voltage drop of 5 V | $\Delta f_{osc}$ | – | – | 10 | % |
| with temperature | TC | – | – | $\pm 10^{-4}$ | $K^{-1}$ |
| Capacitor current during: | | | | | |
| charging | $-I_{16}$ | – | 1024 | – | µA |
| discharging | $I_{16}$ | – | 313 | – | µA |
| Sawtooth voltage timing (pin 14) | | | | | |
| rise time | $t_r$ | – | 49 | – | µs |
| fall time | $t_f$ | – | 15 | – | µs |
| **Horizontal output pulse** (pin 4) | | | | | |
| Output voltage LOW at $I_4$ = 30 mA | $V_{4\text{-}5}$ | – | – | 0,5 | V |
| Pulse duration (HIGH) | $t_p$ | – | 29 ± 1,5 | – | µs |
| Supply voltage for switching off the output pulse (pin 15) | $V_P$ | – | 4 | – | V |

DEVELOPMENT SAMPLE DATA

**CHARACTERISTICS** (continued)

| parameter | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| **Phase comparison $\varphi_1$** (pin 17) | | | | | |
| Control voltage range | $V_{17\text{-}5}$ | 3,55 | – | 8,3 | V |
| Leakage current at $V_{17\text{-}5}$ = 3,55 to 8,3 V | $I_{17}$ | – | – | 1 | μA |
| Control current for external time-constant switch | $\pm I_{17}$ | 1,8 | 2 | 2,2 | mA |
| Control current at $V_{18\text{-}5} = V_{15\text{-}5}$ and $V_{13\text{-}5} < 2$ V or $V_{13\text{-}5} > 9,5$ V | $\pm I_{17}$ | – | 8 | – | mA |
| Control current at $V_{18\text{-}5} = V_{15\text{-}5}$ and $V_{13\text{-}5}$ = 2 to 9,5 V | $\pm I_{17}$ | 1,8 | 2 | 2,2 | mA |
| Horizontal oscillator control | | | | | |
| control sensitivity | $S_\varphi$ | 6 | – | – | kHz/μs |
| catching and holding range | $\Delta f_{osc}$ | – | ± 680 | – | Hz |
| spread of catching and holding range | $\Delta f_{osc}$ | – | ± 10 | – | % |
| Internal keying pulse at $V_{13\text{-}5}$ = 2,9 to 9,5 V | $t_p$ | – | 7,5 | – | μs |
| Time-constant switch | | | | | |
| slow time-constant at | $V_{13\text{-}5}$ | 9,5 | – | 2 | V |
| fast time-constant at | $V_{13\text{-}5}$ | 2 | – | 9,5 | V |
| Impedance converter offset voltage (slow time-constant) | $\pm V_{17\text{-}18}$ | – | – | 3 | mV |
| Output resistance | | | | | |
| slow time-constant | $R_{18\text{-}5}$ | – | – | 10 | Ω |
| fast time-constant | $R_{18\text{-}5}$ | high impedance | | | |
| Leakage current | $I_{18}$ | – | – | 1 | μA |

DEVELOPMENT SAMPLE DATA

| parameter | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| **Coincidence detector** $\varphi_3$ (pin 13) | | | | | |
| Output voltage | | | | | |
| without coincidence with composite video signal | $V_{13\text{-}5}$ | – | – | 1 | V |
| without coincidence without composite video signal (noise) | $V_{13\text{-}5}$ | – | – | 2 | V |
| with coincidence with composite video signal | $V_{13\text{-}5}$ | – | 6 | – | V |
| Output current | | | | | |
| without coincidence with composite video signal | $I_{13}$ | – | 50 | – | μA |
| with coincidence with composite video signal | $-I_{13}$ | – | 300 | – | μA |
| Switching current | | | | | |
| at $V_{13\text{-}5} = V_P - 0{,}5$ V | $I_{13}$ | – | – | 100 | μA |
| at $V_{13\text{-}5} = 0{,}5$ V (average value) | $I_{13(av)}$ | – | – | 100 | μA |
| **Phase comparison** $\varphi_2$ (pins 2 and 3) (see note 1) | | | | | |
| **Input for line flyback pulse** (pin 2) | | | | | |
| Switching level for $\varphi_2$ comparison | $V_{2\text{-}5}$ | – | 3 | – | V |
| Switching level for horizontal blanking and flyback control | $V_{2\text{-}5}$ | – | 3 | – | V |
| Input voltage limiting | $V_{2\text{-}5}$<br>or: | –<br>– | –0,7<br>+4,5 | –<br>– | V<br>V |
| Switching current | | | | | |
| at horizontal flyback | $I_2$ | 0,01 | 1 | – | mA |
| at horizontal scan | $I_2$ | – | – | 2 | μA |
| **Phase detector output** (pin 3) | | | | | |
| Control current for $\varphi_2$ | $\pm I_3$ | – | 1 | – | mA |
| Control range | $\Delta t_{\varphi 2}$ | – | 19 | – | μs |
| Static control error | $\Delta t/\Delta t_d$ | – | – | 0,2 | % |
| Leakage current | $I_3$ | – | – | 5 | μA |

**CHARACTERISTICS** (continued)

| parameter | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| **Phase comparison** $\varphi_2$ (pins 2 and 3) (continued) | | | | | |
| Phase relation between middle of the horizontal sync pulse and the middle of the line flyback pulse at $t_{fp}$ = 12 µs (note 2) | $\Delta t$ | – | 2,6 ± 0,7 | – | µs |
| If additional adjustment is required, it can be arranged by applying a current at pin 3, such that for applied current: | $\Delta I/\Delta t$ | – | 30 | – | µA/µs |
| **Burst gating pulse** (pin 6; note 3) | | | | | |
| Output voltage | $V_{6\text{-}5}$ | 10 | 11 | – | V |
| Pulse duration | $t_p$ | 3,7 | 4 | 4,3 | µs |
| Phase relation between middle of sync pulse at the input and the leading edge of the burst gating pulse at $V_{6\text{-}5}$ = 7 V | $t_{\varphi 6}$ | 2,15 | 2,65 | 3,15 | µs |
| Output trailing edge current | $I_6$ | – | 2 | – | mA |
| **Horizontal blanking pulse** (pin 6) (note 3) | | | | | |
| Output voltage | $V_{6\text{-}5}$ | 4,2 | 4,5 | 4,9 | V |
| Output trailing edge current | $I_6$ | – | 2 | – | mA |
| Saturation voltage at horizontal scan | $V_{6\text{-}5sat}$ | – | – | 0,5 | V |
| **Clamping circuit for vertical blanking pulse** (pin 6; note 3) | | | | | |
| Output voltage at $I_6$ = 2,8 mA | $V_{6\text{-}5}$ | 2,15 | 2,5 | 3 | V |
| Minimum output current at $V_{6\text{-}5} > 2,15$ V | $I_{6min}$ | – | 2,3 | – | mA |
| Maximum output current at $V_{6\text{-}5} < 3$ V | $I_{6max}$ | – | 3,3 | – | mA |
| **TV-transmitter identification** (pin 12) | | | | | |
| Output voltage<br>no TV transmitter | $V_{12\text{-}5}$ | – | – | 1 | V |
| TV transmitter identified | $V_{12\text{-}5}$ | 7 | – | – | V |

| parameter | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| **Mute output** (pin 7) | | | | | |
| Output voltage at $I_7$ = 3 mA no TV transmitter | $V_{7\text{-}5}$ | – | – | 0,5 | V |
| Output resistance at $I_7$ = 3 mA no TV transmitter | $R_{7\text{-}5}$ | – | – | 100 | Ω |
| Output leakage current at $V_{12\text{-}5} > 3$ V TV transmitter identified | $I_7$ | – | – | 5 | μA |
| **Protection circuit (beam-current/ EHT voltage protection)** (pin 8) | | | | | |
| No-load voltage for $I_8 = 0$ (operative condition) | $V_{8\text{-}5}$ | – | 6 | – | V |
| Threshold at positive-going voltage | $V_{8\text{-}5}$ | – | 8 ± 0,8 | – | V |
| Threshold at negative-going voltage | $V_{8\text{-}5}$ | – | 4 ± 0,4 | – | V |
| Current limiting for $V_{8\text{-}5}$ = 1 to 8,5 V | $\pm I_8$ | – | 60 | – | μA |
| Input resistance for $V_{8\text{-}5} > 8{,}5$ V | $R_{8\text{-}5}$ | – | 3 | – | kΩ |
| Response delay of threshold switch | $t_d$ | – | 10 | – | μs |
| **Control output of line flyback pulse control** (pin 1) | | | | | |
| Saturation voltage at standard operation; $I_1$ = 3 mA | $V_{1\text{-}5sat}$ | – | – | 0,5 | V |
| Output leakage current in case of break in transmission | $I_1$ | – | – | 5 | μA |

**Notes to the characteristics**

1. Phase comparison between horizontal oscillator and the line flyback pulse. Generation of a phase modulated ($\varphi_2$) horizontal output pulse with constant duration.
2. $t_{fp}$ is the line flyback pulse duration.
3. Three-level sandcastle pulse.

# 5 W AUDIO POWER AMPLIFIER

The TDA2611A is a monolithic integrated circuit in a 9-lead single in-line (SIL) plastic package with a high supply voltage audio amplifier. Special features are:

- **possibility for increasing the input impedance**
- single in-line (SIL) construction for easy mounting
- very suitable for application in mains-fed apparatus
- extremely low number of external components
- thermal protection
- well defined open loop gain circuitry with simple quiescent current setting and fixed integrated closed loop gain

## QUICK REFERENCE DATA

| | | | | |
|---|---|---|---|---|
| Supply voltage range | $V_P$ | | 6 to 35 | V |
| Repetitive peak output current | $I_{ORM}$ | < | 1,5 | A |
| Output power at $d_{tot}$ = 10% | | | | |
| $V_P$ = 18 V; $R_L$ = 8 Ω | $P_o$ | typ. | 4,5 | W |
| $V_P$ = 25 V; $R_L$ = 15 Ω | $P_o$ | typ. | 5 | W |
| Total harmonic distortion at $P_o < 2$ W; $R_L$ = 8 Ω | $d_{tot}$ | typ. | 0,3 | % |
| Input impedance | $\lvert Z_i \rvert$ | typ. | 45 | kΩ |
| Total quiescent current at $V_P$ = 18 V | $I_{tot}$ | typ. | 25 | mA |
| Sensitivity for $P_o$ = 2,5 W; $R_L$ = 8 Ω | $V_i$ | typ. | 55 | mV |
| Operating ambient temperature | $T_{amb}$ | | −25 to + 150 | °C |
| Storage temperature | $T_{stg}$ | | −55 to + 150 | °C |

## PACKAGE OUTLINE

9-lead SIL; plastic (SOT-110B).

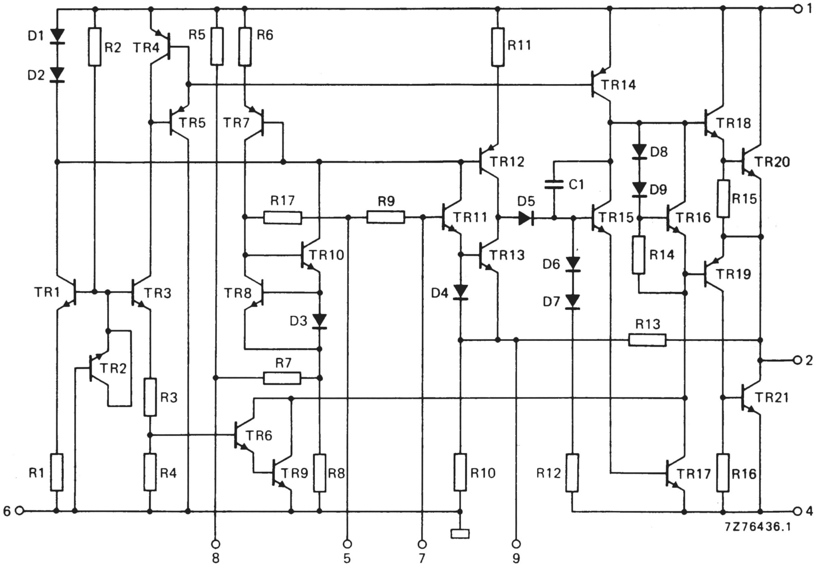

D1
D2
R2
TR4
R5
R6
R11
1
TR14
TR5
TR7
TR18
D8
TR12
TR20
C1
D9
R17
R9
D5
R15
TR11
TR15
TR16
TR10
R14
TR13
D6
TR1
TR3
TR8
D4
TR19
D3
D7
R13
TR2
R7
2
R3
TR21
TR6
R1
R4
TR9
R8
R10
R12
TR17
R16
6
4
7Z76436.1
8
5
7
9

Fig. 1 Circuit diagram; pin 3 not connected.

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | |
|---|---|---|---|
| Supply voltage | $V_P$ | max. | 35 V |
| Non-repetitive peak output current | $I_{OSM}$ | max. | 3 A |
| Repetitive peak output current | $I_{ORM}$ | max. | 1,5 A |
| Total power dissipation | see derating curves Fig. 2 | | |
| Storage temperature | $T_{stg}$ | −55 to + 150 °C | |
| Operating ambient temperature | $T_{amb}$ | −25 to + 150 °C | |

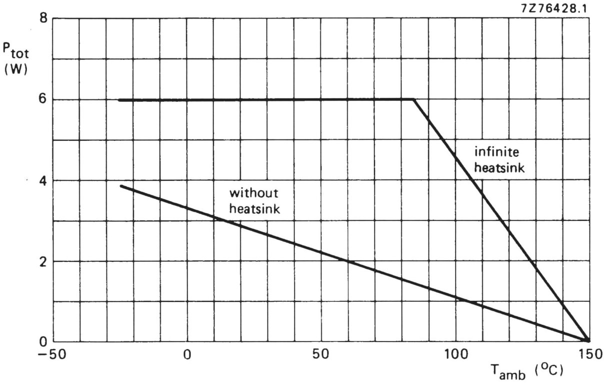


Fig. 2 Power derating curves.

## HEATSINK EXAMPLE

Assume $V_P = 18$ V; $R_L = 8\ \Omega$; $T_{amb} = 60$ °C maximum; $T_j = 150$ °C (max. for a 4 W application into an 8 Ω load, the maximum dissipation is about 2,2 W).
The thermal resistance from junction to ambient can be expressed as:

$$R_{th\ j\text{-}a} = R_{th\ j\text{-}tab} + R_{th\ tab\text{-}h} + R_{th\ h\text{-}a} = \frac{150 - 60}{2,2} = 41\ \text{K/W}.$$

Since $R_{th\ j\text{-}tab} = 11$ K/W and $R_{th\ tab\text{-}h} = 1$ K/W, $R_{th\ h\text{-}a} = 41 - (11 + 1) = 29$ K/W.

## D.C. CHARACTERISTICS

| | | | | |
|---|---|---|---|---|
| Supply voltage range | $V_P$ | | 6 to 35 | V |
| Repetitive peak output current | $I_{ORM}$ | < | 1,5 | A |
| Total quiescent current at $V_P$ = 18 V | $I_{tot}$ | typ. | 25 | mA |

## A.C. CHARACTERISTICS

$T_{amb}$ = 25 °C; $V_P$ = 18 V; $R_L$ = 8 Ω; f = 1 kHz unless otherwise specified; see also Fig. 3

| | | | | |
|---|---|---|---|---|
| A.F. output power at $d_{tot}$ = 10% | | | | |
| $V_P$ = 18 V; $R_L$ = 8 Ω | $P_o$ | > | 4 | W |
| | | typ. | 4,5 | W |
| $V_P$ = 12 V; $R_L$ = 8 Ω | $P_o$ | typ. | 1,7 | W |
| $V_P$ = 8,3 V; $R_L$ = 8 Ω | $P_o$ | typ. | 0,65 | W |
| $V_P$ = 20 V; $R_L$ = 8 Ω | $P_o$ | typ. | 6 | W |
| $V_P$ = 25 V; $R_L$ = 15 Ω | $P_o$ | typ. | 5 | W |
| Total harmonic distortion at $P_o$ = 2 W | $d_{tot}$ | typ. | 0,3 | % |
| | | < | 1 | % |
| Frequency response | | > | 15 | kHz |
| Input impedance | $\lvert Z_i \rvert$ | typ. | 45 | kΩ * |
| Noise output voltage at $R_S$ = 5 kΩ; B = 60 Hz to 15 kHz | $V_n$ | typ. | 0,2 | mV |
| | | < | 0,5 | mV |
| Sensitivity for $P_o$ = 2,5 W | $V_i$ | typ. | 55 | mV |
| | | | 44 to 66 | mV |

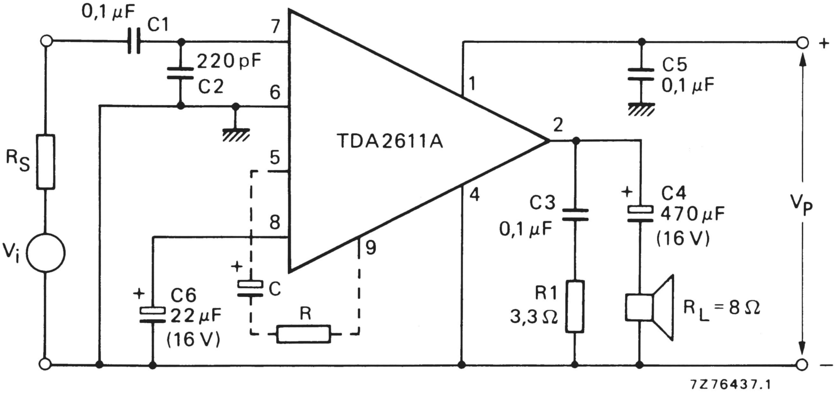

0,1 µF
C1
7
220 pF
C2
6
5
8
9
TDA2611A
1
2
4
C5
0,1 µF
+
−
$V_P$
$R_S$
$V_i$
+
C6
22 µF
(16 V)
+
C
R
C3
0,1 µF
R1
3,3 Ω
+
C4
470 µF
(16 V)
$R_L$ = 8 Ω
7Z76437.1

Fig. 3 Test circuit; pin 3 not connected.

---

* Input impedance can be increased by applying C and R between pins 5 and 9 (see also Figures 6 and 7).

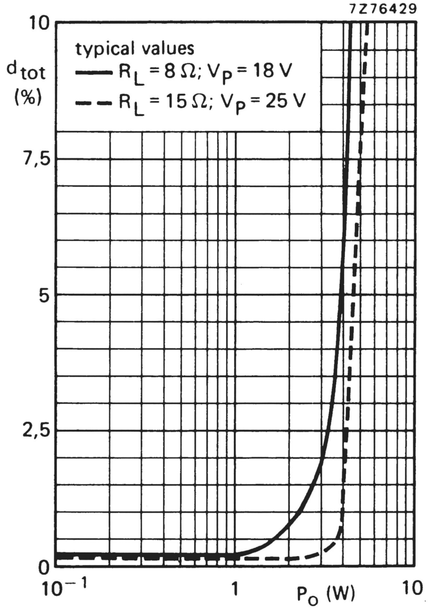


Fig. 4 Total harmonic distortion as a function of output power.

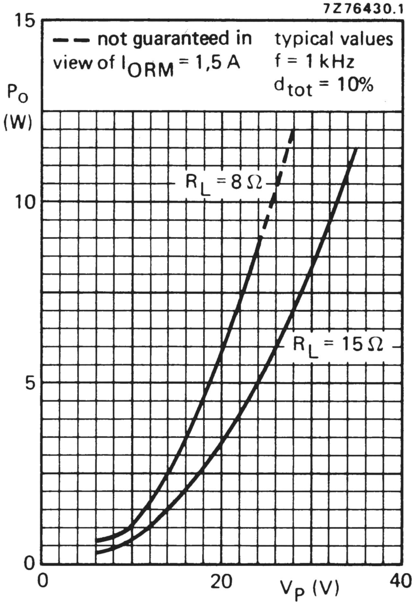


Fig. 5 Output power as a function of supply voltage.

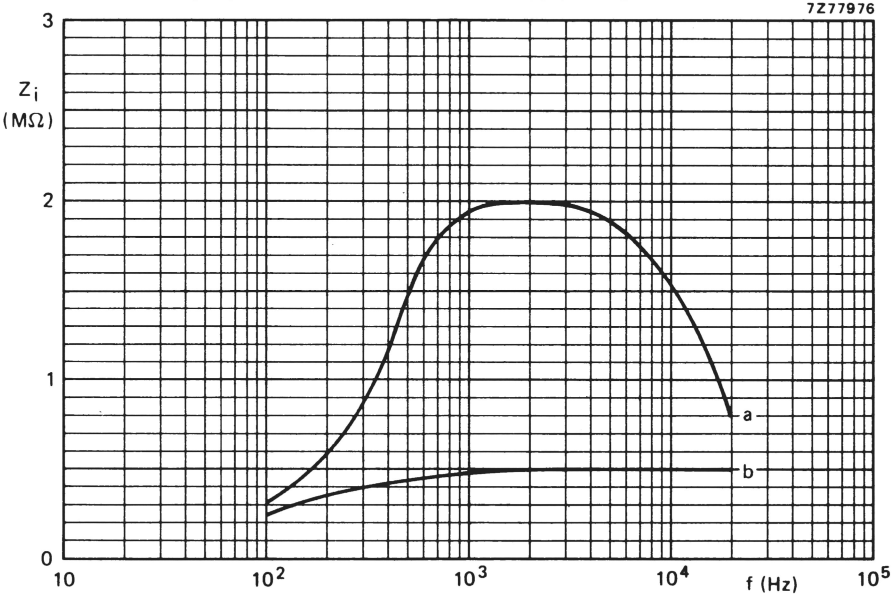


Fig. 6 Input impedance as a function of frequency; curve a for C = 1 $\mu$F, R = 0 Ω; curve b for C = 1 $\mu$F, R = 1 kΩ; circuit of Fig. 3; C2 = 10 pF; typical values.

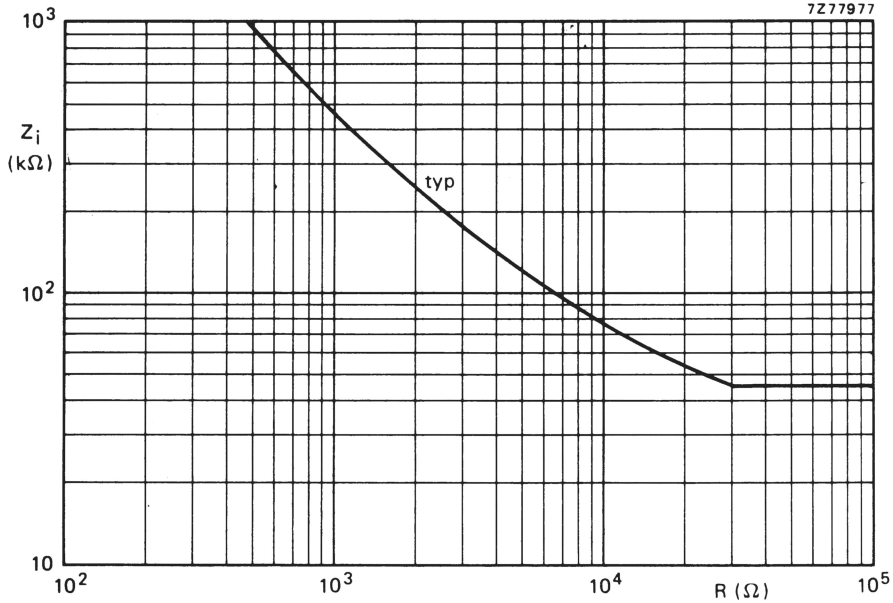


Fig. 7 Input impedance as a function of R in circuit of Fig. 3; C = 1 μF; f = 1 kHz.

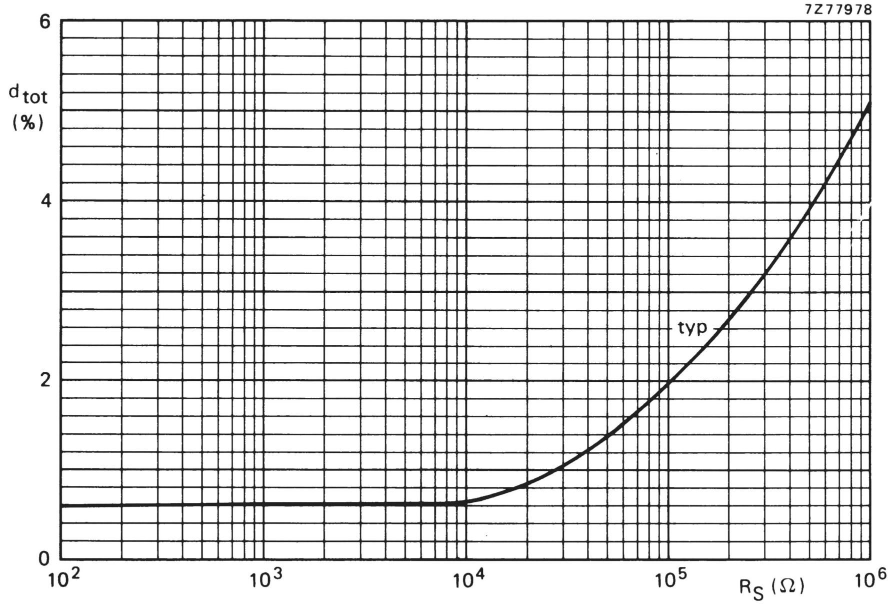
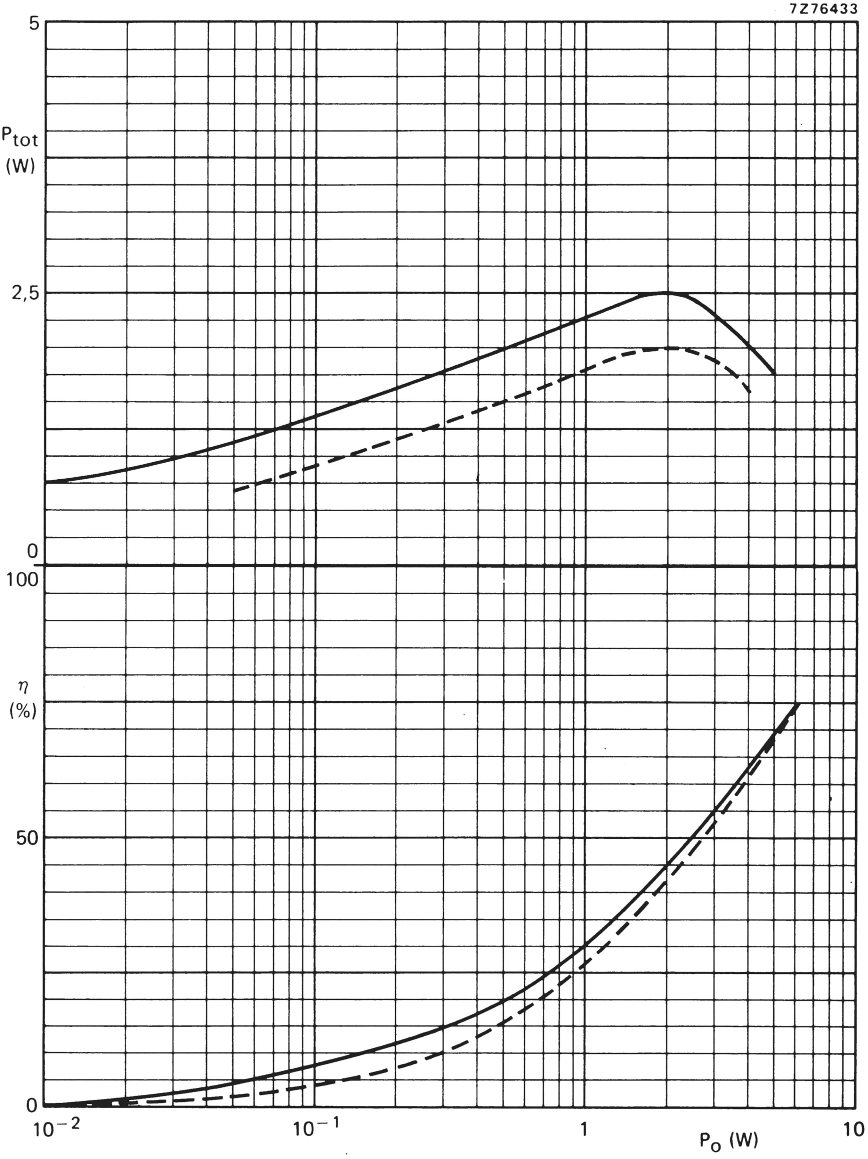


Fig. 8 Total harmonic distortion as a function of $R_S$ in the circuit of Fig. 3; $P_o$ = 3,5 W; f = 1 kHz.



—— $V_P = 25$ V; $R_L = 15\,\Omega$; f = 1 kHz

– – $V_P = 18$ V; $R_L = 8\,\Omega$; f = 1 kHz

Fig. 9 Total power dissipation and efficiency as a function of output power.

## APPLICATION INFORMATION

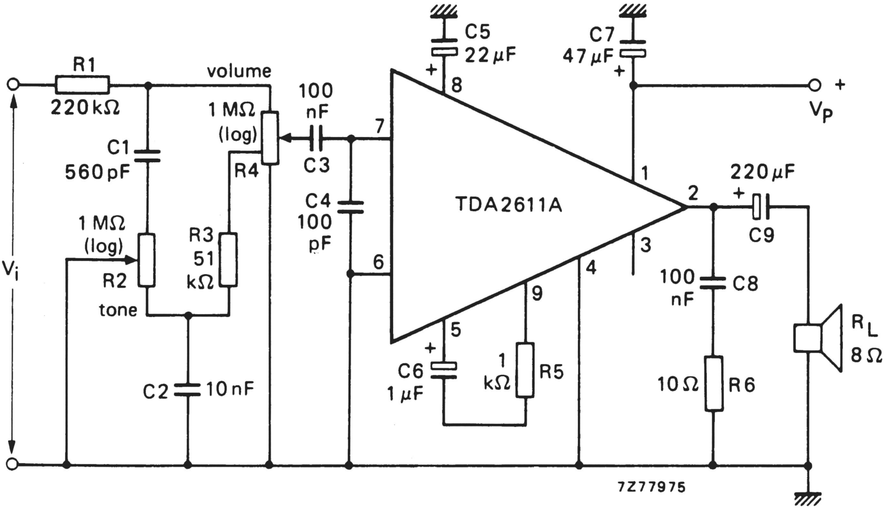

R1
220kΩ
C1
560pF
volume
1 MΩ
(log)
R4
100
nF
C3
C4
100
pF
7
6
R2
1 MΩ
(log)
tone
R3
51
kΩ
C2
10nF
Vi
C5
22 μF
8
C7
47 μF
TDA2611A
1
2
3
4
9
5
C6
1 μF
R5
1
kΩ
VP
220 μF
C9
100
nF
C8
10 Ω
R6
RL
8 Ω
7Z77975

Fig. 10 Ceramic pickup amplifier circuit.

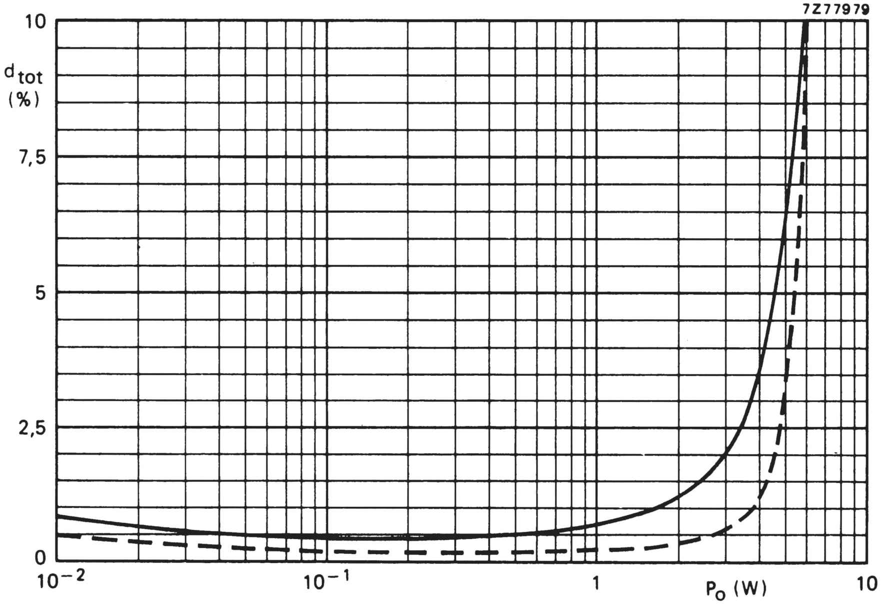


Fig. 11 Total harmonic distortion as a function of output power; —— with tone control; – – – without tone control; in circuit of Fig. 10; typical values.

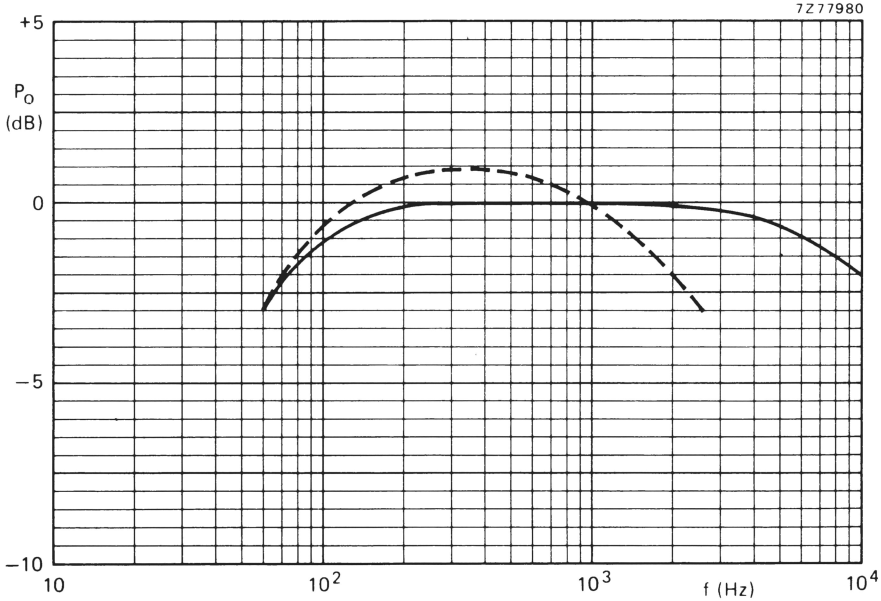


Fig. 12 Frequency characteristics of the circuit of Fig. 10; —— tone control max. high; – – – tone control min. high; $P_o$ relative to 0 dB = 3 W; typical values.

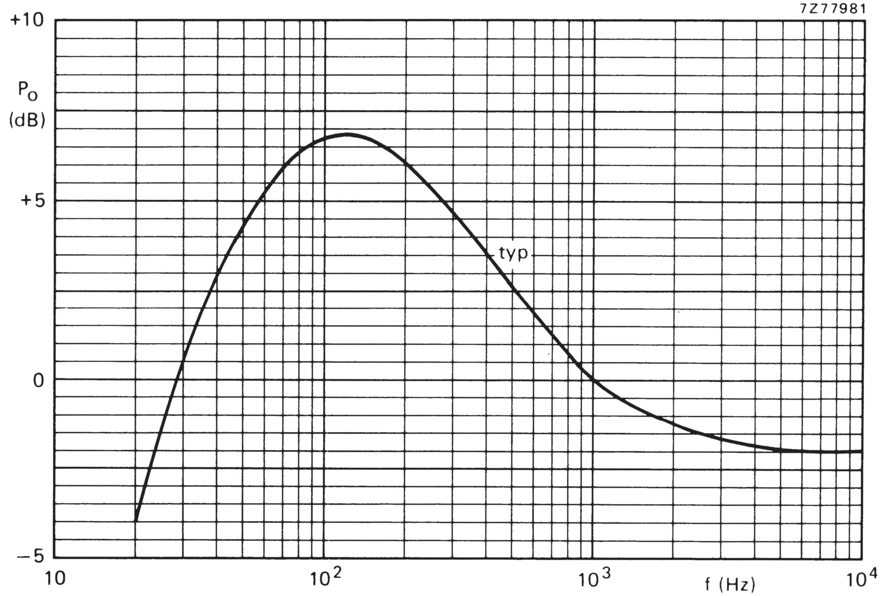


Fig. 13 Frequency characteristic of the circuit of Fig. 10; volume control at the top; tone control max. high.

# SWITCHED-MODE POWER SUPPLY DRIVE CIRCUIT

The TDA2640 is a monolithic integrated circuit for driving the switched-mode power supply of a colour or black and white television receiver.
Except for the drive and output voltage stabilizing circuitry the TDA2640 incorporates the following functions:

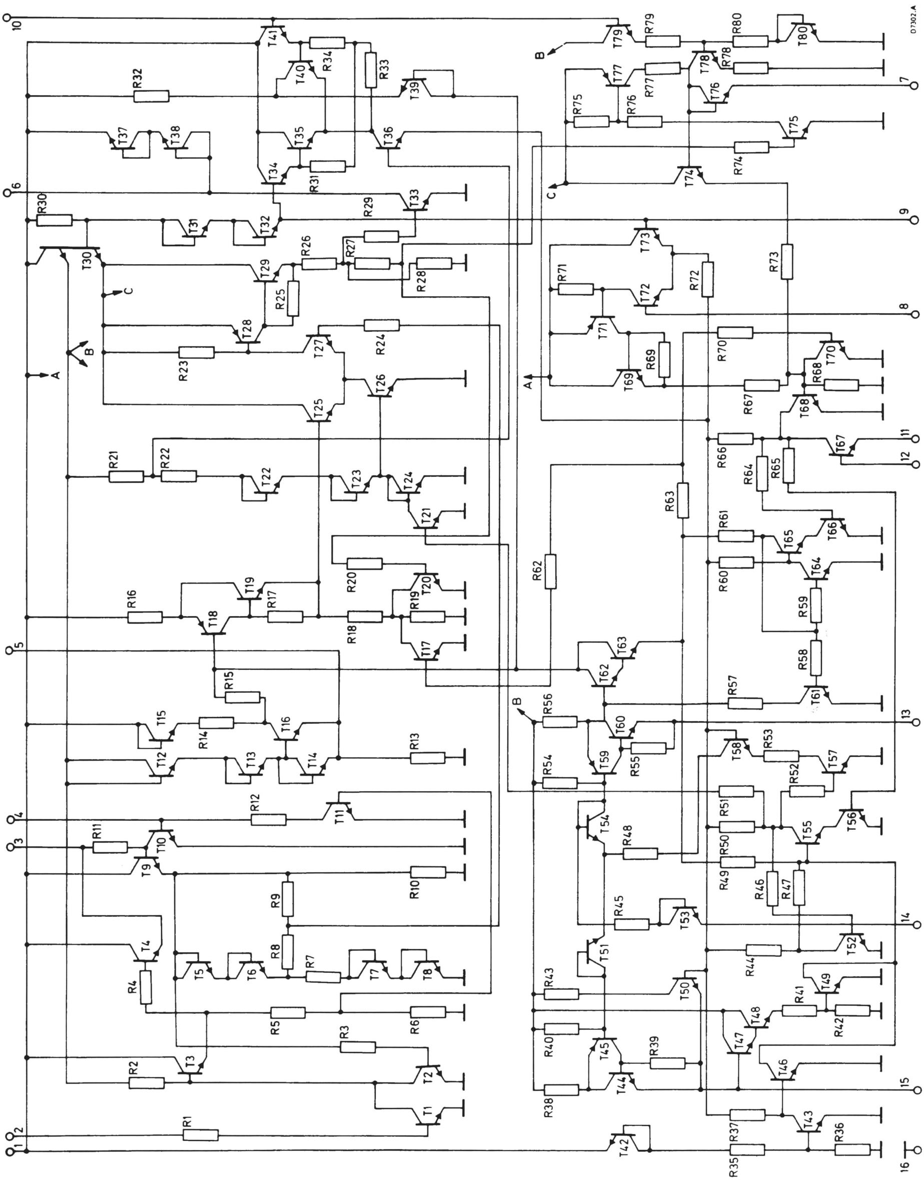
- fixed frequency determined by external components
- remote switch off and restart
- over-current protection
- over-voltage protection
- slow starting
- low supply voltage protection
- open-circuit feedback protection
- optional synchronization

| QUICK REFERENCE DATA | | | | |
|---|---|---|---|---|
| Supply voltage | $V_{1-16}$ | typ. | 12 | V |
| Supply current | $I_1$ | typ. | 8,1 | mA |
| Output voltage (peak-to-peak value) | $V_{6-16(p-p)}$ | > | 11,5 | V |
| Output current (peak value) | $I_{6M}$ | < | 20 | mA |
| Duty factor of output pulse | $\delta$ | typ. | 20 to 85 | % |
| Reference input voltage | $V_{9-16}$ | typ. | 6,2 | V |
| Sync pulse (peak-to-peak value) | $V_{2-16(p-p)}$ | | 1 to 10 | V |

**PACKAGE OUTLINES**

TDA2640 : 16-lead DIL; plastic (SOT-38).
TDA2640Q : 16-lead QIL; plastic (SOT-58).

## CIRCUIT DIAGRAM


7Z67302.A
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
A
B
C
T1
T2
T3
T4
T5
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T77
T78
T79
T80
R1
R2
R3
R4
R5
R6
R7
R8
R9
R10
R11
R12
R13
R14
R15
R16
R17
R18
R19
R20
R21
R22
R23
R24
R25
R26
R27
R28
R29
R30
R31
R32
R33
R34
R35
R36
R37
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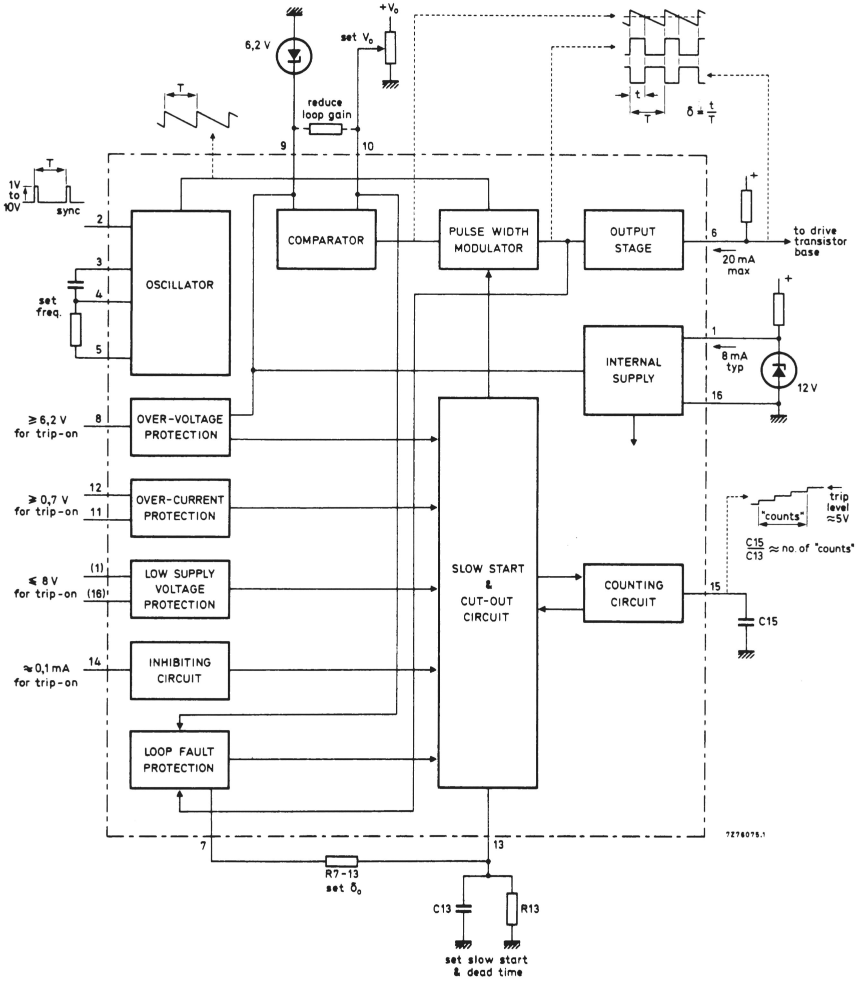
R62
R63
R64
R65
R66
R67
R68
R69
R70
R71
R72
R73
R74
R75
R76
R77
R78
R79
R80

## BLOCK DIAGRAM


6,2 V
+V$_o$
set V$_o$
reduce loop gain
9
10
T
t
$\delta = \frac{t}{T}$
1V to 10V
sync
2
3
4
5
set freq.
OSCILLATOR
COMPARATOR
PULSE WIDTH MODULATOR
OUTPUT STAGE
6
to drive transistor base
20 mA max
1
8 mA typ
INTERNAL SUPPLY
12 V
16
≥ 6,2 V for trip-on
8
OVER-VOLTAGE PROTECTION
≥ 0,7 V for trip-on
12
11
OVER-CURRENT PROTECTION
≤ 8 V for trip-on
(1)
(16)
LOW SUPPLY VOLTAGE PROTECTION
≈ 0,1 mA for trip-on
14
INHIBITING CIRCUIT
LOOP FAULT PROTECTION
SLOW START & CUT-OUT CIRCUIT
COUNTING CIRCUIT
"counts"
trip level ≈5V
$\frac{C15}{C13}$ ≈ no. of "counts"
15
C15
7Z76075.1
7
13
R7-13 set $\delta_o$
C13
R13
set slow start & dead time

**RATINGS** Limiting values in accordance with the Absolute Maximum System (IEC134)

Voltages

| | | | |
|---|---|---|---|
| Supply voltage | $V_{1-16}$ | max. | 13,8 V |
| Pin 2 | $V_{2-16}$ | | −5 to +10 V |
| Pin 8 | $V_{8-16}$ | | 0 to +10 V |
| Pin 9 | $V_{9-16}$ | | 0 to +10 V |
| Pin 10 | $V_{10-16}$ | | 0 to $V_{9-16}$ +1 V |
| Pin 9 with respect to pin 10 | $V_{9-10}$ | | −1 to +7 V |
| Pin 11 (pin 12 not connected) | $V_{11-16}$ | | −1 to 0 V |

Current

| | | | |
|---|---|---|---|
| Output current (peak value) | $I_{6M}$ | max. | 20 mA |

Power dissipation

| | | | |
|---|---|---|---|
| Total power dissipation | $P_{tot}$ | max. | 145 mW |

Temperatures

| | | | |
|---|---|---|---|
| Storage temperature | $T_{stg}$ | | −55 to +125 °C |
| Operating ambient temperature | $T_{amb}$ | | −25 to +65 °C |

**CHARACTERISTICS** at $V_{1-16} = 12$ V; $T_{amb} = 25$ °C

| | | | | |
|---|---|---|---|---|
| Supply current at $\delta = 50\%$ | $I_1$ | typ. | 8,1 mA | |
| | | | 5,1 to 10,4 mA | |
| Reference voltage | | typ. | 6,2 V | 1) |
| | | | 5,6 to 6,5 V | |
| Sync pulse (peak-to-peak value) | $V_{2-16(p-p)}$ | | 1 to 10 V | |
| Remote switch: inhibit (switched off) | $V_{14-16}$ | | 0 to 3 V | 2) |
| normal (switched on) | $V_{14-16}$ | | 5 to 12 V | |
| Over-voltage protection: threshold voltage | $V_{8-16}$ | typ. | 6,2 V | 3) |
| input current | $I_8$ | typ. | 2 µA | |
| temperature coefficient | | typ. | 0,1 mV/°C | |
| Over-current protection: threshold voltage | $V_{12-11}$ | | 660 to 760 mV | 4) |
| Low supply voltage protection: threshold voltage | $V_{1-16}$ | typ. | 8,6 V | |
| | | | 8 to 9,5 V | |
| Horizontal drive pulse (peak-to-peak value) | $V_{6-16(p-p)}$ | > | 11,5 V | 5) |
| Duty factor of output pulse: maximum | $\delta_{max}$ | > | 85 % | 6) |
| | | typ. | 90 % | |
| minimum | $\delta_{min}$ | typ. | 15 % | |
| | | < | 20 % | |

---

For notes see page 5.

## CHARACTERISTICS (continued)

| | | | |
|---|---|---|---|
| Saturation voltage of output transistor at $I_6$ = 20 mA | $V_{CEsat}$ | typ. | 280 mV |
| | | < | 400 mV |
| Feedback input impedance at pin 10 | $\lvert Z_{10-16}\rvert$ | typ. | 100 kΩ |
| Temperature coefficient for constant duty factor at pin 10 | | typ. | 0,3 mV/°C |
| Oscillator frequency spread (with fixed external components) | | < | ±3 % |
| Rise time of leading edge of output pulse | | typ. | 0,1 μs |

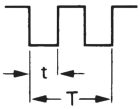
## PINNING

1. Positive supply
2. Sync pulse input
3. Oscillator timing capacitor
4. Junction of oscillator timing C and R
5. Oscillator timing resistor
6. Output
7. Low feedback protection external resistor
8. Over-voltage protection input
9. Reference input
10. Feedback voltage input
11. Over-current protection input (emitter)
12. Over-current protection input (base)
13. Slow start C and R controlling network
14. Inhibitor
15. Re-start count capacitor
16. Negative supply (ground)

Notes (from page 4)

1. Voltage obtained via an external reference diode (6,2 V).
2. Or pin 14 not connected.
3. The over-voltage protection threshold is equal to the reference voltage $V_{9-16}$ ±50 mV.
4. The temperature coefficient is typ. −1,7 mV/°C (pin 11 or pin 12 can be connected to pin 16).
5. The maximum voltage on pin 6 is limited to approximately the supply voltage (pin 1) by an internal diode.
6. Valid for normal operating conditions. The circuit starts with 0% duty factor, controlled by the switch-on circuit; the duty factor then rises to the normal operating value.

   The duty factor is specified as follows:



$$\delta = \frac{t}{T} \times 100\%.$$

## APPLICATION INFORMATION (see circuits on pages 3 and 8)

**The function is quoted against the corresponding pin number**

1. 12 V positive supply

The maximum voltage that may be applied is 13, 8 V. Where this is derived from an unstabilized supply rail, a regulator diode (12 V) should be connected between pins 1 and 16 to ensure that the maximum voltage does not exceed 13, 8 V. When the voltage on this pin falls below a minimum of 8 V the protection circuit will switch off the power supply.

2. Sync pulse input

The switching repetition rate may be synchronized to a source of positive-going sync pulses between 1 and 10 V. The free-running frequency of the TDA2640 oscillator must be above the synchronized frequency.
The minimum duration of the sync pulses is the difference between the period of the oscillator pulses and the period of the sync pulses. Synchronization reduces the maximum obtainable duty factor. If synchronization is not required, connect pin 2 to pin 16.

3, 4 and 5. Oscillator timing network

The timing network consists of a capacitor connected between pins 3 and 4, and a resistor connected between pins 4 and 5. The value of these components determines the switching period of the SMPS drive pulses.

6. Output

An external resistor connected between this pin and the supply rail determines the base drive current for the drive transistor. The integrated output circuit consists of an n-p-n transistor with a catching diode connected between its collector and an internal 12 V supply. This provides a low impedance in the "ON" state, that is with the drive transistor turned off.

7. Low feedback protection

An external resistor connected between this pin and pin 13 determines the maximum obtainable duty factor for the output pulses if the feedback voltage (pin 10) remains below the specified limit during starting.

8. Over-voltage protection

A voltage that is proportional to the power supply output voltage can be connected to this pin to operate a protection circuit if a threshold level is exceeded. The threshold level is determined by the external voltage reference diode connected to pin 9 (6, 2 V nominal). If over-voltage protection is not required, pin 8 should be connected to pin 16.

9. Reference input

An external voltage reference diode (6, 2 V nominal) must be connected between this pin and pin 16. The stability of the reference source determines the overall stability of the power supply output voltage. The voltage reference diode current is derived from within the integrated circuit; it has a typical value of 0, 8 mA.

**APPLICATION INFORMATION** (continued)

10. Feedback voltage input

The control loop input is applied to pin 10. This pin is internally connected to one input of a differential error amplifier, functioning as an amplitude comparator, the other input of which is connected to the reference source on pin 9. Under normal operating conditions with the comparator at balance, the voltage on pin 10 will be about equal to the reference voltage on pin 9 (6,2 V), and the d.c. feedback factor of the external network should be designed for this value.

11 and 12. Over-current protection

A voltage proportional to the output current of the SMPS is applied to these pins. Pin 11 is connected to the emitter of an internal n-p-n detection transistor; pin 12 is connected to its base. Either of these pins may be grounded (pin 16) depending on the polarity of the input during increasing current. For example, if pin 11 is grounded the trip level on pin 12 is 660 mV to 760 mV; if pin 12 is grounded, the trip level on pin 11 is −660 mV to −760 mV.

13. Slow start

A resistor and capacitor in parallel must be connected between this pin and pin 16 (1 µF and 390 kΩ). This network controls the rate at which the duty factor of the SMPS drive pulses increases to its normal operating value after switch-on. This minimizes inrush current. The network also influences the repetition period of the slow start during a fault.

14. Inhibitor

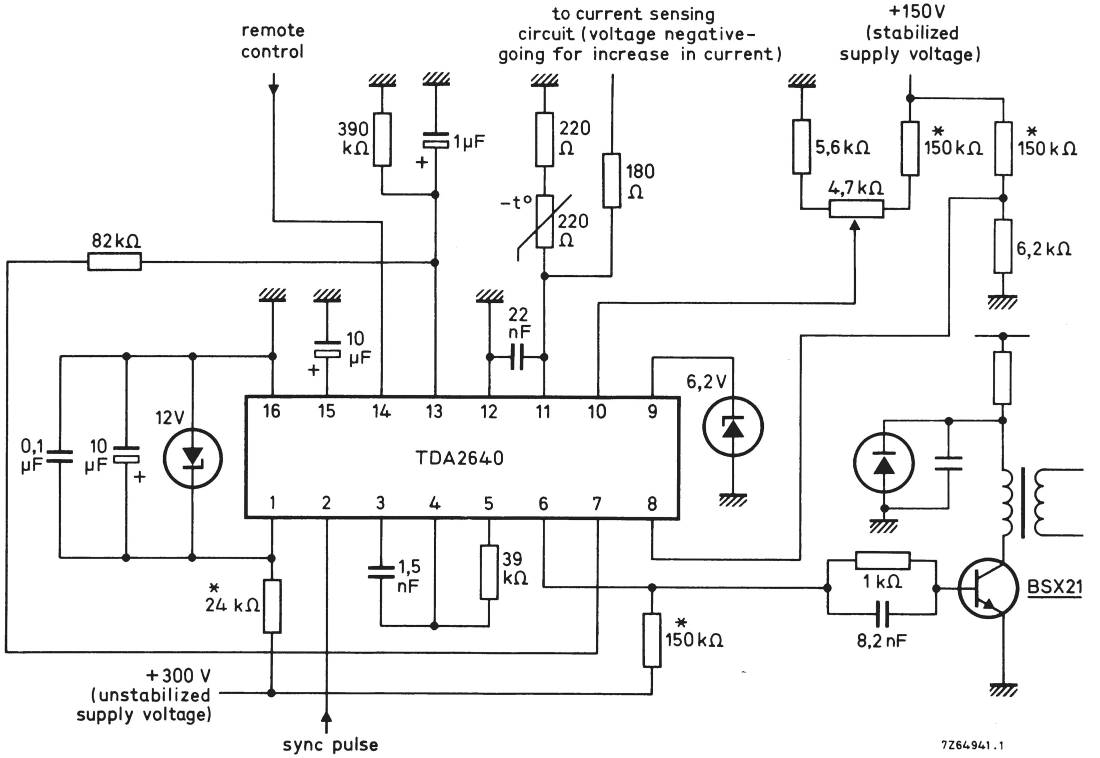
The power supply is switched off if the voltage on this pin is between 0 V and 3 V ($-I_{14} > 0,1$ mA). The power supply is switched on if this pin is not connected, or is connected to a voltage of between 5 V and the 12 V supply. The slow start and protection circuits remain operative under both conditions.

15. Re-start count capacitor

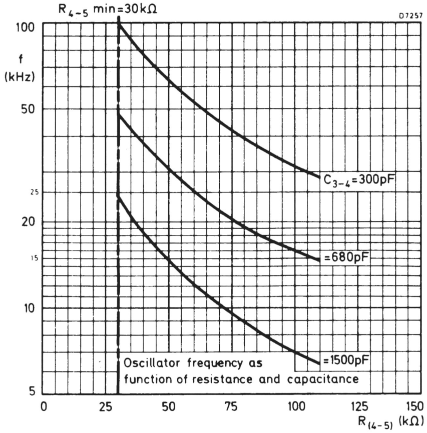
An external capacitor (C15 = 10 µF) should be connected between pins 15 and 16. This capacitor controls the characteristics of the protection circuits as follows. When the protection circuit operates due to a fault, the duty factor of the drive pulses is reduced to zero. After an interval determined by the time-constant of the circuit connected to pin 13, the duty factor of the pulses slowly increases toward its normal operating value. If the fault persists, the duty factor of the pulses is again reduced to zero and the protection cycle is repeated. The number of times that the cycle is repeated before the power supply drive pulses are permanently discontinued is determined by the value of the capacitor connected to pin 15. The number of counts is roughly C15/C13.

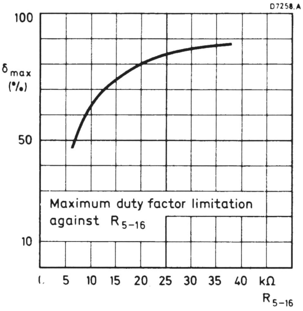
16. Negative supply (ground)

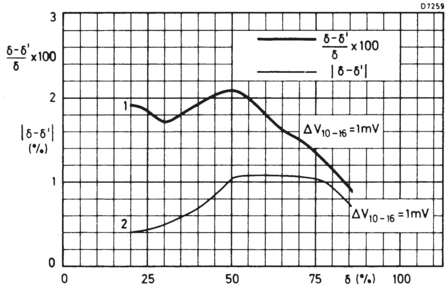
APPLICATION INFORMATION (continued)


remote control
to current sensing circuit (voltage negative-going for increase in current)
+150 V (stabilized supply voltage)
390 kΩ
1 μF
220 Ω
180 Ω
-t°
220 Ω
5,6 kΩ
4,7 kΩ
* 150 kΩ
* 150 kΩ
6,2 kΩ
82 kΩ
10 μF
22 nF
6,2 V
16
15
14
13
12
11
10
9
TDA2640
1
2
3
4
5
6
7
8
0,1 μF
10 μF
12V
* 24 kΩ
1,5 nF
39 kΩ
* 150 kΩ
1 kΩ
8,2 nF
BSX21
+300 V (unstabilized supply voltage)
sync pulse
7Z64941.1

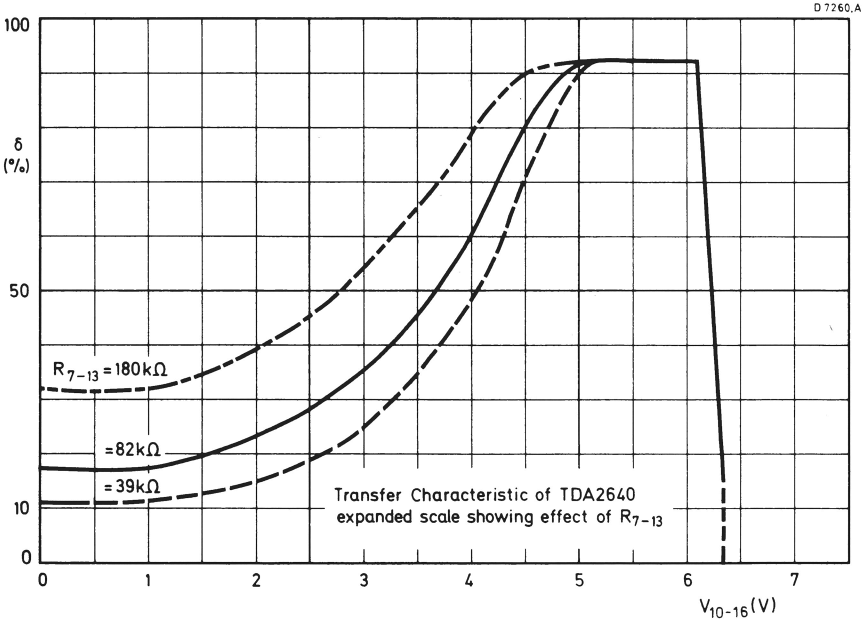
Note: To operate with other supply and output voltages, alternative values of resistors marked thus * must be chosen.



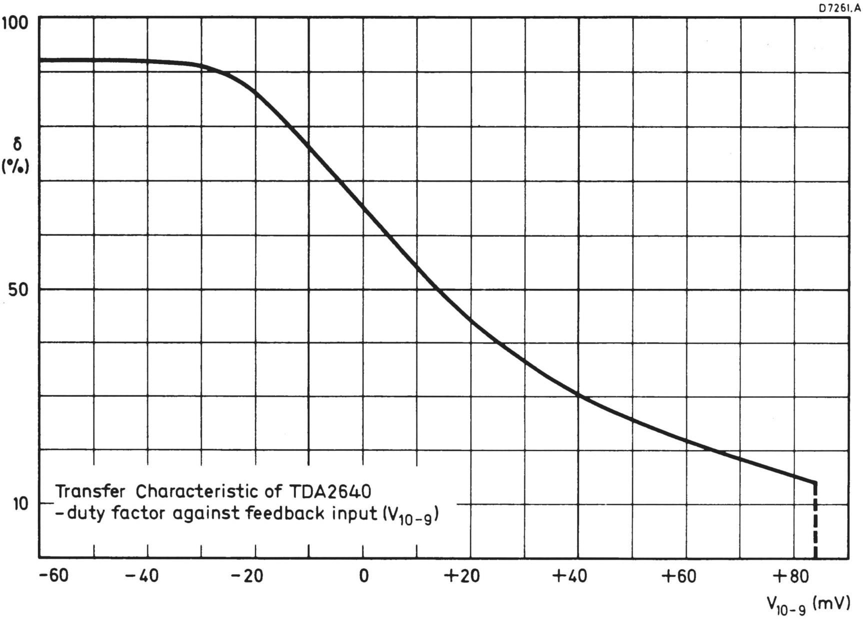




1. Change of transfer characteristic against duty factor for $\Delta V_{10-16} = 1$ mV.
2. Percentage change of transfer characteristics against duty factor for $\Delta V_{10-16} = 1$ mV.



Transfer Characteristic of TDA2640 expanded scale showing effect of R$_{7-13}$



Transfer Characteristic of TDA2640 – duty factor against feedback input (V$_{10-9}$)

# VERTICAL DEFLECTION CIRCUIT

The TDA2652 is a monolithic integrated circuit for colour television receivers with 110° deflection. With an external circuit it can be used in 20AX and 30AX systems. The circuit incorporates the following functions:

- Synchronization circuit
- Vertical oscillator
- Blanking pulse generator
- Sawtooth generator with buffer stage
- Preamplifier
- Driver and output stage
- Short-circuit and thermal protection
- Guard circuit
- Voltage stabilizer

## QUICK REFERENCE DATA

| | | | | |
|---|---|---|---|---|
| Supply voltage range | $V_P$ | | 15 to 35 | V |
| Output current (peak-to-peak value) | $I_{9(p-p)}$ | max. | 4 | A |
| Total power dissipation | $P_{tot}$ | max. | 10 | W |
| Operating junction temperature | $T_j$ | max. | 150 | °C |
| Thermal resistance from junction to copper heat spreader (tab) | $R_{th\ j\text{-}tab}$ | = | 3 | K/W |

## PACKAGE OUTLINE

16-lead DIL; plastic power (SOT-69C).

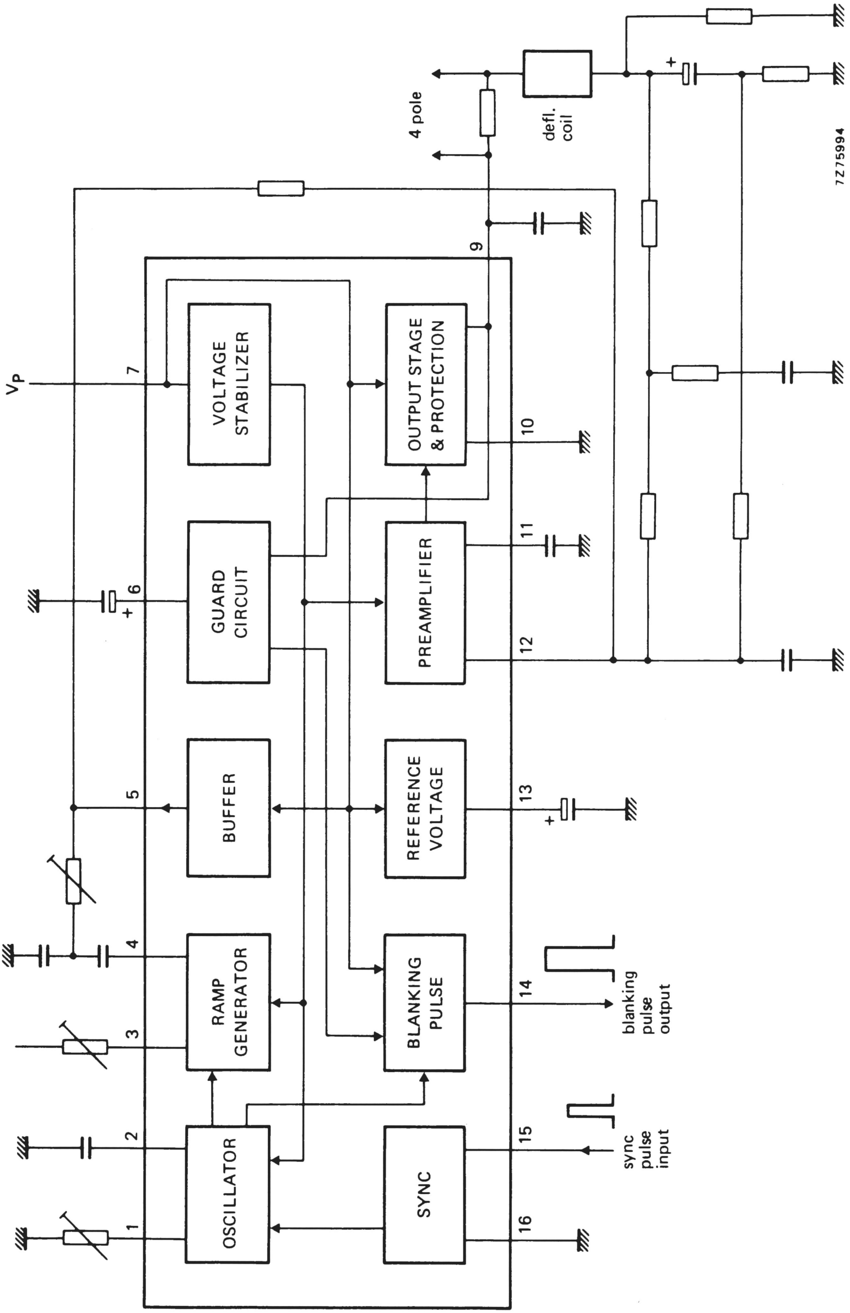

VP
7
VOLTAGE STABILIZER
OUTPUT STAGE & PROTECTION
9
10
4 pole
defl. coil
7Z75994
6
GUARD CIRCUIT
PREAMPLIFIER
11
12
5
BUFFER
REFERENCE VOLTAGE
13
4
3
RAMP GENERATOR
BLANKING PULSE
14
blanking pulse output
2
1
OSCILLATOR
SYNC
15
16
sync pulse input

Fig. 1 Block diagram.

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages

| | | | | |
|---|---|---|---|---|
| Pin 2 | $V_{2-16}$ | max. | 8 | V |
| Pin 4 | $V_{4-16}$ | max. | 50 | V |
| Pin 7 (supply voltage) | $V_{7-16}$ ($V_P$) | max. | 50 | V |
| Pin 9 | $V_{9-16}$ | max. | 50 | V |
| Pin 11 | $V_{11-16}$ | max. | 50 | V |
| Pin 12 | $V_{12-16}$ | max. | 12 | V |
| Pin 13 | $V_{13-16}$ | max. | 50 | V |
| Pin 15 | $V_{15-16}$ | max. | 12 | V |

Currents

| | | | | |
|---|---|---|---|---|
| Pin 1 | $-I_1$ | max. | 1 | mA |
| Pin 3 | $I_3$ | max. | 1 | mA |
| Pin 5 | $I_5$ | max. | 5 | mA |
| Pin 6 | $I_6$ | max. | 1 | mA |
| Pin 7, 9, 10 | Internally limited by short-circuit protection | | | |
| Pin 14 | $\pm I_{14}$ | max. | 15 | mA |

Total power dissipation internally limited by the thermal protection circuit.

| | | | | |
|---|---|---|---|---|
| Storage temperature | $T_{stg}$ | | −25 to + 150 | °C |
| Operating junction temperature | $T_j$ | max. | 150 | °C |

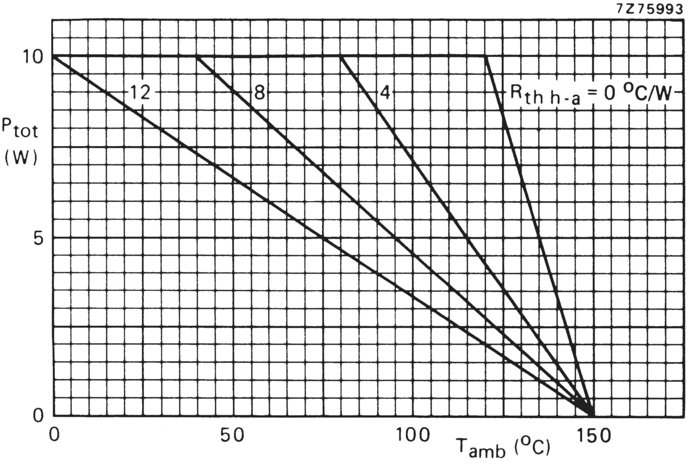


Fig. 2 Total power dissipation. $R_{th\ h\text{-}a}$ includes the $R_{th\ tab\text{-}h}$ which is expected when heatsink compound is used. $R_{th\ j\text{-}tab}$ = 3 °C/W.

## CHARACTERISTICS

$T_{amb}$ = 25 °C unless otherwise specified

| | | | | |
|---|---|---|---|---|
| Supply voltage | $V_P = V_{7\text{-}16}$ | | 15 to 35 | V |
| Input voltage<br>$V_P$ = 30,5 V | $V_{12\text{-}16}$ | typ. | 2,07<br>2,01 to 2,13 | V<br>V |
| Input current<br>$V_P$ = 30,5 V | $I_{12}$ | typ. | 1 | μA |
| Blanking pulse duration<br>synchronized at 50 Hz | $t_p$ | typ. | 1,4<br>1,33 to 1,47 | ms<br>ms |
| Blanking pulse current | $\pm I_{14}$ | typ. | 12 | mA |
| Blanking pulse generator output voltage<br>$\pm I_{14}$ = 10 mA | $V_{7\text{-}14}$ | typ. | 1 | V |
| | $V_{14\text{-}16}$ | typ. | 1 | V |
| Oscillator voltage (d.c.) | $V_{1\text{-}16}$ | typ. | 9 | V |
| Sawtooth generator output voltage | $V_{5\text{-}16}$ | | 1 to $V_P$–0,5 | V |
| Sync pulse amplitude | $V_{15\text{-}16}$ | | 1 to 12 | V |
| Oscillator temperature dependency<br>$T_{case}$ = 20 to 100 °C | $(\Delta f/f)/\Delta T$ | typ. | 0,0001 | $^{o}C^{-1}$ |
| Oscillator voltage dependency<br>$V_P$ = 15 to 35 V | $(\Delta f/f)/\Delta V_P$ | typ. | 0,0004 | $V^{-1}$ |
| Junction temperature<br>switching point thermal protection | $T_j$ | typ. | 150<br>142 to 158 | °C<br>°C |
| Synchronization range | | typ. | 15 | % |
| Output voltage<br>$-I_9$ = 2 A | $V_{9\text{-}16}$ | | $V_P$–2,3 to $V_P$–2,6 | V |
| $I_9$ = 2 A | $V_{9\text{-}16}$ | | 2,3 to 2,6 | V |
| Output current | $I_9$ | $\leq$ | 2 | A |

## PINNING

1. Oscillator adjustment
2. Oscillator capacitor
3. Amplitude adjustment
4. Sawtooth capacitors
5. Output ramp oscillator
6. Guard circuit
7. Positive supply
8. n.c.
9. Output
10. Ground
11. Preamplifier
12. Preamplifier input
13. Reference voltage stage
14. Blanking output
15. Synchronization input
16. Ground.

## APPLICATION INFORMATION

**The function is described against the corresponding pin number**

1.2. Oscillator
The frequency of the oscillator is determined by a potentiometer at pin 1 and a capacitor at pin 2.

3.4. Sawtooth generator
The timing of the ramp generator is determined by a potentiometer at pin 3 and a capacitor at pin 4. This capacitor has been split to realize linearity control.

5. Output ramp oscillator
This pin delivers a ramp signal which is used for linearity control, and drive of the preamplifier. The ramp signal is applied via a shaping network to pin 4 (linearity) and via a resistor to pin 12 (preamplifier).

6. Guard circuit input
When a capacitor is connected between this pin and ground a continuous blanking signal is available at pin 14 in case of missing vertical deflection current.
When no continuous blanking is required this capacitor is replaced by a resistor between pin 6 and pin 7.

7. Positive supply
No voltage stabilizer is necessary resulting in optimum tracking with line deflection. The internal stabilizer delivers the voltage for the oscillator, ramp generator and preamplifier.

8. Not connected.

9. Output of class B power stage
The deflection coil is connected to this pin, via a four-pole network, a coupling capacitor and a feedback resistor, to ground.

10. Ground for output stage.

11. Preamplifier
The cut-off frequency of the internal differential amplifier (preamplifier) is adjusted with the capacitor between pin 11 and ground.

12. Preamplifier input
The d.c. voltage is proportional to the output voltage (d.c. feedback). The a.c. voltage is proportional to the sum of the ramp voltage at pin 5 and the voltage, with opposite polarity, at the feedback resistor (a.c. feedback).

13. Reference voltage stage
The bias stage of the preamplifier is decoupled at this pin.

14. Blanking output
The maximum pulse amplitude with no load is $V_P$. When $I_{14}$ is 10 mA the amplitude of the pulse is 1 V.

15. Synchronization input
The oscillator has to be synchronized by a positive-going pulse of between 1 and 12 V.

16. Ground of small signal part.

**APPLICATION INFORMATION** (continued)

| | | | 20AX (Fig. 3) | 30AX (Fig. 4) |
|---|---|---|---|---|
| Supply voltage | $V_S$ | typ. | 33 V | 35 V |
| Output voltage (d.c.) | $V_{9\text{-}16}$ | typ. | 17 V | 16 V |
| Output voltage (peak value) | $V_{9\text{-}16}$ | typ. | 36 V | 43 V |
| Supply current | $I_7$ | typ. | 500 mA | 290 mA |
| Deflection current (peak-to-peak value) | $I_{(p\text{-}p)}$ | typ. | 3,6 A | 2,1 A |
| Output current (peak-to-peak value) | $\pm I_{9(p\text{-}p)}$ | typ. | 1,9 A | 1,1 A |
| Flyback time | $t_{fl}$ | typ. | 0,85 ms | 1,2 ms |
| Total power dissipation in I.C. | $P_{tot}$ | typ. | 8,5 W * | 4 W ** |
| Blanking time | $t_b$ | typ. | 1,4 ms | 1,4 ms |
| Non-linearity | | < | 3 % | 3 % |

* For 20AX systems the heatsink has to be constructed for $P_{tot} < 10$ W, $R_{th\ h\text{-}a} = 4\ ^{o}C/W$ at $T_{amb} = 60\ ^{o}C$.

** For 30AX systems the heatsink has to be constructed for $P_{tot} < 5$ W, $R_{th\ h\text{-}a} = 8{,}5\ ^{o}C/W$ at $T_{amb} = 60\ ^{o}C$.

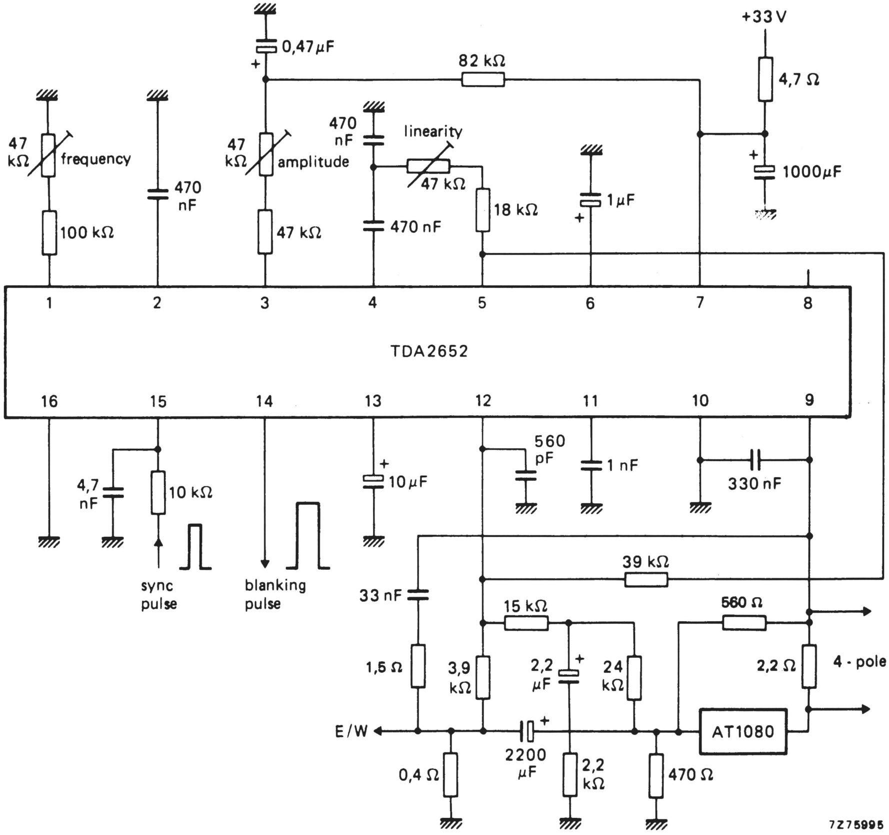

+33 V
4,7 Ω
1000 μF
82 kΩ
0,47 μF
47 kΩ
frequency
100 kΩ
470 nF
47 kΩ
amplitude
47 kΩ
470 nF
linearity
47 kΩ
470 nF
18 kΩ
1 μF
TDA2652
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
4,7 nF
10 kΩ
sync pulse
blanking pulse
10 μF
560 pF
1 nF
330 nF
33 nF
39 kΩ
15 kΩ
560 Ω
1,5 Ω
3,9 kΩ
2,2 μF
24 kΩ
2,2 Ω
4 - pole
E/W
2200 μF
AT1080
0,4 Ω
2,2 kΩ
470 Ω
7Z75995

Fig. 3 Complete vertical deflection circuit for 20AX.

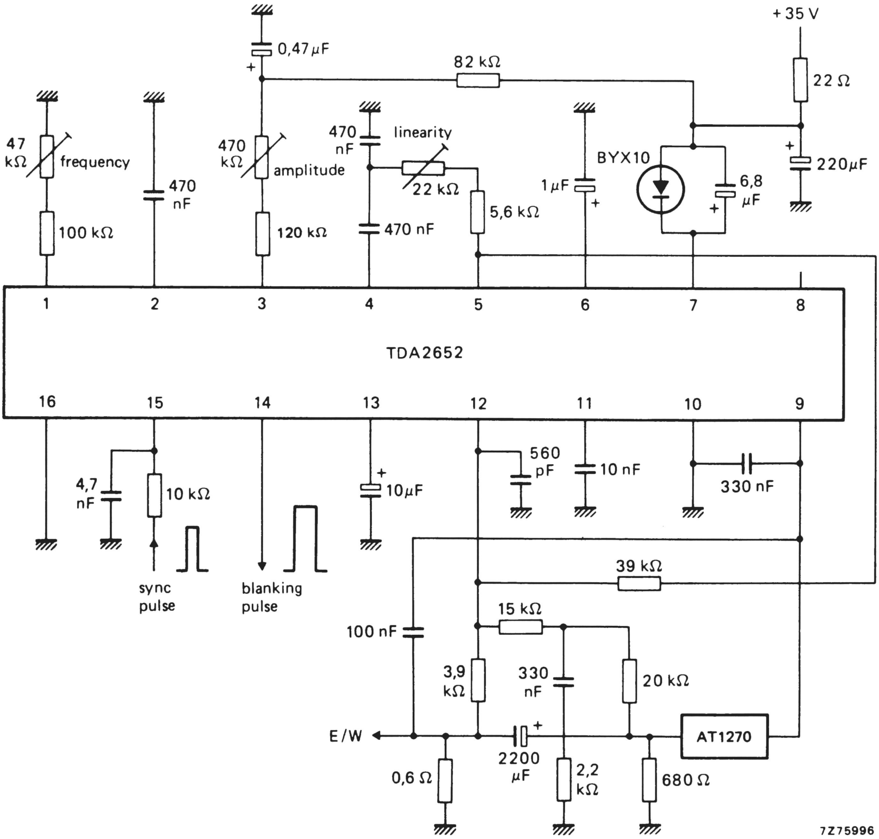

+35 V
22 Ω
220µF
0,47µF
82 kΩ
47 kΩ
frequency
100 kΩ
470 nF
470 kΩ
amplitude
120 kΩ
470 nF
linearity
22 kΩ
470 nF
5,6 kΩ
1µF
BYX10
6,8 µF
TDA2652
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
4,7 nF
10 kΩ
sync pulse
blanking pulse
10µF
560 pF
10 nF
330 nF
39 kΩ
100 nF
15 kΩ
3,9 kΩ
330 nF
20 kΩ
E/W
AT1270
0,6 Ω
2200 µF
2,2 kΩ
680 Ω
7Z75996

Fig. 4 Complete vertical deflection circuit for 30AX.

# VERTICAL DEFLECTION CIRCUIT

The TDA2653 is a monolithic integrated circuit for vertical deflection in large screen colour television receivers, e.g. 30AX and PIL-S4 systems.

The circuit incorporates the following functions:

- Oscillator.
- Synchronization circuit.
- Blanking pulse generator with guard circuit.
- Frequency detector and storage.
- Sawtooth generator with amplitude switch for 50 Hz/60 Hz.
- Buffer stage.
- Reference voltage unit.
- Preamplifier.
- Output stage with thermal and short-circuit protection.
- Flyback generator.
- Voltage stabilizer.

## QUICK REFERENCE DATA

| | | | | |
|---|---|---|---|---|
| For 30AX system | | | | |
| Supply voltage | $V_S$ | typ. | 26 | V |
| Supply current | $I_S$ | typ. | 325 | mA |
| Output current (peak-to-peak value) | $I_{9(p\text{-}p)}$ | typ. | 2,2 | A |
| Frequency frequency | f | | 50 | Hz/60 Hz |
| Sync input pulse (peak-to-peak value) | $V_{15\text{-}16(p\text{-}p)}$ | $>$ | 1 | V |

## PACKAGE OUTLINE

16-lead DIL; plastic power (SOT-69C).

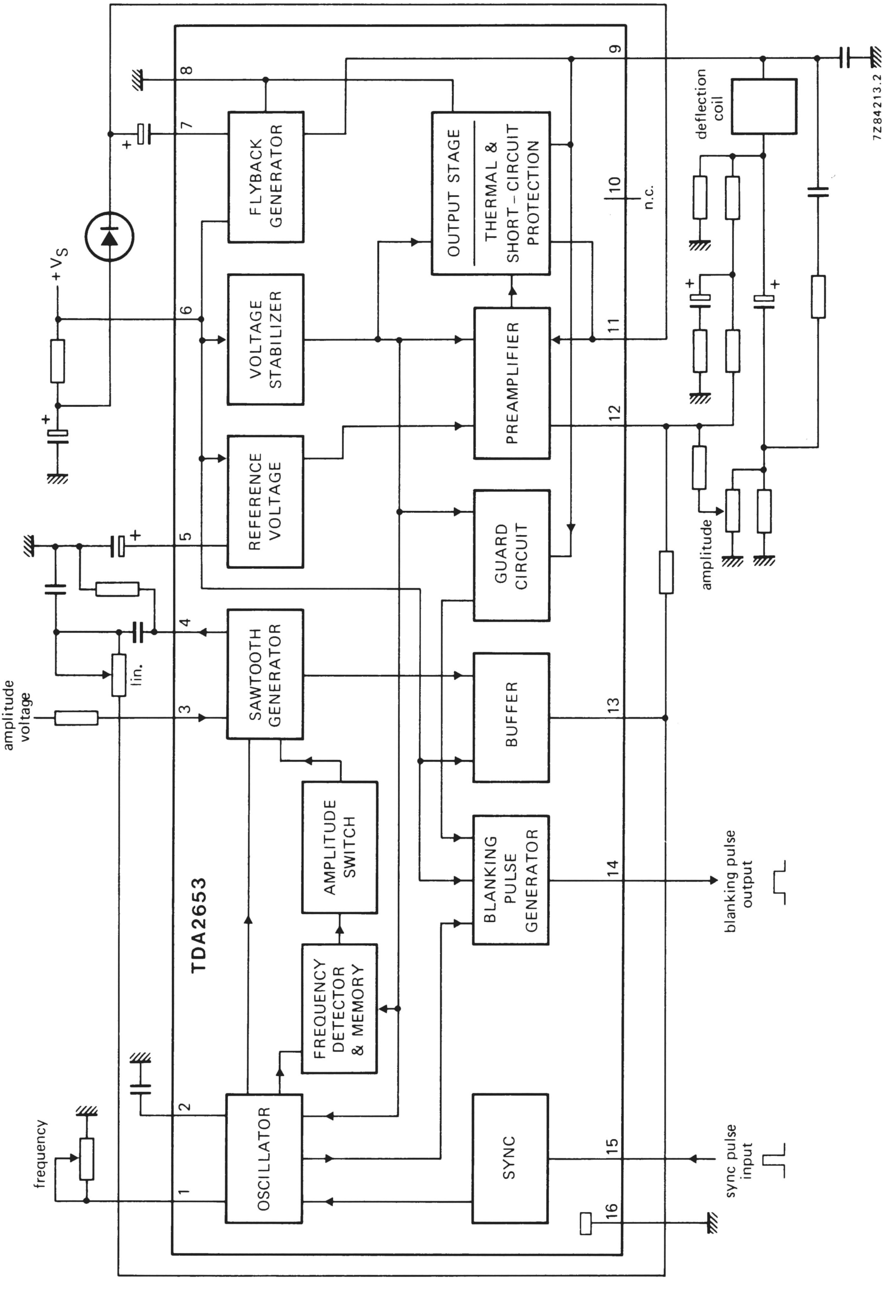

TDA2653
OSCILLATOR
FREQUENCY DETECTOR & MEMORY
AMPLITUDE SWITCH
SAWTOOTH GENERATOR
REFERENCE VOLTAGE
VOLTAGE STABILIZER
FLYBACK GENERATOR
SYNC
BLANKING PULSE GENERATOR
BUFFER
GUARD CIRCUIT
PREAMPLIFIER
OUTPUT STAGE
THERMAL & SHORT-CIRCUIT PROTECTION
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
n.c.
+V<sub>S</sub>
+
frequency
amplitude voltage
lin.
amplitude
deflection coil
blanking pulse output
sync pulse input
7Z84213.2

Fig. 1 Block diagram.

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | |
|---|---|---|---|
| Supply voltage (pin 6) | $V_{6\text{-}16} = V_S$ | max. | 40 V |
| Supply voltage output stage (pin 11) | $V_{11\text{-}16}$ | max. | 58 V |
| Voltages | | | |
| Pin 2 | $V_{2\text{-}16}$ | max. | 7 V |
| Pins 5 and 7 | $V_{5;7\text{-}16}$ | max. | 40 V |
| Pin 9 | $V_{9\text{-}16}$<br>$-V_{9\text{-}16}$ | max.<br>max. | 58 V<br>0 V |
| Pin 12 | $V_{12\text{-}16}$ | max. | 12 V |
| Pin 15 | $V_{15\text{-}16}$ | max. | 30 V |
| Currents | | | |
| Pin 1 | $I_1$<br>$-I_1$ | max.<br>max. | 0 mA<br>1 mA |
| Pin 3 | $I_3$<br>$-I_3$ | max.<br>max. | 1 mA<br>0 mA |
| Pin 4 | $I_4$<br>$-I_4$ | max.<br>max. | 50 mA<br>1 mA |
| Pin 7 | $I_7$<br>$-I_7$ | max.<br>max. | 1,2 A<br>1,5 A |
| Pin 13 | $I_{13}$<br>$-I_{13}$ | max.<br>max. | 5 mA<br>2 mA |
| Pin 14 | $\pm I_{14}$ | max. | 15 mA |

Pins 8, 9 and 11: internally limited by the short-circuit protection circuit.

Total power dissipation: internally limited by the thermal protection circuit (see Fig. 2).

| | | |
|---|---|---|
| Storage temperature range | $T_{stg}$ | −20 to +150 °C |
| Operating ambient temperature range (see Fig. 2) | $T_{amb}$ | − 20 °C to limiting value |

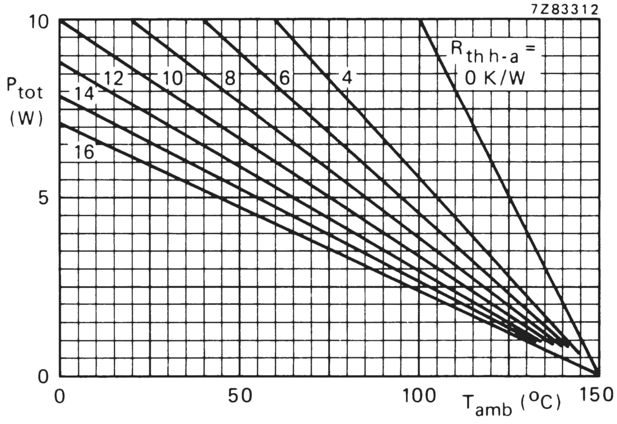


Fig. 2 Total power dissipation. $R_{th\ h\text{-}a}$ includes $R_{th\ mb\text{-}h}$ which is expected when heat-sink compound is used. $R_{th\ j\text{-}mb} \leqslant 5$ K/W.

## CHARACTERISTICS

$T_{amb}$ = 25 °C unless otherwise specified.

### Supply voltage/output stage

| | | | | |
|---|---|---|---|---|
| Supply voltage | $V_{6-16} = V_S$ | | 9 to 30 | V |
| Output voltage | | | | |
| at $-I_9$ = 1,1 A | $V_{9-16}$ | ⩾ | $V_{11-16} - 2,2$ | V |
| | | typ. | $V_{11-16} - 1,9$ | V |
| at $I_9$ = 1,1 A | $V_{9-16}$ | typ. | 1,3 | V |
| | | ⩽ | 1,6 | V |
| Flyback generator output voltage at $-I_9$ = 1,1 A | $V_{7-16}$ | typ. | $V_S - 2,2$ | V |
| Peak output current | $\pm I_9$ | typ. | 1,2 | A |
| Flyback generator peak current | $\pm I_7$ | typ. | 1,2 | A |

### Feedback

| | | | | |
|---|---|---|---|---|
| D.C. voltage level of preamplifier at $V_S$ = 26 V | $V_{12-16}$ | typ. | 2,03 | V |
| | | | 1,97 to 2,09 | V |
| Input quiescent current of preamplifier | $-I_{12}$ | typ. | 0,1 | μA |

### Synchronization

| | | | | |
|---|---|---|---|---|
| Sync input pulse | $V_{15-16}$ | | 1 to 12 | V |
| Tracking range | | typ. | 28 | % |

### Oscillator/sawtooth generator

| | | | | |
|---|---|---|---|---|
| Oscillator frequency control input voltage | $V_{1-16}$ | | 6 to 9 | V |
| Sawtooth generator output voltage | $V_{13-16}$ | | 1,2 to $V_S - 0,5$ | V |
| Sawtooth generator output current | | | | |
| synchronized at 50 Hz | $I_4$ | typ. | 50 | μA |
| synchronized at 60 Hz | $I_4$ | typ. | 60 | μA |
| Oscillator temperature dependency $T_{case}$ = 20 to 100 °C | $(\Delta f/f)/\Delta T_{case}$ | typ. | $10^{-4}$ | $K^{-1}$ |
| Oscillator voltage dependency $V_S$ = 10 to 30 V | $(\Delta f/f)/\Delta V_S$ | typ. | $4 \times 10^{-4}$ | $V^{-1}$ |

### Blanking pulse generator

| | | | | |
|---|---|---|---|---|
| Output voltage | | | | |
| at $I_{14}$ = 10 mA | $V_{14-16}$ | typ. | 6 | V |
| at $-I_{14}$ = 10 mA | $V_{6-14}$ | typ. | 6 | V |
| Output current | $\pm I_{14}$ | ⩽ | 12 | mA |
| Blanking pulse duration at 50 Hz sync | $t_b$ | typ. | 1,4 ± 0,07 | ms |

### Thermal resistance/junction temperature

| | | | | |
|---|---|---|---|---|
| From junction to copper heat spreader (mounting base) | $R_{th\ j-mb}$ | ⩽ | 5 | K/W |
| Junction temperature; switching point thermal protection | $T_j$ | typ. | 150 ± 8 | °C |

## PINNING

1. Oscillator adjustment
2. Oscillator capacitor
3. Amplitude adjustment
4. Sawtooth capacitor
5. Reference voltage decoupling
6. Positive supply ($V_S$)
7. Flyback generator output
8. Negative supply (ground) of output stage
9. Output
10. n.c. (not connected)
11. Positive supply of output stage
12. Preamplifier input
13. Output of sawtooth buffer stage
14. Blanking output
15. Synchronization input
16. Negative supply (ground) of small signal part

## APPLICATION INFORMATION

**The function is described against the corresponding pin number**

1. 2. Oscillator

The oscillator frequency is determined by a potentiometer at pin 1 and a capacitor at pin 2.

3. 4. Sawtooth generator

The amplitude of the sawtooth generator is determined by two resistors at pin 3 and a capacitor at pin 4. This capacitor has been split to realize linearity control.

5. Reference voltage decoupling

An electrolytic capacitor connected from this pin to ground, suppresses the ripple voltage on the supply voltage, from which, via an internal resistor divider the reference voltage is derived.

6. Positive supply

The supply voltage at this pin is used to supply the flyback generator, the voltage stabilizer, reference voltage unit, buffer stage and blanking pulse generator.

7. Flyback generator output

An electrolytic capacitor has to be connected between pins 7 and 11 to complete the flyback generator.

8. Negative supply (ground) of output stage

9. Output of class-B power stage

The vertical deflection coil is connected to this pin, via a series connection of a coupling capacitor and a feedback resistor, to ground.

10. Not connected

11. Positive supply of output stage

This supply is obtained from the flyback generator. An electrolytic capacitor between pins 11 and 7, and a diode between pins 6 and 11 have to be connected for proper operation of the flyback generator.

12. Preamplifier input

The d.c. voltage is proportional to the output voltage (d.c. feedback). The a.c. voltage is proportional to the sum of the buffered sawtooth voltage at pin 13 and the voltage, with opposite polarity, at the feedback resistor (a.c. feedback).

13. Output of sawtooth buffer stage

The sawtooth signal is fed via a buffer stage to pin 13. It delivers the signal which is used for linearity control, and drive of the preamplifier. The sawtooth is applied via a shaping network to pin 4 (linearity) and via a resistor to pin 12 (preamplifier).

**APPLICATION INFORMATION** (continued)

14. Blanking output

    The maximum pulse amplitude with no load is $V_S$. When $I_{14}$ is 10 mA the amplitude of the pulse is 6 V.

15. Synchronization input

    The oscillator has to be synchronized by a positive-going pulse between 1 and 12 V. The integrated frequency detector, with storage and amplitude switch, takes care of automatic recognition and processing of 50 Hz or 60 Hz signals.

16. Negative supply (ground) of small signal part.

The following application data are measured in Fig. 3.

| | | | 30AX system | PIL-S4 system | |
|---|---|---|---|---|---|
| System supply voltage | $V_S$ | typ. | 26 | 26 | V |
| Output voltage (d.c. value) | $V_{9\text{-}16}$ | typ. | 14 | 13,5 | V |
| Output voltage (peak value) | $V_{9\text{-}16}$ | typ. | 42 | 49 | V |
| Supply current (pin 6 + pin 11) | $I_6 + I_{11}$ | typ. | 325 | 195 | mA |
| Deflection current (peak-to-peak value) | $I_{9(p\text{-}p)}$ | typ. | 2,2 | 1,32 | A |
| Flyback time | $t_{fl}$ | typ. | 0,85 | 1,1 | ms |
| Blanking time | $t_b$ | typ. | 1,46 | – | ms |
| Total power dissipation per package | $P_{tot}$ | typ. | 4,2 | 3 | W |
| Total power consumption | $P$ | typ. | 8,1 | – | W |
| Thermal resistance of heatsink | $R_{th\ h\text{-}a}$ | typ. | 10 | 10 | K/W |

---

* Including 6% overscan.

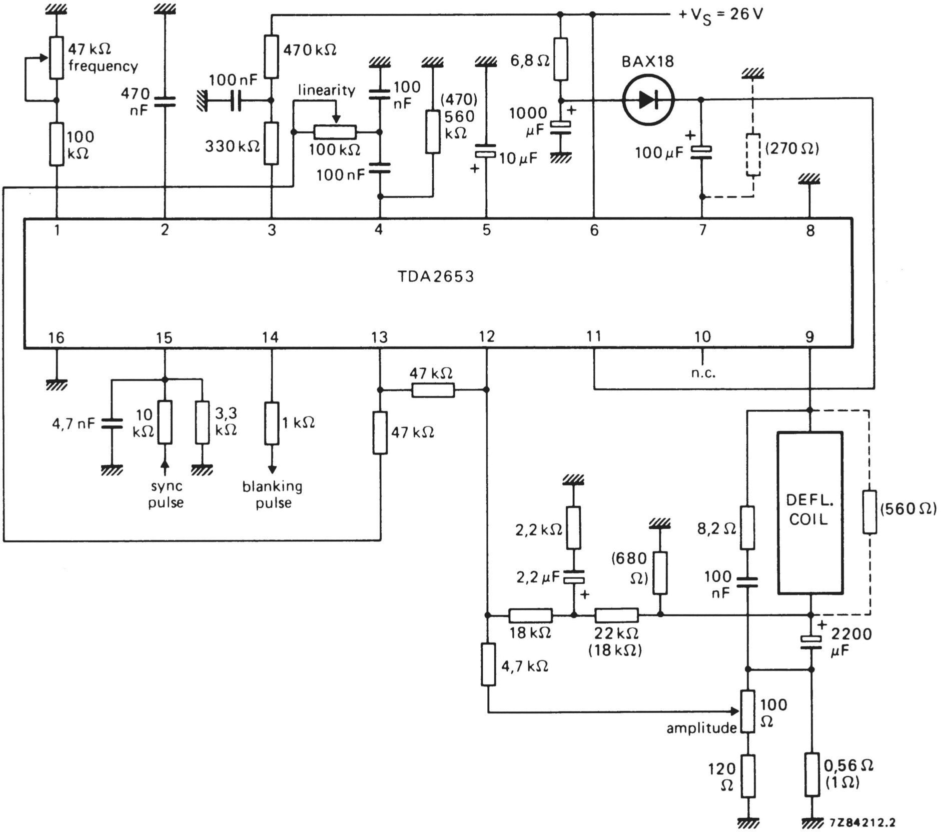

+V_S = 26 V
47 kΩ
frequency
100 kΩ
470 nF
100 nF
470 kΩ
330 kΩ
linearity
100 kΩ
100 nF
100 nF
(470)
560 kΩ
10 µF
6,8 Ω
1000 µF
BAX18
100 µF
(270 Ω)
1
2
3
4
5
6
7
8
TDA2653
16
15
14
13
12
11
10
9
n.c.
4,7 nF
10 kΩ
3,3 kΩ
1 kΩ
sync pulse
blanking pulse
47 kΩ
47 kΩ
2,2 kΩ
2,2 µF
(680 Ω)
18 kΩ
22 kΩ
(18 kΩ)
4,7 kΩ
8,2 Ω
100 nF
DEFL. COIL
(560 Ω)
2200 µF
amplitude
100 Ω
120 Ω
0,56 Ω
(1 Ω)
7Z84212.2

Fig. 3 Typical vertical deflection circuit for 30AX. The values given in parentheses and the dotted components are valid for the PIL-S4 system.

# VERTICAL DEFLECTION CIRCUIT

The TDA2653A is a monolithic integrated circuit for vertical deflection in large screen colour television receivers, e.g. 30AX and PIL-S4 systems.

The circuit incorporates the following functions:

- Oscillator; switch capability for 50 Hz/60 Hz operation.
- Synchronization circuit.
- Blanking pulse generator with guard circuit.
- Sawtooth generator with buffer stage.
- Preamplifier with fed-out inputs.
- Output stage with thermal and short-circuit protection.
- Flyback generator.
- Voltage stabilizer.

## QUICK REFERENCE DATA

| | | | | |
|---|---|---|---|---|
| For 30AX system | | | | |
| Supply voltage (pin 9) | $V_{9\text{-}8} = V_S$ | typ. | 26 | V |
| Supply current (pin 5 + pin 9) | $I_5 + I_9 = I_S$ | typ. | 325 | mA |
| Output current (peak-to-peak value) | $I_{6(p\text{-}p)}$ | typ. | 2,2 | A |
| Picture frequency | f | | 50 Hz/60 | Hz |
| Sync input pulse (peak-to-peak value) | $V_{2\text{-}8(p\text{-}p)}$ | $\geqslant$ | 1 | V |
| Thermal resistance from junction to mounting base | $R_{th\ j\text{-}mb}$ | $\leqslant$ | 5 | K/W |

## PACKAGE OUTLINE

13-lead DIL; plastic power (SOT-141B).

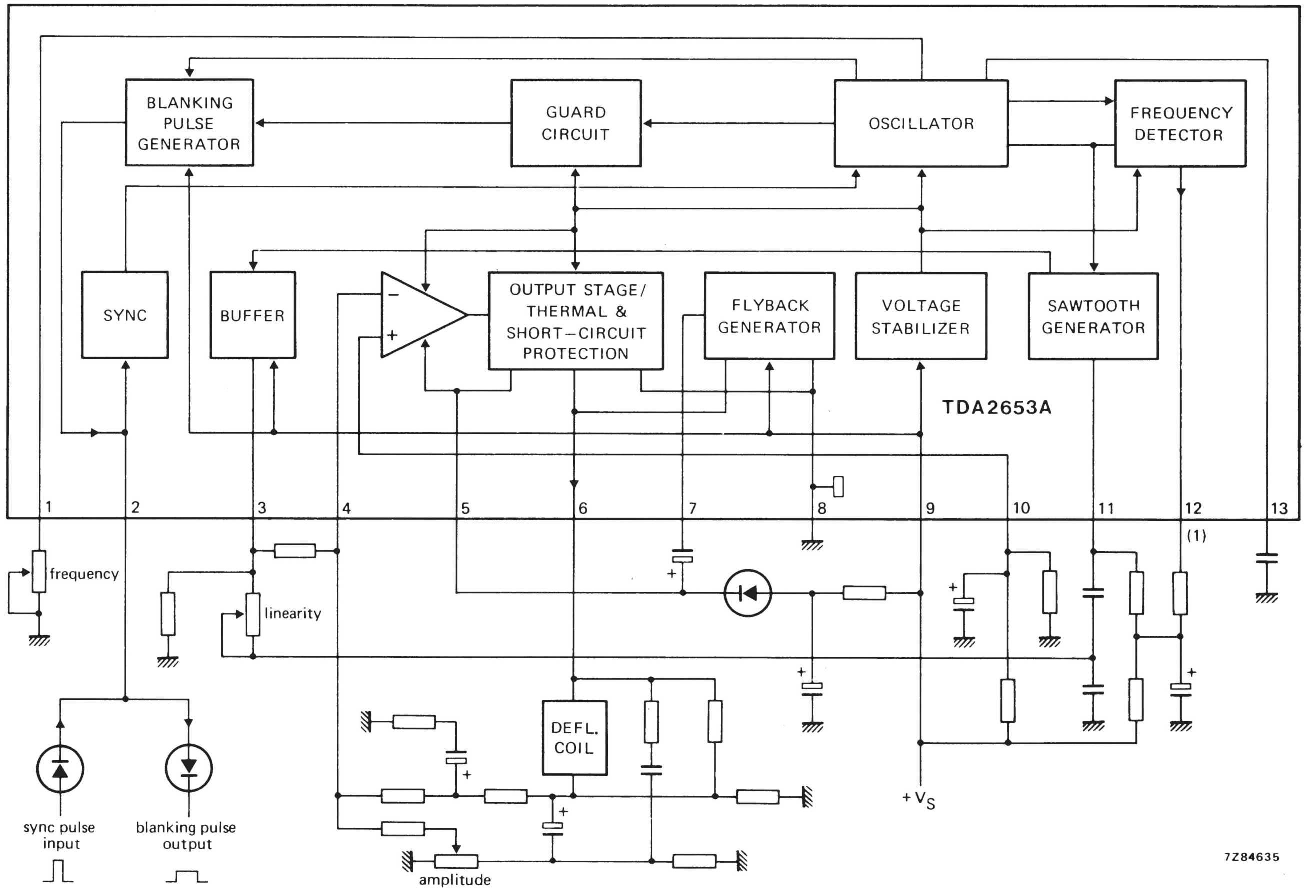

TDA2653A
BLANKING PULSE GENERATOR
GUARD CIRCUIT
OSCILLATOR
FREQUENCY DETECTOR
SYNC
BUFFER
OUTPUT STAGE/ THERMAL & SHORT–CIRCUIT PROTECTION
FLYBACK GENERATOR
VOLTAGE STABILIZER
SAWTOOTH GENERATOR
–
+
1
2
3
4
5
6
7
8
9
10
11
12
13
(1)
frequency
linearity
DEFL. COIL
amplitude
+V<sub>S</sub>
sync pulse input
blanking pulse output
7Z84635

Fig. 1 Block diagram.

(1) Condition for pin 12: LOW voltage level = 50 Hz; HIGH voltage level = 60 Hz.

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | | |
|---|---|---|---|---|
| Supply voltage (pin 9) | $V_{9-8} = V_S$ | max. | 40 | V |
| Supply voltage output stage (pin 5) | $V_{5-8}$ | max. | 58 | V |
| Voltages | | | | |
| Pin 3 | $V_{3-11}$ | max. | 7 | V |
| Pin 13 | $V_{13-8}$ | max. | 7 | V |
| Pins 4 and 10 | $V_{4;10-8}$ | max. | 24 | V |
| Pin 6 | $V_{6-8}$ | max. | 58 | V |
| | $-V_{6-8}$ | max. | 0 | V |
| Pins 7 and 11 | $V_{7;11-8}$ | max. | 40 | V |
| Currents | | | | |
| Pin 1 | $I_1$ | max. | 0 | mA |
| | $-I_1$ | max. | 1 | mA |
| Pin 2 | $\pm I_2$ | max. | 10 | mA |
| Pin 3 | $I_3$ | max. | 0 | mA |
| | $-I_3$ | max. | 5 | mA |
| Pin 7 | $I_7$ | max. | 1,2 | A |
| | $-I_7$ | max. | 1,5 | A |
| Pin 11 | $I_{11}$ | max. | 50 | mA |
| | $-I_{11}$ | max. | 1 | mA |
| Pin 12 | $I_{12}$ | max. | 3 | mA |
| | $-I_{12}$ | max. | 0 | mA |

Pins 5, 6 and 8: internally limited by the short-circuit protection circuit.

Total power dissipation: internally limited by the thermal protection circuit.

| | | |
|---|---|---|
| Storage temperature range | $T_{stg}$ | −25 to + 150 °C |
| Operating ambient temperature range | $T_{amb}$ | −20 °C to limiting value |

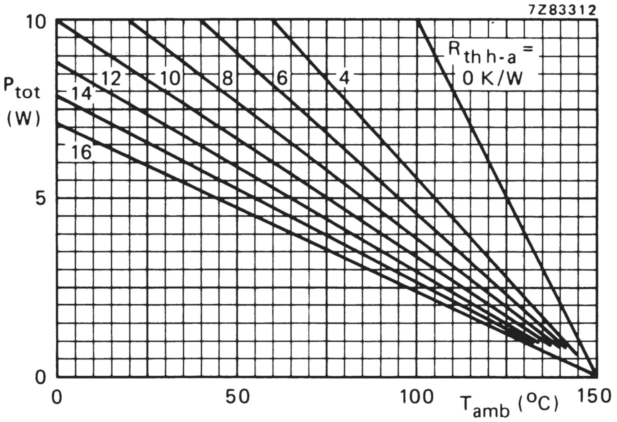


Fig. 2 Total power dissipation. $R_{th\,h-a}$ includes $R_{th\,mb-h}$ which is expected when heat-sink compound is used. $R_{th\,j-mb} \leqslant 5$ K/W.

## CHARACTERISTICS

$T_{amb}$ = 25 °C unless otherwise specified.

**Supply voltage/output stage**

| | | | | |
|---|---|---|---|---|
| Supply voltage | $V_{9-8} = V_S$ | | 9 to 30 | V |
| Output voltage<br>at $-I_6$ = 1,1 A | $V_{6-8}$ | $\geq$<br>typ. | $V_{5-8} - 2,2$<br>$V_{5-8} - 1,9$ | V<br>V |
| at $I_6$ = 1,1 A | $V_{6-8}$ | typ.<br>$\leq$ | 1,3<br>1,6 | V<br>V |
| Flyback generator output voltage at $-I_6$ = 1,1 A | $V_{7-8}$ | typ. | $V_S - 2,2$ | V |
| Peak output current | $\pm I_6$ | $\leq$ | 1,2 | A |
| Flyback generator peak current | $\pm I_7$ | $\leq$ | 1,2 | A |

**Feedback**

| | | | | |
|---|---|---|---|---|
| Input quiescent current | $-I_{4;10}$ | typ. | 0,1 | μA |

**Synchronization**

| | | | | |
|---|---|---|---|---|
| Sync input pulse | $V_{2-8}$ | | 1 to 12 | V |
| Tracking range | | typ. | 28 | % |

**Oscillator/sawtooth generator**

| | | | | |
|---|---|---|---|---|
| Oscillator frequency control input voltage | $V_{1-8}$ | | 6 to 9 | V |
| Sawtooth generator output voltage | $V_{3-8}$<br>$V_{11-8}$ | | 0 to $V_S - 1$<br>0 to $V_S - 2$ | V<br>V |
| Sawtooth generator output current | $-I_3$ | | 0 to 4 | mA |
| | $I_{11}$ | $\geq$<br>$\leq$ | $-2$<br>$+30$ | μA<br>mA |
| Oscillator temperature dependency<br>$T_{case}$ = 20 to 100 °C | $(\Delta f/f)/\Delta T_{case}$ | typ. | $10^{-4}$ | $K^{-1}$ |
| Oscillator voltage dependency<br>$V_S$ = 10 to 30 V | $(\Delta f/f)/\Delta V_S$ | typ. | $4 \times 10^{-4}$ | $V^{-1}$ |

**Blanking pulse generator**

| | | | | |
|---|---|---|---|---|
| Output voltage<br>at $V_S$ = 24 V; $I_2$ = 1 mA | $V_{2-8}$ | typ. | 18,5 | V |
| Output current | $-I_2$ | $\leq$ | 3 | mA |
| Output resistance | $R_{2-8}$ | typ. | 410 | Ω |
| Blanking pulse duration at 50 Hz sync | $t_b$ | typ. | 1,4 ± 0,07 | ms |

**50 Hz/60 Hz switch capability**

| | | | | |
|---|---|---|---|---|
| Saturation voltage; LOW voltage level | $V_{12-8}$ | typ. | 1 | V |
| Output leakage current | $I_{12}$ | typ. | 1 | μA |

**Thermal resistance/junction temperature**

| | | | |
|---|---|---|---|
| From junction to mounting base | $R_{th\ j\text{-}mb}$ | ⩽ | 5 K/W |
| Junction temperature; switching point thermal protection | $T_j$ | typ. | 150 ± 8 °C |

## PINNING

1. Oscillator adjustment
2. Synchronization input/blanking output
3. Sawtooth generator output
4. Preamplifier input
5. Positive supply of output stage
6. Output
7. Flyback generator output
8. Ground
9. Positive supply ($V_S$)
10. Reference voltage
11. Sawtooth capacitor
12. 50 Hz/ 60 Hz switching voltage
13. Oscillator capacitor

## APPLICATION INFORMATION

**The function is described against the corresponding pin number**

1, 13. Oscillator

The oscillator frequency is determined by a potentiometer at pin 1 and a capacitor at pin 13.

2. Sync input/blanking output

Combination of sync input and blanking output. The oscillator has to be synchronized by a positive-going pulse between 1 and 12 V. The integrated frequency detector delivers a switching level at pin 12.
The blanking pulse amplitude is 20 V with a load of 1 mA.

3. Sawtooth generator output

The sawtooth signal is fed via a buffer stage to pin 3. It delivers the signal which is used for linearity control, and drive of the preamplifier. The sawtooth is applied via a shaping network to pin 11 (linearity) and via a resistor to pin 4 (preamplifier).

4. Preamplifier input

The d.c. voltage is proportional to the output voltage (d.c. feedback). The a.c. voltage is proportional to the sum of the buffered sawtooth voltage at pin 3 and the voltage, with opposite polarity, at the feedback resistor (a.c. feedback).

5. Positive supply of output stage

This supply is obtained from the flyback generator. An electrolytic capacitor between pins 7 and 5, and a diode between pins 5 and 9 have to be connected for proper operation of the flyback generator.

6. Output of class-B power stage

The vertical deflection coil is connected to this pin, via a series connection of a coupling capacitor and a feedback resistor, to ground.

7. Flyback generator output

An electrolytic capacitor has to be connected between pins 7 and 5 to complete the flyback generator.

8. Negative supply (ground)

Negative supply of output stage and small signal part.

9. Positive supply

The supply voltage at this pin is used to supply the flyback generator, voltage stabilizer, blanking pulse generator and buffer stage.

**APPLICATION INFORMATION** (continued)

10. Reference voltage of preamplifier

    External adjustment and decoupling of reference voltage of the preamplifier.

11. Sawtooth capacitor

    This sawtooth capacitor has been split to realize linearity control.

12. 50 Hz/60 Hz switching level

    This pin delivers a LOW voltage level for 50 Hz and a HIGH voltage level for 60 Hz. The amplitudes of the sawtooth signals can be made equal for 50 Hz and 60 Hz with these levels.

The following application data are measured in Figs 3 and 4.

| | | | 30AX system (26 V) Fig. 3 | 30AX system (26 V/12 V) Fig. 4 | PIL-S4 system Fig. 3 | |
|---|---|---|---|---|---|---|
| System supply voltages | $V_{S1}$ | typ. | 26 | 26 | 26 | V |
| | $V_{S2}$ | typ. | – | 12 | – | V |
| System supply currents | $I_{S1}$ | typ. | 315 | 330 | 195 | mA |
| | $I_{S2}$ | typ. | – | –35 | – | mA |
| Output voltage | $V_{6\text{-}8}$ | typ. | 14 | 14,6 | 13,5 | V |
| Output voltage (peak value) | $V_{6\text{-}8}$ | typ. | 42 | 42 | 49 | V |
| Deflection current (peak-to-peak value) | $I_{6(p\text{-}p)}$ | typ. | 2,2 | 2,2 | 1,32 | A |
| Flyback time | $t_{fl}$ | typ. | 1 | 0,9 | 1,1 | ms |
| Total power dissipation per package | $P_{tot}$ | typ. | 4,1 | 4 | 3 | W |
| | | max. | 4,8 | 4,8 | 3,4 | W* |
| Oscillator frequency unsynchronized | f | typ. | 46,5 | 46,5 | 46,5 | Hz |

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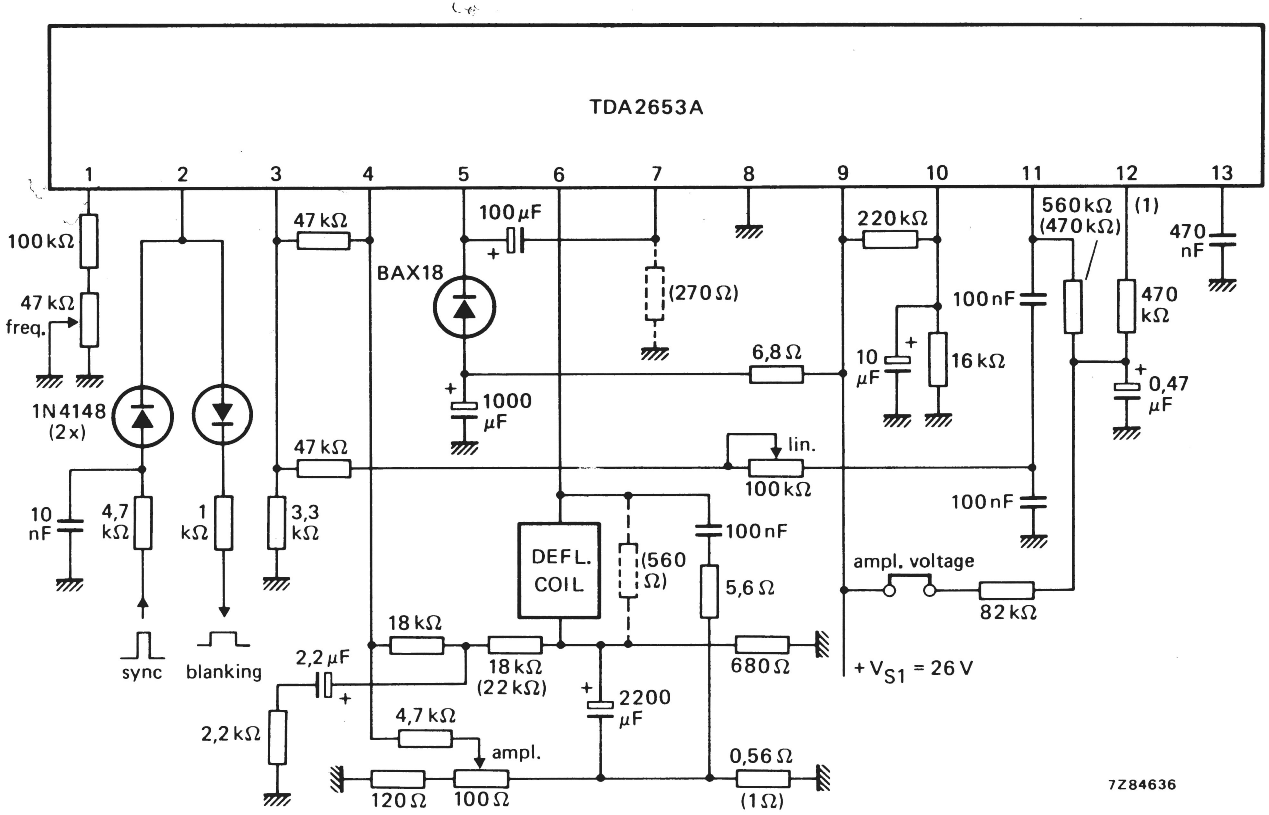
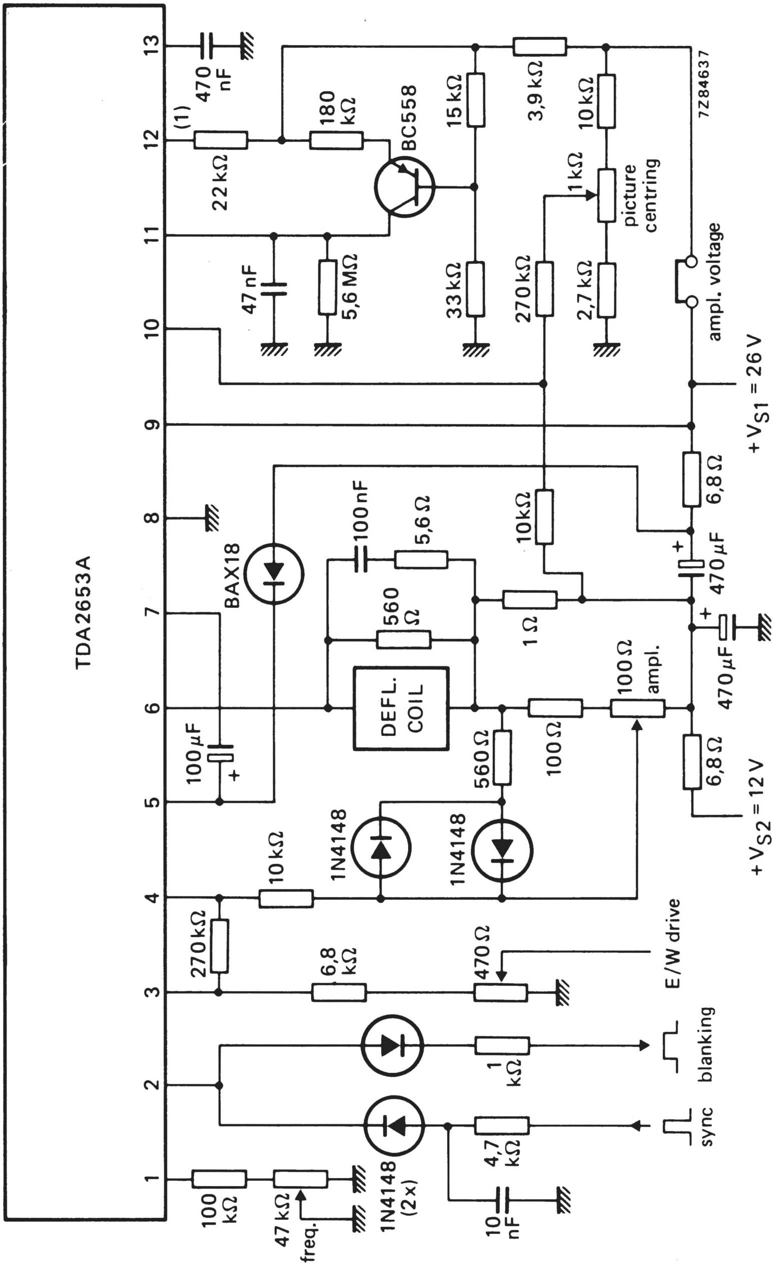
* Calculated with $\Delta V_S = +5\%$ and $\Delta R_{yoke} = -7\%$.


TDA2653A
1
2
3
4
5
6
7
8
9
10
11
12
13
100 kΩ
47 kΩ
freq.
1N4148
(2x)
10 nF
4,7 kΩ
1 kΩ
sync
blanking
47 kΩ
47 kΩ
3,3 kΩ
BAX18
100 μF
1000 μF
(270 Ω)
6,8 Ω
220 kΩ
10 μF
16 kΩ
100 nF
560 kΩ
(470 kΩ)
(1)
470 kΩ
0,47 μF
470 nF
lin.
100 kΩ
100 nF
DEFL. COIL
(560 Ω)
100 nF
5,6 Ω
ampl. voltage
82 kΩ
18 kΩ
18 kΩ
(22 kΩ)
680 Ω
+ V_S1 = 26 V
2,2 μF
2,2 kΩ
4,7 kΩ
ampl.
2200 μF
120 Ω
100 Ω
0,56 Ω
(1 Ω)
7Z84636

(1) Condition for pin 12: LOW voltage level = 50 Hz; HIGH voltage level = 60 Hz.

Fig. 3 Typical vertical deflection circuit for 30AX system (26 V). The values given in parentheses and the dotted components are valid for the PIL-S4 system.


TDA2653A
1
2
3
4
5
6
7
8
9
10
11
12
13
470 nF
(1)
22 kΩ
180 kΩ
BC558
15 kΩ
3,9 kΩ
10 kΩ
1 kΩ
picture centring
47 nF
5,6 MΩ
33 kΩ
270 kΩ
2,7 kΩ
ampl. voltage
+ V_S1 = 26 V
7Z84637
BAX18
100 nF
5,6 Ω
560 Ω
10 kΩ
1 Ω
6,8 Ω
470 µF
470 µF
100 µF
DEFL. COIL
100 Ω
100 Ω ampl.
560 Ω
6,8 Ω
+ V_S2 = 12 V
1N4148
1N4148
10 kΩ
270 kΩ
6,8 kΩ
470 Ω
E/W drive
blanking
1 kΩ
sync
4,7 kΩ
10 nF
100 kΩ
47 kΩ
freq.
1N4148 (2x)

(1) Condition for pin 12: LOW voltage level = 50 Hz; HIGH voltage level = 60 Hz.

Fig. 4 Typical vertical deflection circuit for 30AX system ($V_{S1}$ = 26 V, $V_{S2}$ = 12 V) in quasi-bridge connection.

# VERTICAL DEFLECTION CIRCUIT

The TDA2654 is a monolithic integrated circuit for vertical deflection in monochrome and tiny-vision colour television receivers.

The circuit incorporates the following functions:

- Oscillator
- Synchronization circuit
- Blanking pulse generator
- Sawtooth generator
- S-correction and linearity circuit
- Comparator and drive circuit
- Output stage
- Flyback dissipation limiting circuit
- Supply for pre-stages via internal voltage divider
- Thermal protection circuit
- Controlled switch-on

## QUICK REFERENCE DATA

| | | | | |
|---|---|---|---|---|
| Supply voltage range (ref. to tab = ground) | $V_P$ | | 10 to 35 | V |
| Output current (peak-to-peak value) | $I_{9(p\text{-}p)}$ | max. | 2 | A |
| Total power dissipation | $P_{tot}$ | max. | 5 | W |
| Operating junction temperature | $T_j$ | max. | 150 | °C |
| Thermal resistance from junction to tab | $R_{th\ j\text{-}tab}$ | = | 12 | °C/W |

## PACKAGE OUTLINE

9-lead SIL; plastic (SOT-110B).

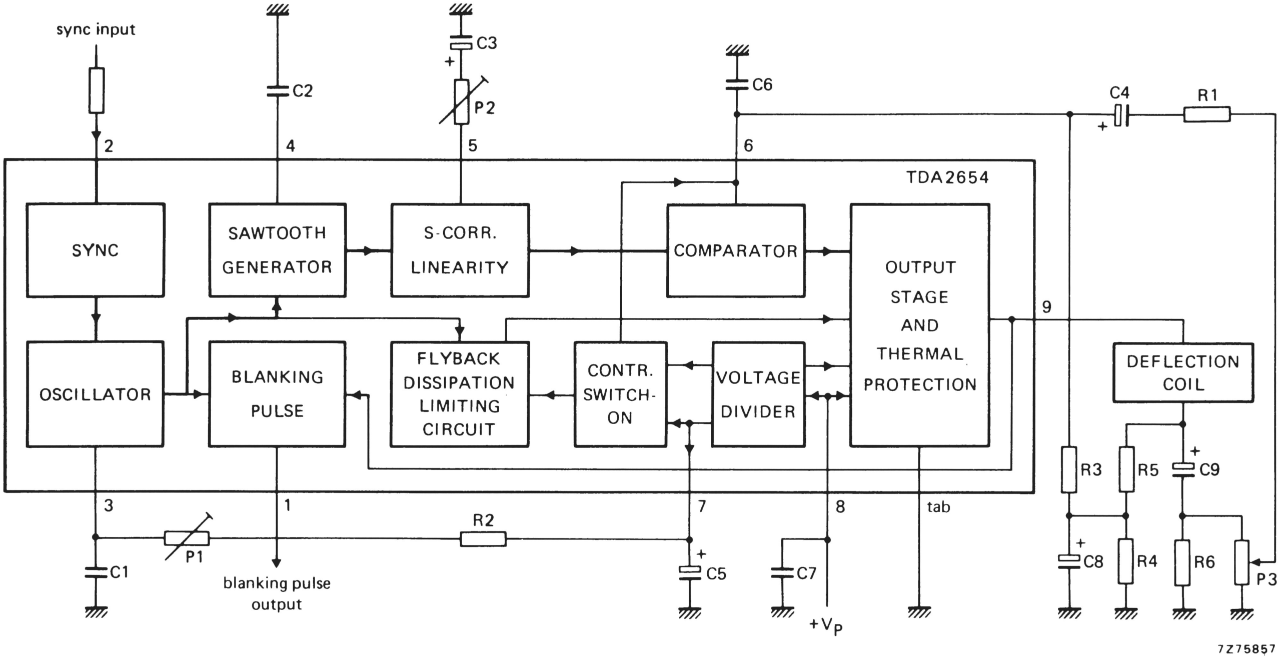

sync input
2
4
5
6
C2
C3
P2
C6
C4
R1
TDA2654
SYNC
SAWTOOTH GENERATOR
S-CORR. LINEARITY
COMPARATOR
OUTPUT STAGE AND THERMAL PROTECTION
OSCILLATOR
BLANKING PULSE
FLYBACK DISSIPATION LIMITING CIRCUIT
CONTR. SWITCH-ON
VOLTAGE DIVIDER
DEFLECTION COIL
9
3
1
7
8
tab
C1
P1
R2
blanking pulse output
C5
C7
+V_P
R3
R5
C9
C8
R4
R6
P3
7Z75857

Fig. 1 Block diagram.

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

All voltages and currents refer to the tab (ground) connection.

| | | | | |
|---|---|---|---|---|
| **Voltages** | | | | |
| Pin 2 | $V_2$ | max. | 5 | V |
| Pin 3 | $V_3$ | max. | 17 | V |
| Pin 4 | $V_4$ | max. | 17 | V |
| Pin 5 | $V_5$ | max. | 6 | V |
| Pin 6 | $V_6$ | max. | 13 | V |
| Pin 7 | $V_7$ | max. | 18 | V |
| Pin 8 | $V_8$ ($V_P$) | max. | 35 | V |
| **Currents** | | | | |
| Pin 1 | $+I_1$ | max. | 1 | mA |
| | $-I_1$ | max. | 5 | mA |
| Pin 2 | $I_2$ | max. | 2,5 | mA |
| Pin 3 | $I_3$ | max. | 30 | mA |
| Pin 4 | $I_4$ | max. | 30 | mA |
| Pin 5 | $\pm I_5$ | max. | 1 | mA |
| Pin 6 | $\pm I_6$ | max. | 3 | mA |
| Pin 9 (repetitive) | $\pm I_9$ | max. | 1 | A |
| Pin 9 (non-repetitive) | $\pm I_9$ | max. | 1,5 | A |
| Total power dissipation (see also Fig. 2) | $P_{tot}$ | max. | 5 | W |
| Storage temperature | $T_{stg}$ | −25 to + | 150 | °C |
| Operating junction temperature | $T_j$ | max. | 150 | °C |

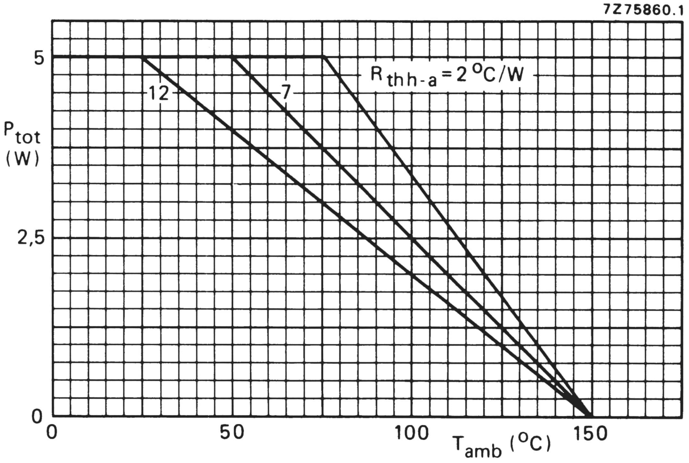


Fig. 2 Total power dissipation. The graph takes into account an $R_{th\,tab\text{-}h} = 1$ °C/W which is to be expected when the tab is connected to a heatsink with one 3 mm bolt, without using heatsink compound. $R_{th\,j\text{-}tab} = 12$ °C/W.

## CHARACTERISTICS

$T_{amb}$ = 25 °C unless otherwise specified; voltages and currents ref. to tab (ground)

| | | | monochrome (Fig. 3) | tiny-vision colour (Fig. 4) | |
|---|---|---|---|---|---|
| Supply voltage (pin 8) | $V_P$ | typ. | 25 | 31 | V |
| Supply current (pin 8) | $I_P$ | typ. | 165 | 150 | mA |
| Total power dissipation | $P_{tot}$ | typ. | 3,1 | 3,5 | W |
| Output voltage (peak-to-peak value) | $V_{9(p-p)}$ | typ. | 22 | 28 | V |
| Blanking pulse; $I_1$ = 1 mA | $V_1$ | typ. | 11,5 | 14,5 | V |
| Blanking pulse duration | $t_p$ | typ. | 1,3 | 1,4 | ms |
| D.C. input voltage (pin 6) | $V_6$ | typ. | 3,4 | 4,4 | V |
| Deflection current (peak-to-peak value) | $I_{9(p-p)}$ | typ. | 1,1 | 0,92 | A |
| Flyback time | t | typ. | 1,3 | 1,32 | ms |
| Free running oscillator frequency | $f_{osc}$ | typ. | 46 | 46 | Hz |
| Oscillator thermal drift | | typ. | –0,01 | –0,01 | Hz/°C |
| Oscillator voltage shift | | typ. | –0,13 | –0,12 | Hz/V |
| Tracking range oscillator | | typ. | 18 | 18 | % |
| Synchronization input voltage | $V_2$ | > | 1 | 1 | V |
| Voltage divider ratio | $V_7/V_8$ | typ. | 0,52 | 0,52 | |
| Input resistance pin 7 | $R_7$ | typ. | 2,8 | 2,8 | kΩ |
| Recommended thermal resistance of heatsink for $T_{amb}$ up to 70 °C | $R_{th\ h\text{-}a}$ | < | 13 | 10 | °C/W |

## PINNING

1. Blanking pulse output
2. Synchronization input
3. Oscillator timing network
4. Sawtooth generator
5. S-correction and linearity control
6. Feedback input
7. Voltage divider
8. Positive supply
9. Output

Tab. Negative supply (ground)

## APPLICATION INFORMATION (see also Fig. 1)

**The function is described against the corresponding pin number**

1. Blanking pulse output

When the IC is adjusted on a free running frequency of 46 Hz the internal blanking pulse generator delivers a blanking pulse with a duration between 1,2 ms and 1,5 ms. The circuit is, however, made such that when the flyback time of the deflection current is longer, the blanking pulse corresponds to the flyback time. The output voltage is also high when the voltage at pin 9 is lower than nominal 5 V. An external blanking circuit is recommended when tiny-vision receivers are operated from a car-battery.

2. Synchronization input

The oscillator has to be synchronized by a positive-going pulse. The circuit is made such that synchronization is inhibited during the flyback time.

## APPLICATION INFORMATION (continued)

3. Oscillator

   The oscillator frequency is set by the potentiometer P1 and resistor R2 between pins 3 and 7 and capacitor C1 between pin 3 and ground. For 50 Hz systems the free running frequency is preferably adjusted to 46 Hz.

4. Sawtooth generator

   This pin supplies the charging and discharging currents of the capacitor between pin 4 and ground (C2).

5. S-correction and linearity control

   The amount of S-correction can be set by the value of C3. For 110° deflection coils, e.g. AT1040/15, a capacitor of 15 $\mu$F will give the right value for S-correction. For 90° deflection systems (e.g. AT1235/00) a nearly linear deflection current is required, this can be achieved by increasing C3 to 100 $\mu$F. The linearity can be adjusted by potentiometer P2.

6. Output current feedback

   To this pin is applied a part of the output current measured across R6 and superimposed on a d.c. voltage derived from the voltage across the output coupling capacitor. This signal is compared with the internal reference sawtooth. The internal reference sawtooth has an amplitude of about 0,6 V peak to peak and a d.c. level of about 3,4 V, for a supply voltage of 25 V at pin 8.

7. Internal voltage divider decoupling

   The voltage on this pin is about half the supply voltage at pin 8 and is applied to the bases of emitter followers supplying the pre-stages of the IC. This voltage controls the amplitude of the internal reference sawtooth. In this way tracking with the line deflection system is achieved when the supply voltage at pin 8 is derived from the line output transformer.

8. Positive supply

   The value depends on the deflection coil.

9. Output

   The deflection coil is connected to ground via coupling capacitor C9 and current sensing resistor R6. The line frequency superimposed on the output voltage may be too high due to the current feedback system. The line frequency ripple can be decreased by connecting a resistor across the deflection coil. The flyback time can be influenced by the resistor divider (R4, R5) for the d.c. feedback to pin 6. It should be noted that the output voltage shows a negative swing of about 1 V during the first (positive current) part of the flyback.

Tab

The tab is used as negative supply (ground) connection. Therefore, the tab should be well connected to the negative side of the power supply.

Controlled switch-on

This feature is achieved by charging the a.c. coupling capacitor (C4; connected to pin 6) from an internal current source of about 2 mA (voltage limited to maximum 15 V) for a short period after switch-on. The charging time can be influenced by the value of C5 (connected to pin 7). Discharging of C4 results in a slowly increasing deflection current after a delay of about 1 second. The blanking voltage at pin 1 is high during this delay.

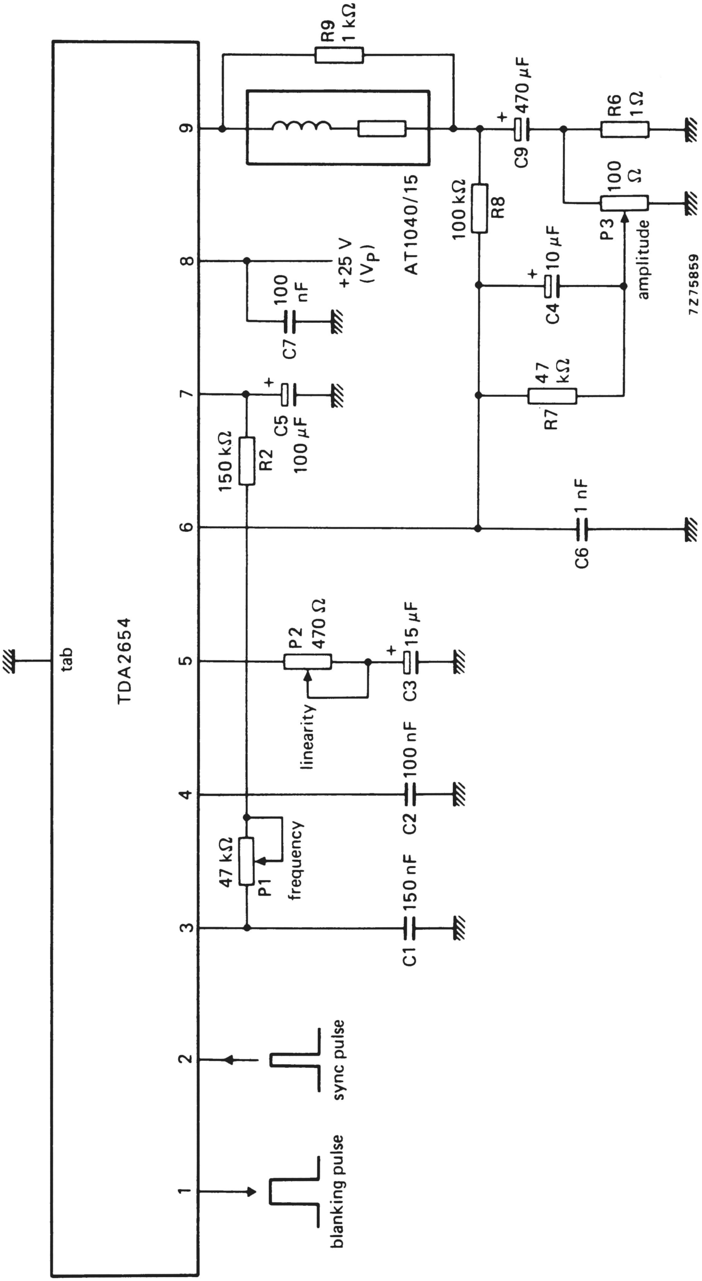
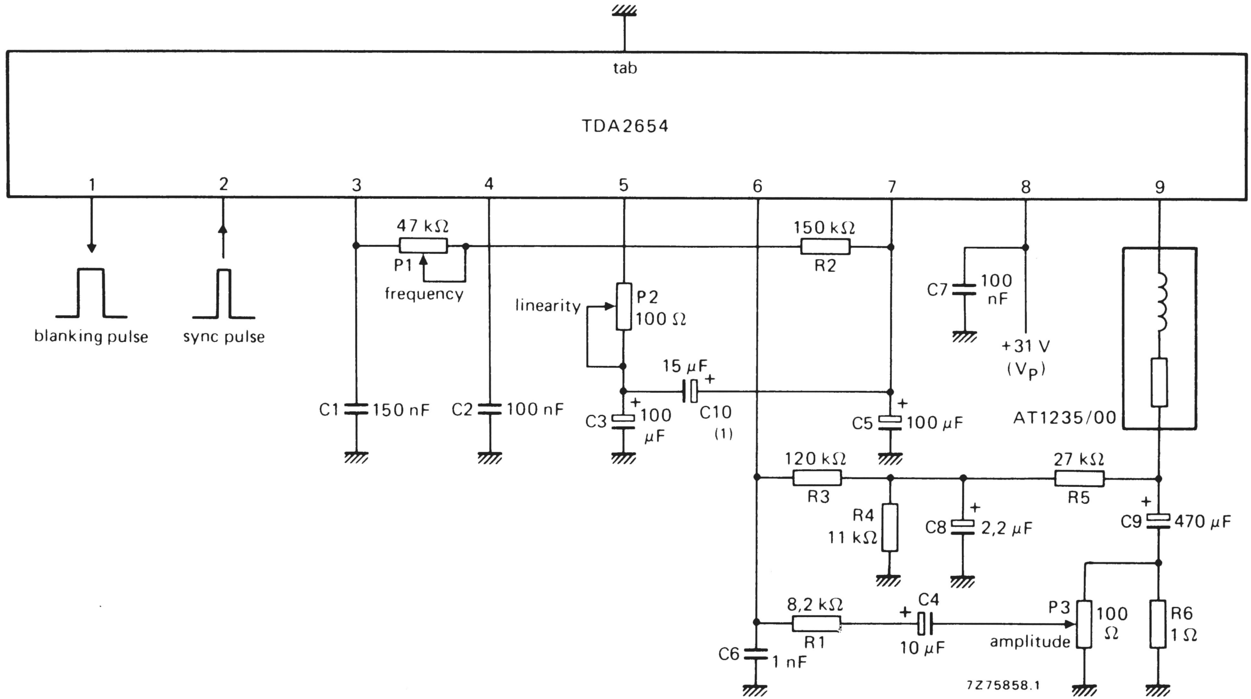

TDA2654
tab
1
2
3
4
5
6
7
8
9
blanking pulse
sync pulse
C1
150 nF
P1
47 kΩ
frequency
C2
100 nF
linearity
P2
470 Ω
C3
15 μF
+
R2
150 kΩ
C5
100 μF
+
C7
100 nF
+25 V
($V_P$)
AT1040/15
R9
1 kΩ
C9
470 μF
+
R8
100 kΩ
R6
1 Ω
P3
100 Ω
amplitude
C4
10 μF
+
R7
47 kΩ
C6
1 nF
7Z75859

Fig. 3 Monochrome 110° vertical deflection system.

APPLICATION INFORMATION (continued)


tab
TDA2654
1
2
3
4
5
6
7
8
9
blanking pulse
sync pulse
47 kΩ
P1
frequency
150 kΩ
R2
C7
100 nF
+31 V
(V$_P$)
linearity
P2
100 Ω
15 μF
C10
(1)
C1
150 nF
C2
100 nF
C3
100 μF
C5
100 μF
AT1235/00
120 kΩ
R3
27 kΩ
R5
R4
11 kΩ
C8
2,2 μF
C9
470 μF
8,2 kΩ
R1
C4
10 μF
P3
100 Ω
amplitude
R6
1 Ω
C6
1 nF
7Z75858.1

(1) Only required when rapid variations in the supply voltage are expected.

Fig. 4 Colour 90° vertical deflection system.

# VERTICAL DEFLECTION CIRCUIT

The TDA2655A is a monolithic integrated circuit for vertical deflection in colour television receivers with 90° picture tubes.

The circuit incorporates the following functions:

- Synchronization circuit.
- Oscillator.
- Sawtooth generator with buffer stage.
- Preamplifier with fed-out inputs.
- Output stage with thermal and short-circuit protection.
- Flyback generator.
- Blanking pulse generator with guard circuit.
- Voltage stabilizer.

## QUICK REFERENCE DATA

For 90° deflection; measured with respect to cooling fin (ground)

| | | | | |
|---|---|---|---|---|
| System supply voltages | $V_{S1}$ | typ. | 22 | V |
| | $V_{S2}$ | typ. | 12 | V |
| System supply currents | $I_{S1}$ | typ. | 135 | mA |
| | $-I_{S2}$ | typ. | 8 | mA |
| Deflection current | $I_9$ | typ. | 425 | mA |
| Sync input pulse (peak-to-peak value) | $V_{4(p\text{-}p)}$ | $\geqslant$ | 1 | V |

## PACKAGE OUTLINE

12-lead DIL; plastic with metal cooling fin (SOT-150).

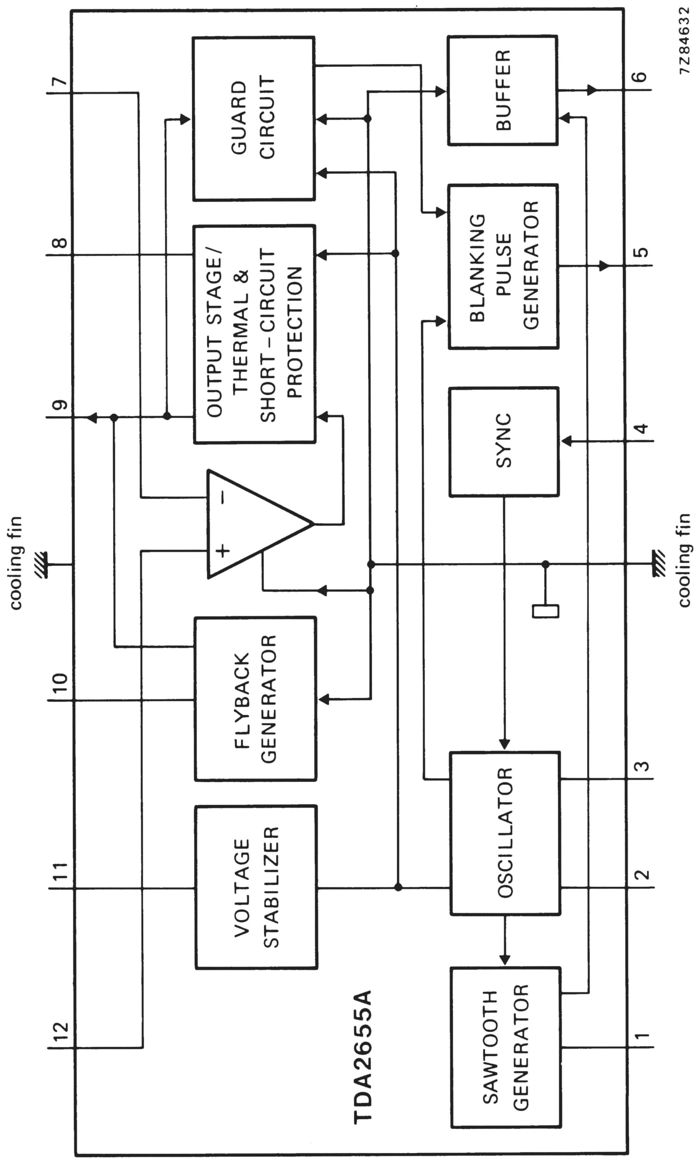

TDA2655A
GUARD CIRCUIT
OUTPUT STAGE/ THERMAL & SHORT-CIRCUIT PROTECTION
FLYBACK GENERATOR
VOLTAGE STABILIZER
BUFFER
BLANKING PULSE GENERATOR
SYNC
OSCILLATOR
SAWTOOTH GENERATOR
−
+
cooling fin
cooling fin
1
2
3
4
5
6
7
8
9
10
11
12
7Z84632

Fig. 1 Block diagram.

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages with respect to cooling fin (ground)

| | | | | |
|---|---|---|---|---|
| Supply voltage (pin 11) | $V_{11} = V_S$ | max. | 40 | V |
| Supply voltage output stage (pin 8) | $V_8$ | max. | 55 | V |
| Pin 9 | $V_9$ | max. | 55 | V |
| | $-V_9$ | max. | 0 | V |
| Pin 4 | $V_4$ | max. | 30 | V |
| Pin 10 | $V_{10}$ | max. | 40 | V |
| Pin 2 | $V_2$ | max. | 7 | V |
| Pin 1 | $V_1$ | max. | 40 | V |
| Pin 6 with respect to 1 | $V_{6-1}$ | max. | 7 | V |
| Pins 7 and 12 | $V_7; V_{12}$ | max. | 24 | V |
| Currents | | | | |
| Pin 10 | $I_{10}$ | max. | 1,2 | A |
| | $-I_{10}$ | max. | 1,5 | A |
| Pin 5 | $\pm I_5$ | max. | 15 | mA |
| Pin 3 | $I_3$ | max. | 0 | mA |
| | $-I_3$ | max. | 1 | mA |
| Pin 1 | $I_1$ | max. | 50 | mA |
| | $-I_1$ | max. | 1 | mA |
| Pin 6 | $I_6$ | max. | 0 | mA |
| | $-I_6$ | max. | 5 | mA |

Pins 8, 9 and cooling fin: internally limited by the short-circuit protection circuit.

Total power dissipation: internally limited by the thermal protection circuit.

| | | |
|---|---|---|
| Storage temperature range | $T_{stg}$ | −25 to + 150 °C |
| Operating ambient temperature range | $T_{amb}$ | −20 °C to limiting value |

## CHARACTERISTICS

$T_{amb}$ = 25 °C; measured with respect to cooling fin (ground), unless otherwise specified.

**Supply voltage/output stage**

| | | | | |
|---|---|---|---|---|
| Supply voltage (pin 11) | $V_{11} = V_S$ | | 9 to 30 | V |
| Output voltage<br>at $-I_9$ = 1,1 A | $V_9$ | ≥<br>typ. | $V_8 - 2{,}2$<br>$V_8 - 1{,}9$ | V<br>V |
| at $I_9$ = 1,1 A | $V_9$ | typ.<br>≤ | 1,3<br>1,6 | V<br>V |
| Flyback generator output voltage at $-I_9$ = 1,1 A | $V_{10}$ | typ. | $V_S - 2{,}2$ | V |
| Peak output current | $\pm I_9$ | typ. | 1,2 | A |
| Flyback generator peak current | $\pm I_{10}$ | typ. | 1,2 | A |

**Feedback**

| | | | | |
|---|---|---|---|---|
| Input quiescent current of preamplifier | $-I_{12} = -I_7$ | typ. | 0,1 | μA |

**Synchronization**

| | | | | |
|---|---|---|---|---|
| Sync input pulse | $V_4$ | | 1 to 12 | V |
| Tracking range | | typ. | 20 | % |

**Oscillator/sawtooth generator**

| | | | | |
|---|---|---|---|---|
| Oscillator frequency control input voltage | $V_3$ | | 6 to 9 | V |
| Sawtooth generator output voltage | $V_6$ | | 0 to $V_S - 2{,}0$ | V |
| Oscillator temperature dependency<br>$T_{case}$ = 20 to 100 °C | $(\Delta f/f)/\Delta T_{case}$ | typ. | $10^{-4}$ | $K^{-1}$ |
| Oscillator voltage dependency<br>$V_S$ = 10 to 30 V | $(\Delta f/f)\Delta V_S$ | typ. | $4 \times 10^{-4}$ | $V^{-1}$ |

**Blanking pulse generator**

| | | | | |
|---|---|---|---|---|
| Output voltage<br>at $I_5$ = 10 mA | $V_5$ | typ. | 6 | V |
| at $-I_5$ = 10 mA; pin 11 with respect to pin 5 | $V_{11\text{-}5}$ | typ. | 6 | V |
| Output current | $\pm I_5$ | ≤ | 12 | mA |
| Blanking pulse duration at 50 Hz sync | $t_b$ | typ. | 1,4 ± 0,07 | ms |

**Thermal resistance/junction temperature**

| | | | | |
|---|---|---|---|---|
| From junction to case (cooling fin) | $R_{th\ j\text{-}c}$ | ≤ | 15 | K/W |
| Junction temperature; switching point thermal protection | $T_j$ | typ. | 150 ± 8 | °C |

## PINNING

1. Sawtooth capacitor
2. Oscillator capacitor
3. Oscillator resistor (adjustment)
4. Synchronization input
5. Blanking output
6. Output of sawtooth buffer stage
7. Feedback input
8. Positive supply of output stage
9. Output
10. Flyback generator output
11. Positive supply ($V_S$)
12. Preamplifier input.

## APPLICATION INFORMATION

The following application data are measured in Figs 2 and 3 (90° deflection); with respect to cooling fin (ground).

| | | | Fig. 2 | Fig. 3 | |
|---|---|---|---|---|---|
| System supply voltages | $V_{S1}$ | typ. | 22 | 22 | V |
| | $V_{S2}$ | typ. | 12 | – | V |
| Output voltage (d.c. value) | $V_9$ | typ. | 12,2 | 12 | V |
| Output voltage (peak value) | $V_9$ | typ. | 42 | 42 | V |
| Supply current (pin 8 + pin 11) | $I_8 + I_{11}$ | typ. | 135 | 140 | mA |
| Deflection current (peak value) | $\pm I_9$ | typ. | 450 | 430 | mA* |
| Flyback time | $t_{fl}$ | typ. | 0,9 | 0,9 | ms |
| Total power dissipation per package | $P_{tot}$ | typ. | 1,6 | 1,6 | W |
| System supply current | $-I_{S2}$ | typ. | 8 | – | mA |
| Thermal resistance from junction to ambient | $R_{th\ j\text{-}a}$ | typ. | 40 | 40 | K/W** |

---

* Including 6% overscan.

** Depends on the deflection unit.

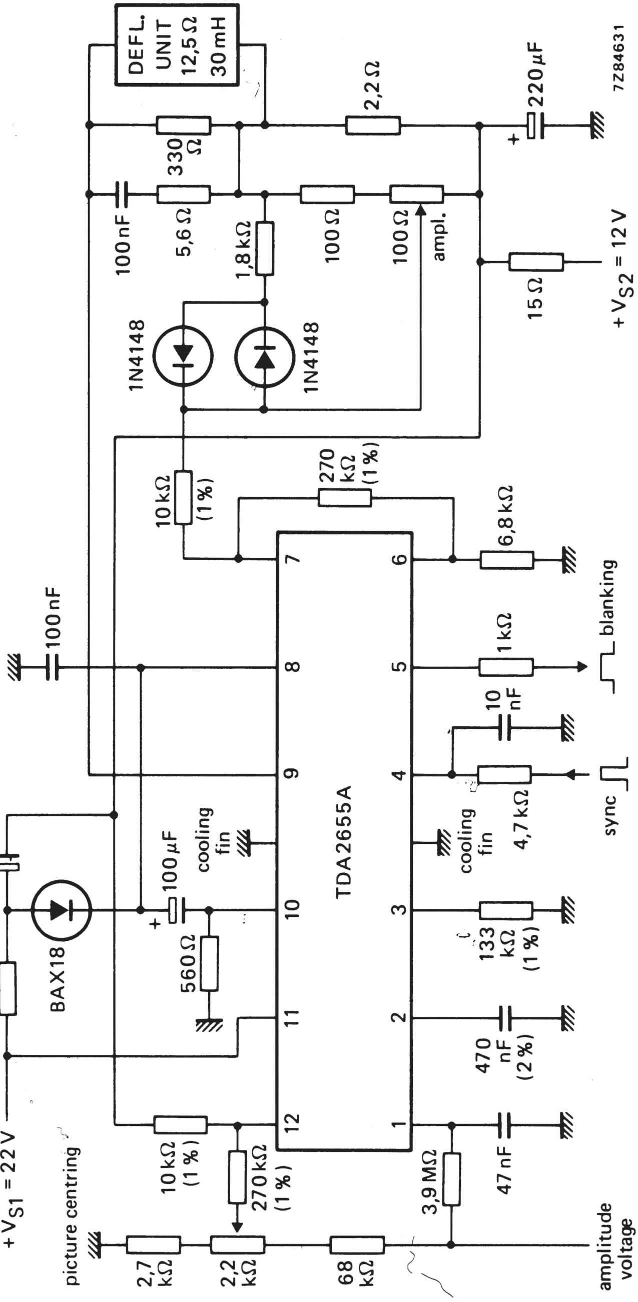

DEFL. UNIT 12,5 Ω 30 mH
2,2 Ω
220 μF
7Z84631
330 Ω
100 nF
5,6 Ω
1,8 kΩ
100 Ω
100 Ω
ampl.
15 Ω
+V$_{S2}$ = 12 V
1N4148
1N4148
270 kΩ (1%)
10 kΩ (1%)
6,8 kΩ
100 nF
1 kΩ
blanking
10 nF
sync
4,7 kΩ
220 μF
100 μF
cooling fin
cooling fin
TDA2655A
BAX18
4,7 Ω
560 Ω
133 kΩ (1%)
470 nF (2%)
+V$_{S1}$ = 22 V
10 kΩ (1%)
270 kΩ (1%)
3,9 MΩ
47 nF
picture centring
2,7 kΩ
2,2 kΩ
68 kΩ
amplitude voltage (+120 V)
1
2
3
4
5
6
7
8
9
10
11
12

Fig. 2 Typical vertical deflection circuit for 90° system in quasi-bridge connection.

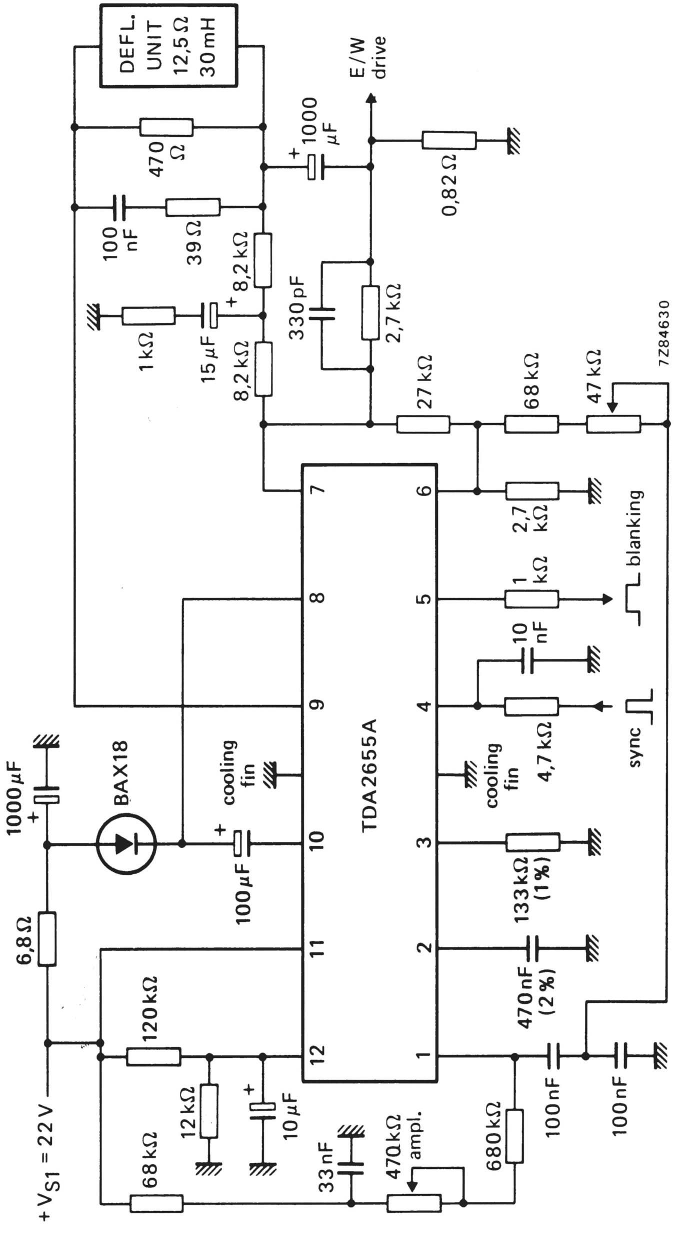

DEFL. UNIT 12,5 Ω 30 mH
470 Ω
100 nF
39 Ω
1000 µF
E/W drive
0,82 Ω
8,2 kΩ
1 kΩ
15 µF
8,2 kΩ
330 pF
2,7 kΩ
27 kΩ
68 kΩ
47 kΩ
7Z84630
2,7 kΩ
1 kΩ
blanking
10 nF
4,7 kΩ
sync
cooling fin
TDA2655A
133 kΩ (1%)
470 nF (2%)
100 nF
100 nF
680 kΩ
470 kΩ ampl.
33 nF
10 µF
12 kΩ
120 kΩ
68 kΩ
+V_S1 = 22 V
6,8 Ω
1000 µF
BAX18
100 µF
1 2 3 4 5 6 7 8 9 10 11 12

Fig. 3 Typical vertical deflection circuit for 90° system with coupling electrolytic capacitor.

DEVELOPMENT SAMPLE DATA
This information is derived from development samples made available for evaluation. It does not necessarily imply that the device will go into regular production.

# VERTICAL DEFLECTION CIRCUIT

## GENERAL DESCRIPTION

The TDA2655B is a monolithic integrated circuit for vertical deflection in colour television receivers with 90° picture tubes.

### Features

- Synchronization circuit
- Vertical oscillator; 50/60 Hz switch
- Sawtooth generator with buffer stage
- Preamplifier with fed-out inputs
- Output stage with termal and short-circuit protection
- Flyback generator
- Blanking pulse generator with guard circuit
- Voltage stabilizer
- Frequency detector with memory and storage

## QUICK REFERENCE DATA

For 90° deflection; measured with respect to cooling fin (ground)

| | | | concept 1* | concept 2* | |
|---|---|---|---|---|---|
| System supply voltages | $V_{P1}$ | typ. | 22 | 22 | V |
| | $V_{P2}$ | typ. | 12 | – | V |
| System supply currents | $I_{P1}$ | typ. | 135 | 140 | mA |
| | $-I_{P2}$ | typ. | 8 | – | mA |
| Deflection current (peak-to-peak value) | $I_{9(p\text{-}p)}$ | typ. | 450 | 450 | mA |
| Synchronization input voltage (peak-to-peak value) | $V_{5(p\text{-}p)}$ | min. | 1 | 1 | V |

*Concept 1: with two supply voltages ; concept 2: with one supply voltage. (See also Figs 2 and 3).

## PACKAGE OUTLINE

12-lead DIL; plastic with metal cooling fin (SOT-150).

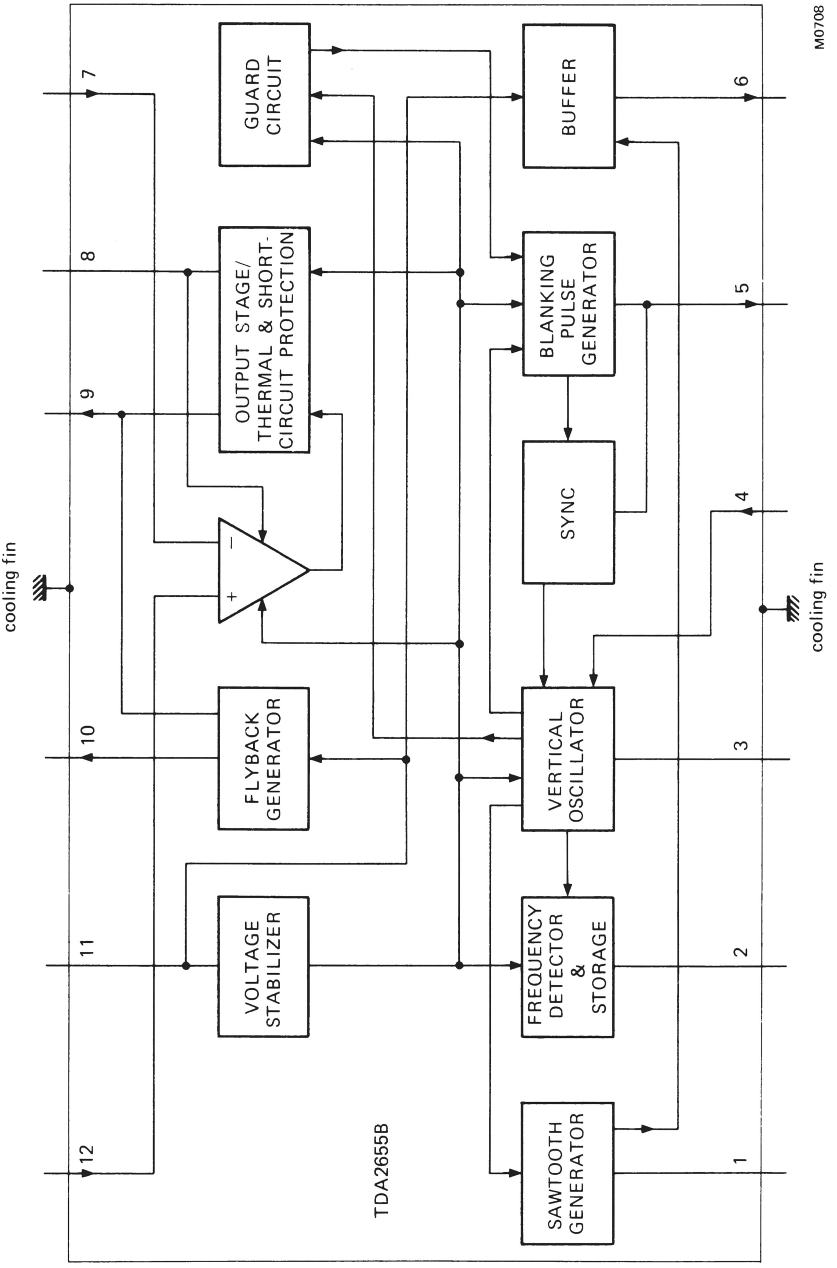

M0708
GUARD CIRCUIT
BUFFER
OUTPUT STAGE/ THERMAL & SHORT-CIRCUIT PROTECTION
BLANKING PULSE GENERATOR
SYNC
FLYBACK GENERATOR
VERTICAL OSCILLATOR
VOLTAGE STABILIZER
FREQUENCY DETECTOR & STORAGE
SAWTOOTH GENERATOR
TDA2655B
cooling fin
cooling fin
−
+
1
2
3
4
5
6
7
8
9
10
11
12

Fig. 1 Block diagram.

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC134)

**Voltages**

with respect to cooling fin (ground)

| | | | | |
|---|---|---|---|---|
| Supply voltage (pin 11) | $V_{11} = V_P$ | max. | 40 | V |
| Supply voltage output stage (pin 8) | $V_8$ | max. | 60 | V |
| Pin 9 | $V_9$ | max. | 60 | V |
| | $-V_9$ | max. | 0 | V |
| Pin 10 | $V_{10}$ | max. | 40 | V |
| Pin 3 | $V_3$ | max. | 7 | V |
| Pin 1 | $V_1$ | max. | 40 | V |
| Pin 6 | $V_6$ | max. | 7 | V |
| Pins 7 and 12 | $V_7; V_{12}$ | max. | 24 | V |

**Currents**

| | | | | |
|---|---|---|---|---|
| Pin 10 | $I_{10}$ | max. | 1,2 | A |
| | $-I_{10}$ | max. | 1,5 | A |
| Pin 5 | $\pm I_5$ | max. | 10 | mA |
| Pin 2 | $I_2$ | max. | 3 | mA |
| Pin 1 | $I_1$ | max. | 50 | mA |
| | $-I_1$ | max. | 0,1 | mA |
| Pin 6 | $-I_6$ | max. | 5 | mA |
| Pin 4 | $-I_4$ | max. | 1 | mA |
| Pin 8, pin 9 and cooling fin | internally limited by the short-circuit protection circuit | | | |

**Temperatures**

| | | |
|---|---|---|
| Total power dissipation | internally limited by the short-circuit protection circuit | |
| Storage temperature range | $T_{stg}$ | −55 to +150 °C |
| Operating ambient temperature range | $T_{amb}$ | −25 °C to limiting value |

## PINNING

| pin number | function | pin number | function |
|---|---|---|---|
| 1. | sawtooth capacitor | 7. | feedback input |
| 2. | frequency storage information | 8. | positive supply of output stage |
| 3. | oscillator capacitor | 9. | output |
| 4. | oscillator resistor (adjustment) | 10. | flyback generator output |
| 5. | synchronization input/blanking output | 11. | positive supply ($V_P$) |
| 6. | sawtooth buffer stage output | 12. | preamplifier input |

DEVELOPMENT SAMPLE DATA

## CHARACTERISTICS

$V_P$ = 22 V; $T_{amb}$ = 25 °C; these characteristics are measured with respect to cooling fin (ground), unless otherwise specified.

| parameter | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| **Supply voltage/output stage** | | | | | |
| Supply voltage | $V_{11} = V_P$ | 9 | – | 30 | V |
| Output voltage | | | | | |
| at $I_9$ = 0,75 A | $V_9$ | – | 1,2 | 1,4 | V |
| at $-I_9$ = 0,75 A | $V_9$ | $(V_P - 1,9)$ | $(V_P - 1,7)$ | – | V |
| Flyback generator output voltage at $I_{10}$ = 0,75 A | $V_{10}$ | – | $(V_P - 2,0)$ | – | V |
| Supply currents (without load) | | | | | |
| pin 11 | $I_{11}$ | – | 10 | – | mA |
| pin 8 | $I_8$ | – | 3 | – | mA |
| Output current | $\pm I_9$ | – | – | 1,2 | A |
| Flyback generator peak current | $\pm I_{10}$ | – | – | 1,2 | A |
| **Feedback** | | | | | |
| Preamplifier quiescent input currents | $-I_7 = -I_{12}$ | – | 0,1 | – | μA |
| **Synchronization** | | | | | |
| Sync input voltage range | $V_5$ | 1,0 | – | – | V |
| Synchronizing range | | – | 28 | – | % |
| **Oscillator/sawtooth generator** | | | | | |
| Frequency setting input voltage | $V_4$ | 6 | – | 9 | V |
| Sawtooth generator output voltage (peak value) | $V_{1(m)}$ | 0 | $(V_P - 2)$ | – | V |
| Sawtooth generator output current | $I_1$ | – | – | 30 | mA |
| Sawtooth generator leakage current | $-I_1$ | 2 | – | – | μA |
| Oscillator temperature dependency $T_{case}$ = 20 to 100 °C | $(\Delta f/f)/\Delta T_{case}$ | – | $10^{-4}$ | – | $K^{-1}$ |
| Oscillator voltage dependency $V_P$ = 10 to 30 V | $(\Delta f/f)/\Delta V_P$ | – | $10^{-3}$ | – | $V^{-1}$ |
| **Blanking pulse generator** | | | | | |
| Output voltage (at $I_5$ = 1 mA) | $V_5$ | – | 20 | – | V |
| Output resistance | $R_5$ | – | 410 | – | Ω |
| Output current (at $V_P$ = 21 V) | $-I_5$ | – | – | 5 | mA |
| Blanking pulse duration at 50 Hz sync | $t_b$ | 1,33 | 1,4 | 1,47 | ms |
| **50/60 Hz frequency detector** | | | | | |
| Output saturation voltage (LOW level for 50 Hz) | $V_2$ | – | 1 | – | V |
| Leakage current | $I_2$ | – | 1 | – | μA |

| parameter | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| **Buffer stage** | | | | | |
| Output voltage | $V_{6(m)}$ | 0 | $(V_P - 1)$ | – | V |
| Output current | $-I_6$ | – | – | 4 | mA |
| **Thermal resistance** | | | | | |
| From junction to case (cooling fin) | $R_{th\ j\text{-}c}$ | – | – | 15 | K/W |
| **Junction temperature** | | | | | |
| Switching point thermal protection | $T_j$ | 142 | 150 | 158 | °C |

## APPLICATION INFORMATION

The following application data is obtained from measurements made on the circuits shown in Figs 2 and 3, application circuits for 90° deflection systems. Measurements are made with respect to the cooling fin (ground).

DEVELOPMENT SAMPLE DATA

| | | | Fig. 2 concept 1* | Fig. 3 concept 2* | |
|---|---|---|---|---|---|
| System supply voltages | $V_{P1}$ | typ. | 22 | 22 | V |
| | $V_{P2}$ | typ. | 12 | – | V |
| Supply currents | $I_{P1}$ | typ. | 135 | 140 | mA |
| | $-I_{P2}$ | typ. | 8 | – | mA |
| Output voltage (d.c. value) | $V_9$ | typ. | 12,2 | 13,8 | V |
| Output voltage (peak-to-peak value) | $V_{9(p\text{-}p)}$ | typ. | 42 | 43 | V |
| Output current (peak value) | $-I_{9(m)}$ | typ. | 450 | 450 | mA |
| Deflection current (peak-to-peak value) | $I_{defl\ (p\text{-}p)}$ | typ. | 850 | 850 | mA |
| Flyback time | $t_{fl}$ | typ. | 0,9 | 1,0 | ms |
| Oscillator frequency adjustment without sync | $f_o$ | typ. | 46,5 | 46,5 | Hz |
| Total power dissipation per package (see note) | $P_{tot}$ | max. | 1,8 | 1,8 | W |
| Ambient temperature | $T_{amb}$ | max. | 70 | 70 | °C |
| Thermal resistance (junction to ambient) | $R_{th\ j\text{-}a}$ | max. | 40 | 40 | K/W |

*Concept 1 : with two supply voltages; concept 2 : with one supply voltage.

**Note**

Calculated with $\Delta V_{P1}$ of +5% and $\Delta R_{defl}$ of –7%.

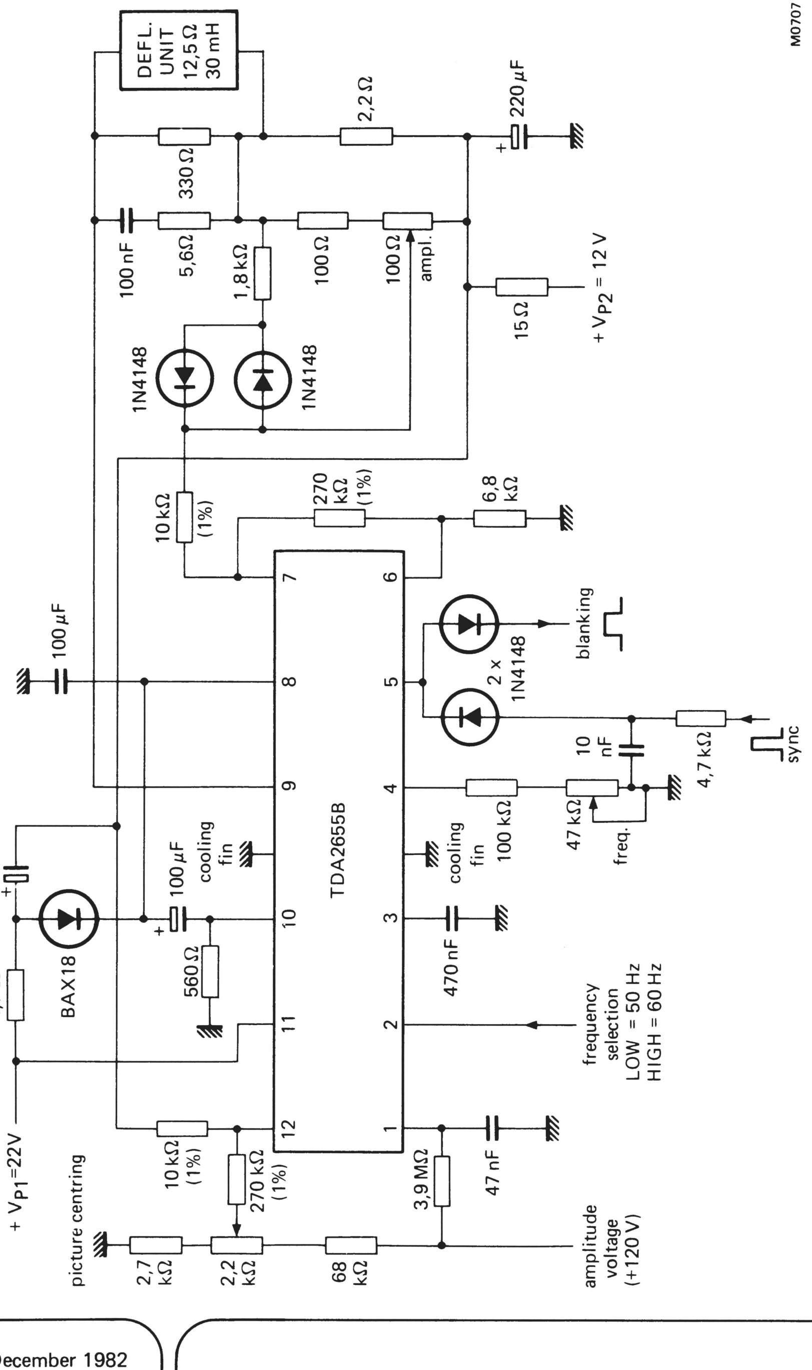

M0707
DEFL. UNIT 12,5 Ω 30 mH
330 Ω
2,2 Ω
220 μF
100 nF
5,6Ω
1,8 kΩ
100 Ω
100 Ω
ampl.
15 Ω
+ V_P2 = 12 V
1N4148
1N4148
10 kΩ (1%)
270 kΩ (1%)
6,8 kΩ
7
6
blanking
2 x 1N4148
5
8
100 μF
sync
4,7 kΩ
10 nF
9
4
100 kΩ
47 kΩ
freq.
220 μF
100 μF
cooling fin
TDA2655B
cooling fin
BAX18
10
3
560 Ω
470 nF
4,7 Ω
11
2
frequency selection LOW = 50 Hz HIGH = 60 Hz
12
1
+ V_P1 = 22V
10 kΩ (1%)
270 kΩ (1%)
3,9 MΩ
47 nF
picture centring
2,7 kΩ
2,2 kΩ
68 kΩ
amplitude voltage (+120 V)

Fig. 2 Typical application circuit with two supply voltages; for use with 90° picture tubes.

**DEVELOPMENT SAMPLE DATA**

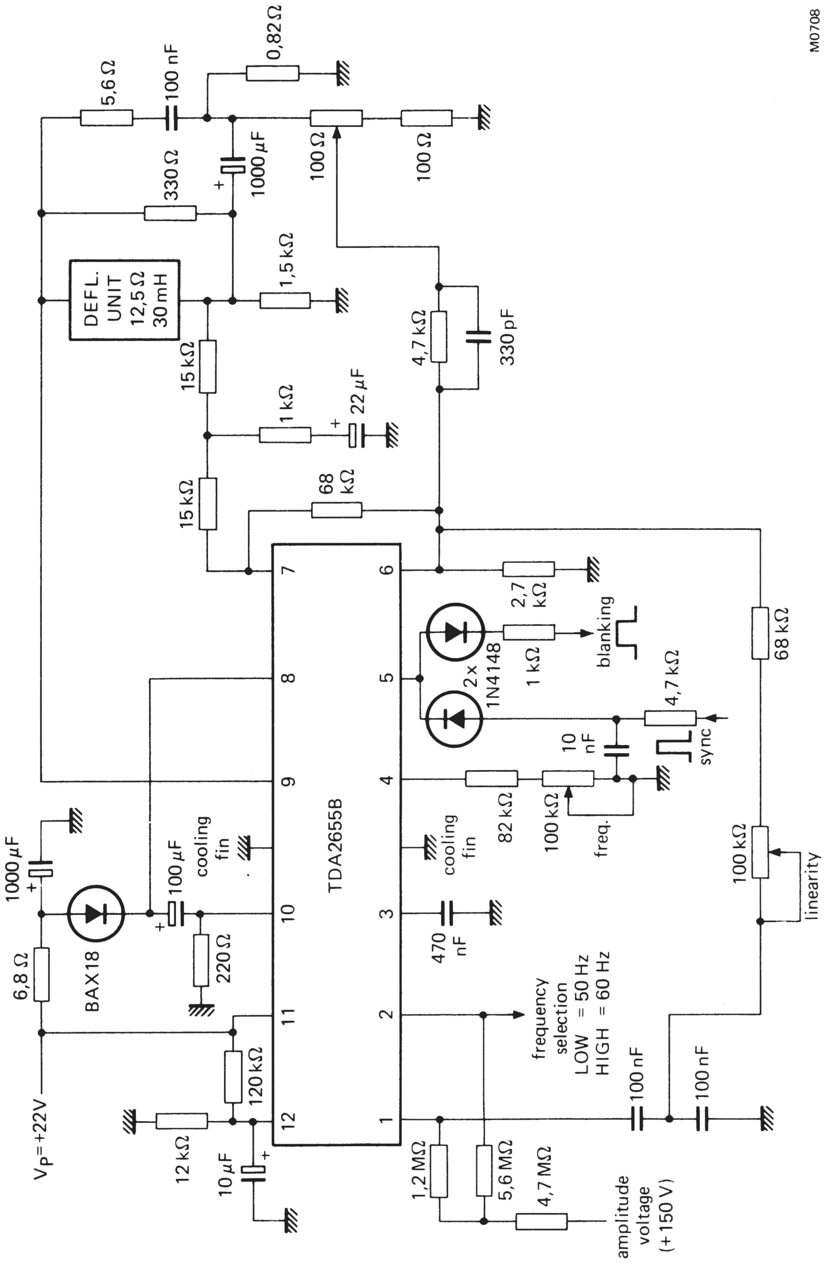

M0708
5,6 Ω
100 nF
0,82 Ω
330 Ω
1000 µF
100 Ω
100 Ω
DEFL. UNIT 12,5 Ω 30 mH
1,5 kΩ
4,7 kΩ
330 pF
15 kΩ
1 kΩ
22 µF
15 kΩ
68 kΩ
TDA2655B
2,7 kΩ
blanking
2 x 1N4148
1 kΩ
4,7 kΩ
10 nF
sync
68 kΩ
82 kΩ
100 kΩ
freq.
cooling fin
cooling fin
100 kΩ
linearity
1000 µF
BAX18
100 µF
220 Ω
6,8 Ω
470 nF
frequency selection
LOW = 50 Hz
HIGH = 60 Hz
V<sub>P</sub> = +22V
120 kΩ
12 kΩ
10 µF
100 nF
100 nF
1,2 MΩ
5,6 MΩ
4,7 MΩ
amplitude voltage (+150 V)
1
2
3
4
5
6
7
8
9
10
11
12

Fig. 3 Typical application circuit for a single supply voltage; for use with 90° picture tubes.

This information is derived from development samples made available for evaluation. It does not necessarily imply that the device will go into regular production.

# COLOUR SUB-CARRIER OSCILLATOR AND MIXER FOR VIDEO RECORDERS

## GENERAL DESCRIPTION

The TDA2721 is a monolithic integrated circuit for video recorders. The circuit incorporates the following functions:

- 8,8 MHz colour sub-carrier oscillator with 2 : 1 divider stage
- Keyed phase comparison for optimum noise behaviour
- Generation of a reference voltage and two control voltages based upon the synchronous demodulation and envelope demodulation principles respectively.
- Stage for generating the colour killer signal and an identification signal
- A mixer stage for generating the 5,06 MHz sub-carrier frequency

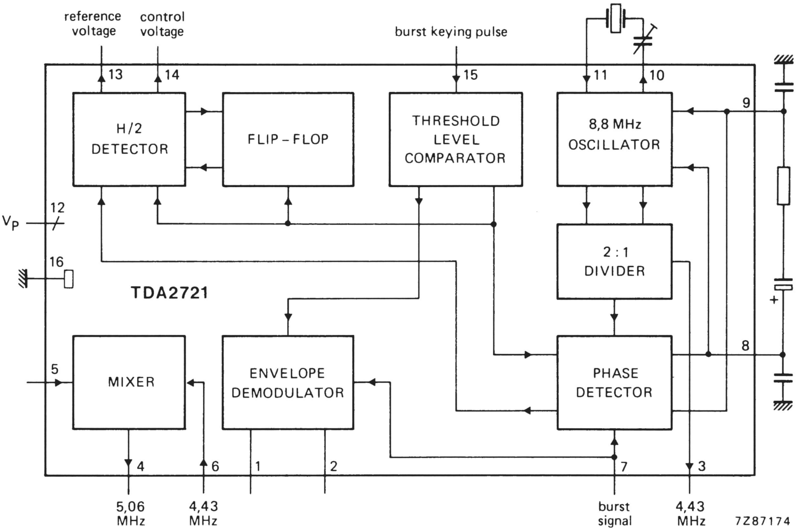

reference voltage
control voltage
burst keying pulse
13
14
15
11
10
9
H/2 DETECTOR
FLIP – FLOP
THRESHOLD LEVEL COMPARATOR
8,8 MHz OSCILLATOR
12
V_P
16
2 : 1 DIVIDER
TDA2721
+
8
5
MIXER
ENVELOPE DEMODULATOR
PHASE DETECTOR
4
6
1
2
7
3
5,06 MHz
4,43 MHz
burst signal
4,43 MHz
7Z87174

Fig. 1 Block diagram.

## PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | | |
|---|---|---|---|---|
| Supply voltage (pin 12) | $V_{12\text{-}16} = V_P$ | max. | 13,2 | V |
| Voltage at pins 1, 3 and 7 | $V_{1;3;7\text{-}16}$ | max. | 9 | V |
| Voltage range at pins 2, 5, 6, 8, 9, 14 and 15 | $V_{2;5;6;8;9;14;15\text{-}16}$ | | 0 to $V_P$ | V |
| Voltage at pins 4, 10 and 13 | $V_{4;10;13\text{-}16}$ | max. | $V_P$ | V |
| Voltage at pin 11 | $V_{11\text{-}16}$ | | 0 to ½$V_P$ | V |
| Current at pins 1, 3, 4, 10 and 13 | $-I_{1;3;4;10;13}$ | max. | 5 | mA |
| Total power dissipation | $P_{tot}$ | max. | 850 | mW |
| Storage temperature range | $T_{stg}$ | | −25 to + 125 | °C |
| Operating ambient temperature range | $T_{amb}$ | | −20 to + 70 | °C |

DEVELOPMENT SAMPLE DATA

## CHARACTERISTICS

$V_P$ = 12 V; $T_{amb}$ = 25 °C; measured in Fig. 2; a nominal burst signal of 600 mV peak to peak with a pulse width of 4 μs at pin 15; unless otherwise specified

| parameter | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| **Supply** | | | | | |
| Supply voltage range (pin 12) | $V_P$ | 10,8 | – | 13,2 | V |
| Supply current (pin 12) | $I_P$ | – | 45 | – | mA |
| **Follow-up synchronization** | | | | | |
| Catching range | Δf | 400 | – | – | Hz |
| *Oscillator* | | | | | |
| Input resistance (pin 11) | $R_{11-16}$ | – | 270 | – | Ω |
| Output resistance (pin 10) | $R_{10-16}$ | – | – | 200 | Ω |
| D.C. voltage at pin 10 | $V_{10-16}$ | – | 10 | – | V |
| D.C. voltage at pin 3 | $V_{3-16}$ | – | 3,5 | – | V |
| Output voltage at pin 3 (peak-to-peak value) | $V_{3-16(p-p)}$ | – | 600 | – | mV |
| *Phase detector* (pin 7) | | | | | |
| Input resistance | $R_{7-16}$ | – | 1,2 | – | kΩ |
| Input voltage (peak-to-peak value) | $V_{7-16(p-p)}$ | – | – | 1,2 | V |
| **Control voltage generation** | | | | | |
| *H/2 demodulator* | | | | | |
| Reference voltage (pin 13) | $V_{13-16}$ | – | 7 | – | V |
| Control voltage (pin 14) | | | | | |
| without burst | $V_{14-16}$ | – | 0 | – | V |
| at nominal burst | $V_{14-16}$ | – | 1,4 | – | V |
| Input voltage (pin 7) | $V_{7-16}$ | – | – | 1,2 | V |
| Burst keying pulse (pin 15) | $V_{15-16}$ | 8,5 | – | – | V |
| *Envelope demodulation* | | | | | |
| Output voltage (pin 4) without burst | $V_{1-16}$ | – | – | $V_{14-16}$ | V |
| Output voltage variation when changing the burst signal from 0 to 600 mV peak to peak | $\Delta V_{1-16}$ | – | –0,6 | – | V |
| Input voltage (pin 7) (peak-to-peak value) | $V_{7-16(p-p)}$ | – | – | 1 | V |
| Burst keying voltage (pin 15) | $V_{15-16}$ | 5,5 | – | – | V |
| Voltage for switching off the demodular (pin 2) | $V_{2-16}$ | – | – | 2 | V |

## CHARACTERISTICS (continued)

| parameter | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| **Mixer** | | | | | |
| Mixer gain at $V_{5\text{-}16(p\text{-}p)}$ = 250 mV | $G_v$* | – | 16 | – | dB |
| Maximum input voltage (pin 5) | $V_{5\text{-}16}$ | – | 600 | – | mV |
| Carrier suppression at pin 4 at $V_{5\text{-}16(p\text{-}p)}$ = 250 mV | $\alpha$** | 20 | – | – | dB |
| Input resistance at pin 5 | $R_{5\text{-}16}$ | – | 1 | – | kΩ |
| at pin 6 | $R_{6\text{-}16}$ | – | 2 | – | kΩ |

* The mixer gain is defined as the ratio: $V_4/V_5$ in which $V_4$ is the total voltage and $V_5$ the voltage at 625 kHz.

** The carrier suppression is defined as the ratio: $V_4/V_6$ in which $V_4$ is the voltage at 5,06 MHz and $V_6$ the voltage at 4,43 MHz.

## APPLICATION INFORMATION

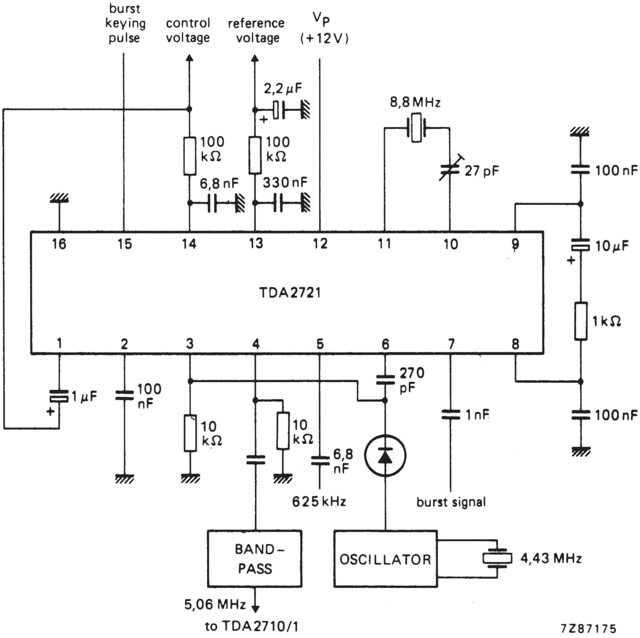

burst keying pulse
control voltage
reference voltage
$V_P$ (+12 V)
2,2 μF
100 kΩ
100 kΩ
6,8 nF
330 nF
8,8 MHz
27 pF
100 nF
10 μF
1 kΩ
100 nF
16
15
14
13
12
11
10
9
TDA2721
1
2
3
4
5
6
7
8
1 μF
100 nF
10 kΩ
10 kΩ
6,8 nF
270 pF
1 nF
625 kHz
burst signal
BAND-PASS
OSCILLATOR
4,43 MHz
5,06 MHz
to TDA2710/1
7Z87175

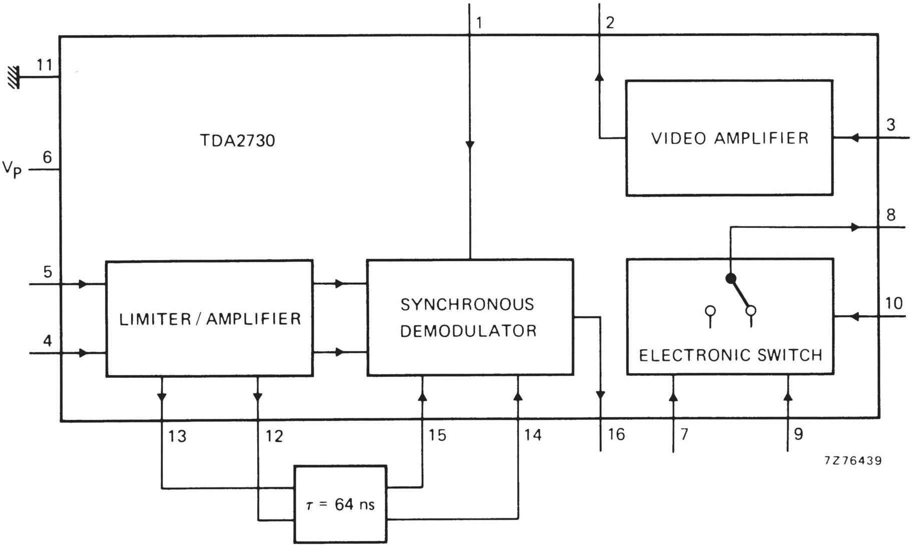
Fig. 2 Application diagram and test circuit.

# FM LIMITER/DEMODULATOR

The TDA2730 is a monolithic integrated circuit for use in audio-visual equipment, e.g.; video recorders and video disc players.
The circuit comprises an f.m. limiter/demodulator for the playback signal, a video amplifier and an electronic switch, which can be used for drop-out elimination.

| QUICK REFERENCE DATA | | | | |
|---|---|---|---|---|
| Supply voltage | $V_{6-11}$ | typ. | 12 | V |
| Supply current | $I_6$ | typ. | 42 | mA |
| Input signal range (peak-to-peak value) | $V_{4-5(p-p)}$ | | 30 to 2000 | mV |
| Video output signal (peak-to-peak value) | $V_{2-11(p-p)}$ | typ. | 4 | V |

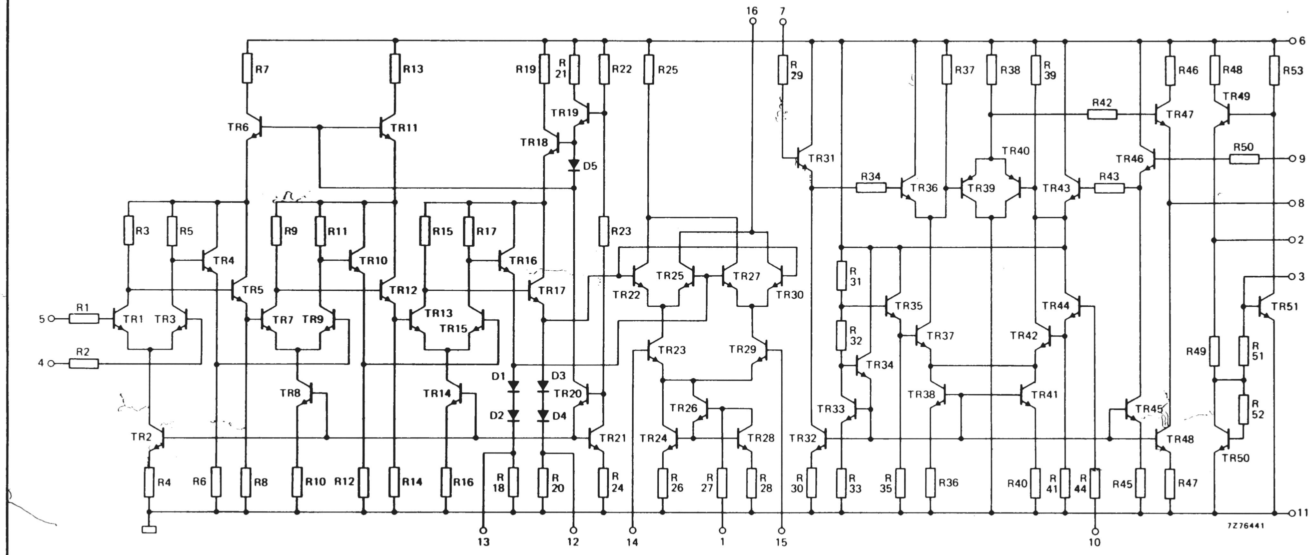
## BLOCK DIAGRAM


1
2
11
TDA2730
VIDEO AMPLIFIER
3
$V_P$
6
8
5
LIMITER / AMPLIFIER
SYNCHRONOUS DEMODULATOR
ELECTRONIC SWITCH
10
4
13
12
15
14
16
7
9
7Z76439
τ = 64 ns

## PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).

## CIRCUIT DIAGRAM


5
4
R1
R2
TR1
TR3
TR2
R4
R3
R5
TR4
TR5
R6
R7
TR6
R8
R9
R11
TR7
TR9
TR8
R10
TR10
R12
R13
TR11
TR12
R14
R15
R17
TR13
TR15
TR14
R16
TR16
TR17
R19
R21
TR18
TR19
D5
D1
D2
D3
D4
TR20
R18
R20
13
12
R22
R23
TR21
R24
R25
TR22
TR25
TR27
TR30
TR23
TR29
TR26
TR24
TR28
R26
R27
R28
14
1
15
16
7
R29
TR31
TR32
R30
R31
R32
TR33
TR34
R33
R34
TR35
R35
TR36
TR37
TR38
R36
R37
R38
TR39
TR40
R39
TR43
R43
TR44
TR42
TR41
R40
R41
R44
10
R42
TR46
TR45
R45
TR47
TR48
R46
R47
R48
TR49
R49
R50
R51
R52
TR50
TR51
R53
6
9
8
2
3
11
7Z76441

**RATINGS** Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltage

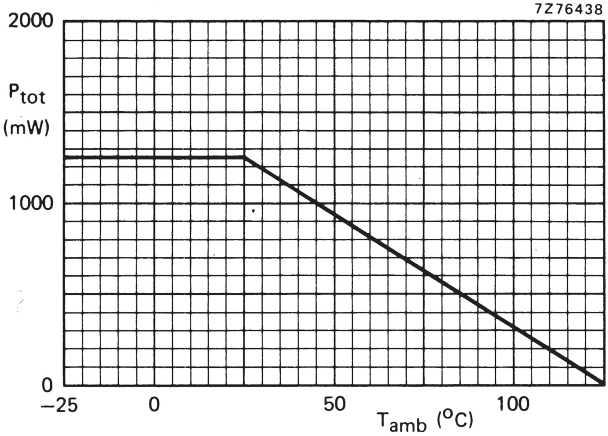
| | | | | |
|---|---|---|---|---|
| Supply voltage | $V_{6-11}$ | max. | 13 | V |

Power dissipation

| | | | | |
|---|---|---|---|---|
| Total power dissipation<br>(see also derating curve below) | $P_{tot}$ | max. | 1,25 | W |

Temperatures

| | | | | |
|---|---|---|---|---|
| Storage temperature | $T_{stg}$ | | −65 to +125 | °C |
| Operating ambient temperature | see derating curve below | | | |



**CHARACTERISTICS** measured in the circuit on page 7 (Fig. 1)

| | | | | |
|---|---|---|---|---|
| Supply voltage range | $V_{6-11}$ | typ. | 12 | V |
| | | | 11 to 13 | V |

The following characteristics are measured at $V_{6-11}$ = 12 V; $T_{amb}$ = 25 °C

| | | | | |
|---|---|---|---|---|
| Supply current | $I_6$ | typ. | 42 | mA |
| | | | 25 to 54 | mA |

**Limiter**

| | | | | |
|---|---|---|---|---|
| Start of limiting (−3 dB)<br>$f_o$ = 4 MHz; peak-to-peak value | $V_{4-5(p-p)}$ | typ. | 0, 8 | V |
| Input signal range for constant luminance output (peak-to-peak value) | $V_{4-5(p-p)}$ | | 30 to 2000 | mV |
| Output voltage (peak-to-peak value) | $V_{12-13(p-p)}$ | typ. | 750 | mV |
| Available output voltage at an external load of 1 kΩ; peak-to-peak value | $V_{12-13(p-p)}$ | > | 5 | V |

**Demodulator**

Measured at $I_1$ = 4 mA; $|Z_{16-11}|$ = 1, 5 kΩ; delay time $\tau$ = 64 ns; $\Delta f$ = 1, 4 MHz ($f_L$ = 3, 0 MHz, $f_H$ = 4, 4 MHz)

| | | | | |
|---|---|---|---|---|
| Current ratio | $I_1/I_{16}$ | typ. | 1 | |
| Output voltage (peak-to-peak value) | $V_{16-11}$ | typ. | 540 | mV |

**Drop-out switch**

| | | | | |
|---|---|---|---|---|
| Input drive voltage range | $V_{7;9-11}$ | | 6, 5 to 12 | V |
| Voltage drop between input and output | | | | |
| for signal flow from pin 7 to pin 8 | $V_{7-8}$ | typ. | 1, 5 | V |
| for signal flow from pin 9 to pin 8 | $V_{9-8}$ | typ. | 1, 5 | V |
| Input offset voltage | $\lvert V_{7-8}-V_{9-8}\rvert$ | < | 20 | mV |
| Switch actuating input voltage | | | | |
| for signal flow from pin 7 to pin 8 | $V_{10-11}$ | | 0 to 2, 7 | V |
| for signal flow from pin 9 to pin 8 | $V_{10-11}$ | | 3, 7 to 6, 0 | V |
| Output impedance at 1, 5 mA by internal load | $Z_{8-11}$ | | emitter follower | |

## CHARACTERISTICS (continued)

**Video amplifier**

| | | | | |
|---|---|---|---|---|
| Input voltage level | $V_{3-11}$ | typ. | 730 | mV |
| Output voltage level | $V_{2-11}$ | typ. | 5,5 | V |
| Open loop gain | G | typ. | 43 | dB |
| Bandwidth (3 dB) | B | typ. | 8,8 | MHz |
| Output voltage (peak-to-peak value; see note) | $V_{2-11(p-p)}$ | typ. | 4 | V |

Note

The gain of the amplifier is determined by the feedback network comprising the impedances between pins 2 and 3, and pins 8 and 3. The values quoted apply to the circuit on page 7 (Fig. 1).

## PINNING

1. Current setting demodulator
2. Video amplifier output
3. Video amplifier input
4. F.M. signal input
5. F.M. signal input
6. Positive supply
7. Switch input
8. Switch output
9. Switch input
10. Switch actuating input
11. Negative supply (ground)
12. Limiter output
13. Limiter output
14. Demodulator input
15. Demodulator input
16. Demodulator output

## APPLICATION INFORMATION

**The function is quoted against the corresponding pin number**

1. Current setting of demodulator

   The current into this pin directly **determines** the amplitude and the d.c. level of the demodulator output. At $I_1$ = 4 mA, optimum temperature compensation is obtained.

2. Video amplifier output

   A signal up to 4 V peak-to-peak is available from this output (Fig. 1).
   This can be the video signal (Fig. 1) or the f.m. signal to the delay line (drop-out elimination; Fig. 2).

3. Video amplifier input

   The demodulator output signal is the input signal to this pin (Fig. 1) or the f.m. modulated signal (Fig. 2).

4. F.M. signal input (in conjunction with pin 5)

   A frequency modulated signal of 1 V peak-to-peak is applied between pins 4 and 5. D.C. feedback from the limiter output is applied to stabilize the operation.

5. F.M. signal input

   See pin 4.

**APPLICATION INFORMATION** (continued)

6. Positive supply

   Correct operation can be obtained in the range 11 to 13 V.

7. Switch input

   The signal applied to pin 7 or to pin 9 is transferred to pin 8, depending on the switch position. For an input level between 0 and 2,7 V at pin 10, the signal at pin 7 is transferred to pin 8, and when between 3,7 and 6 V the input signal at pin 9 is transferred to pin 8.
   The signal at pin 7 or pin 9 may vary from 6,5 to 12 V.
   The signal at pin 8 is 1,5 V below the value at pin 7 or 9.
   The difference in input level at pins 7 and 9, to obtain equal output at pin 8, will be less than 20 mV.

8. Switch output

   See pin 7.

9. Switch input

   See pin 7.

10. Switch actuating input

    See pin 7.

11. Negative supply (ground)

12. Limiter output

    A balanced signal is available between pins 12 and 13. The signal amplitude is limited to 750 mV at both outputs.

13. Limiter output

    See pin 12.

14. Demodulator input

    A phase shifted signal (with respect to the internally applied signal) is applied between pins 14 and 15.

15. Demodulator input

    See pin 14.

16. Demodulator output

    The output signal is proportional to :
    - current into pin 1
    - slope of the phase characteristic of the network between pins 12 and 13, and pins 14 and 15
    - impedance level at the output
    - the sweep (Δf) of the f. m. signal.

    A signal of typically 540 mV is available at this pin when using the component values in Fig. 1 and Δf = 1,4 MHz.

## APPLICATION INFORMATION (continued)

### Test circuit

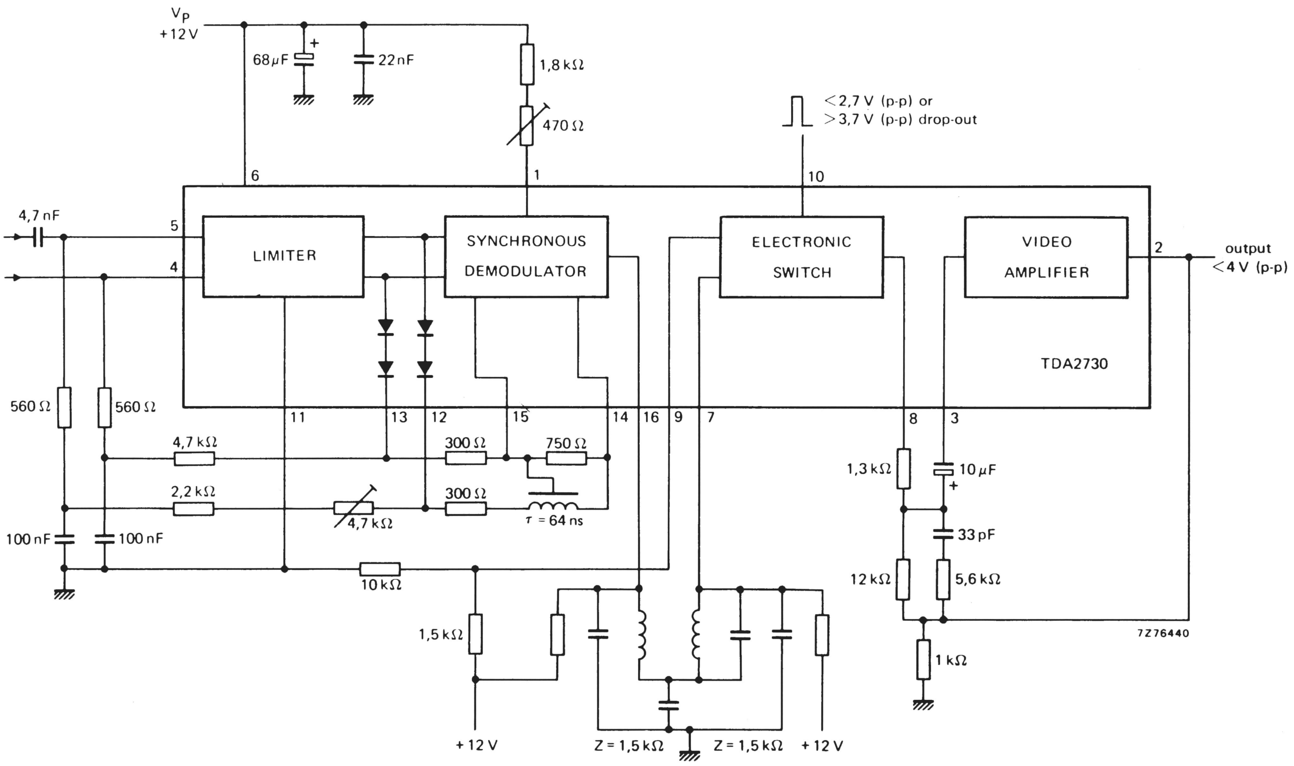

V_P
+12 V
68 μF
22 nF
1,8 kΩ
470 Ω
<2,7 V (p-p) or
>3,7 V (p-p) drop-out
6
1
10
4,7 nF
5
4
LIMITER
SYNCHRONOUS
DEMODULATOR
ELECTRONIC
SWITCH
VIDEO
AMPLIFIER
2
output
<4 V (p-p)
TDA2730
560 Ω
560 Ω
11
13
12
15
14
16
9
7
8
3
4,7 kΩ
300 Ω
750 Ω
2,2 kΩ
4,7 kΩ
300 Ω
τ = 64 ns
100 nF
100 nF
10 kΩ
1,5 kΩ
1,3 kΩ
10 μF
33 pF
12 kΩ
5,6 kΩ
1 kΩ
7Z76440
+12 V
Z = 1,5 kΩ
Z = 1,5 kΩ
+12 V

Fig. 1

## APPLICATION INFORMATION (continued)

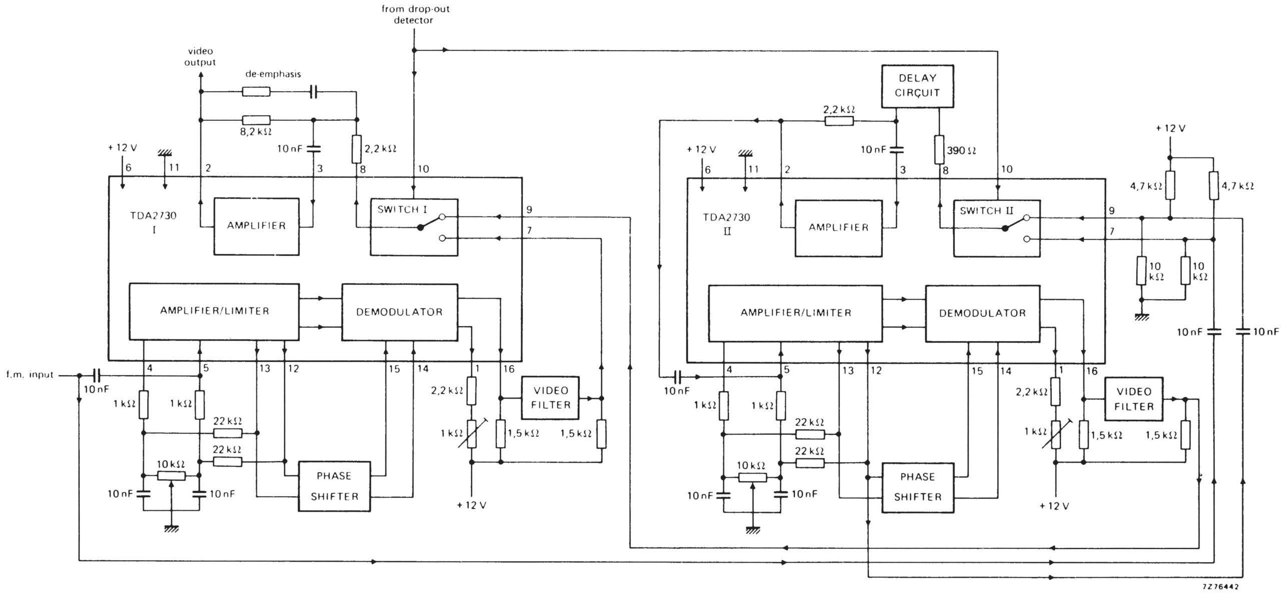

from drop-out detector
video output
de-emphasis
8,2 kΩ
10 nF
2,2 kΩ
+12 V
TDA2730 I
AMPLIFIER
SWITCH I
AMPLIFIER/LIMITER
DEMODULATOR
f.m. input
10 nF
1 kΩ
22 kΩ
10 kΩ
PHASE SHIFTER
VIDEO FILTER
1,5 kΩ
2,2 kΩ
1 kΩ
DELAY CIRÇUIT
390 Ω
TDA2730 II
SWITCH II
4,7 kΩ
10 kΩ
6
11
2
3
8
10
9
7
4
5
13
12
15
14
1
16
7Z76442

Fig. 2. Drop-out eliminator.

# AMPLIFIER AND DROP-OUT IDENTIFICATION CIRCUIT

## GENERAL DESCRIPTION

The TDA2740 is a monolithic integrated circuit intended for use in colour television receivers. It also can be used, in conjunction with the TDA2730, in the reproduction part of video recorder sets. The circuit incorporates the following functions:

- Electronic switch
- A.G.C. FM amplifier with display drive capability
- Drop-out detector
- Schmitt-trigger for generating a drop-out pulse

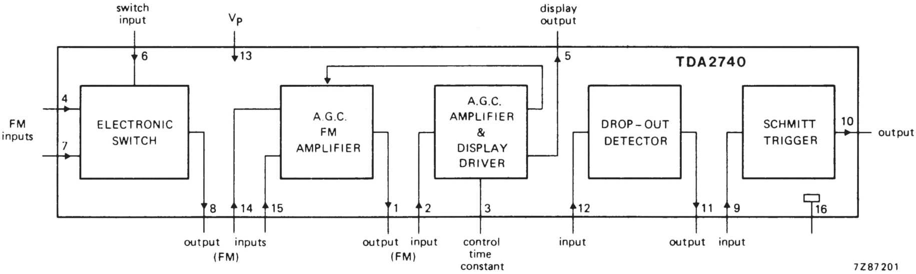

switch input
6
$V_P$
13
display output
5
TDA2740
FM inputs
4
7
ELECTRONIC SWITCH
A.G.C. FM AMPLIFIER
A.G.C. AMPLIFIER & DISPLAY DRIVER
DROP-OUT DETECTOR
SCHMITT TRIGGER
10
output
8
14
15
1
2
3
12
11
9
16
output
inputs (FM)
output
input (FM)
control time constant
input
output
input
7Z87201

Fig. 1 Block diagram.

## PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).

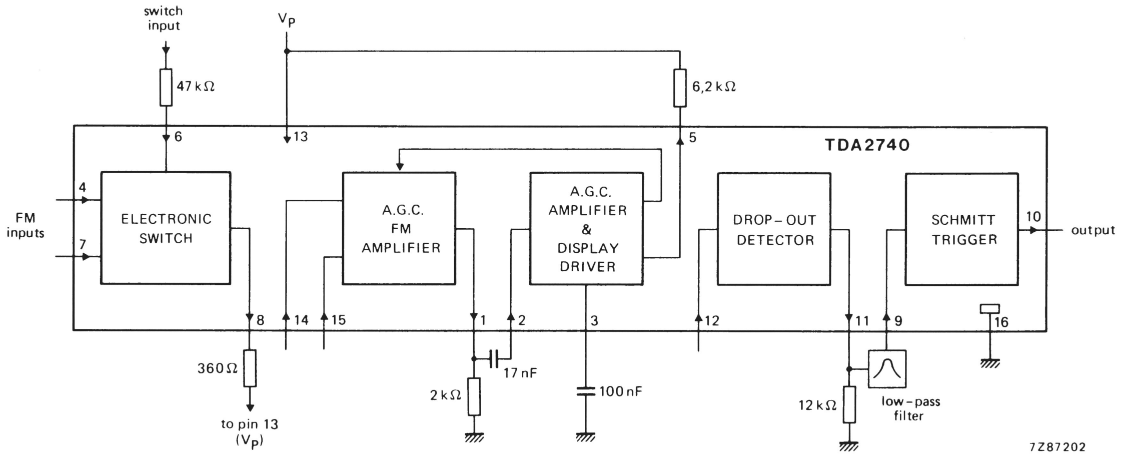

switch
input
47 kΩ
$V_P$
6,2 kΩ
6
13
5
TDA2740
4
7
FM
inputs
ELECTRONIC
SWITCH
A.G.C.
FM
AMPLIFIER
A.G.C.
AMPLIFIER
&
DISPLAY
DRIVER
DROP–OUT
DETECTOR
SCHMITT
TRIGGER
10
output
8
14
15
1
2
3
12
11
9
16
360 Ω
to pin 13
($V_P$)
17 nF
2 kΩ
100 nF
12 kΩ
low–pass
filter
7Z87202

Fig. 2 Test circuit.

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | |
|---|---|---|---|
| Supply voltage (pin 13) | $V_{13-16} = V_P$ | max. | 13 V |
| Total power dissipation | $P_{tot}$ | max. | 780 mW |
| Storage temperature range | $T_{stg}$ | | −25 to +150 °C |
| Operating ambient temperature range | $T_{amb}$ | | −20 to +90 °C |

## CHARACTERISTICS

$V_P = 12$ V; $T_{amb} = 25$ °C; measured in Fig. 2; unless otherwise specified

| parameter | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| **Supply** | | | | | |
| Supply voltage range (pin 13) | $V_P$ | 11,5 | 12 | 13 | V |
| Supply current (pin 13) | $I_P$ | 30 | 40 | 60 | mA |
| **Electronic switch** | | | | | |
| Input voltages (d.c.) | $V_{4;7-16}$ | 6,5 | 7,1 | 7,5 | V |
| Input impedances | $\lvert Z_{4;7-16}\rvert$ | – | 1 | – | kΩ |
| Input voltages (pin 6) | | | | | |
| for signal from pin 7 to pin 8 | $V_6$ | 0 | – | 1,7 | V |
| for signal from pin 4 to pin 8 | $V_6$ | 2,7 | – | $V_P$ | V |
| Input current (pin 6) | $I_6$ | – | – | 60 | μA |
| Output pin 8 | | | open collector | | |
| Output current (d.c.) | $I_8$ | 1,3 | 1,8 | 2,5 | mA |
| Output voltage | $V_{8-16}$ | 6,7 | – | $V_P$ | V |
| Forward transfer admittance | $\lvert Y_f\rvert$ | 2,45 | 3,3 | 4,45 | mS |
| 2nd harmonic suppression referred to a sinusoidal signal at pin 4 or 7 of $V_{4;7(p-p)} = 500$ mV; f = 4 MHz | $\alpha$ | – | −43 | – | dB |
| **A.G.C. amplifier and display driver** | | | | | |
| Input voltages (d.c.) | $V_{14;15-16}$ | 2,3 | 2,6 | 2,9 | V |
| Input impedance | $\lvert Z_{14-15}\rvert$ | – | 1,2 | – | kΩ |
| Input voltage range (peak-to-peak value) | $V_{14-15(p-p)}$ | 6 | – | 60 | mV |
| Output voltage (peak-to-peak value) | $V_{1(p-p)}$ | 0,7 | 1 | 1,4 | V |
| Open-loop voltage gain at f = 4 MHz | $G_{ov}$ | 43 | 46 | 49 | dB |
| Bandwidth (−3 dB) within control range | B | 7 | – | – | MHz |
| Output voltage (d.c.) | $V_{1-16}$ | 5,0 | 6,7 | 8,5 | V |
| Output impedance | $Z_{1-16}$ | | emitter follower | | |
| Input voltage (d.c.) | $V_{2-16}$ | 2,2 | 2,5 | 2,8 | V |
| Input impedance | $\lvert Z_{2-16}\rvert$ | – | 2,3 | – | kΩ |
| Output pin 5 | | | open collector | | |

**CHARACTERISTICS** (continued)

| paramter | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| **A.G.C. amplifier and display driver** (continued) | | | | | |
| Display current (pin 5) | | | | | |
| without input signal | $I_5$ | – | – | 400 | μA |
| with input signal of 60 mV (peak to peak) | $I_5$ | – | 1,3 | – | mA |
| D.C. voltage at pin 3 | | | | | |
| without input signal | $V_{3\text{-}16}$ | 1,1 | 1,5 | 1,9 | V |
| with input signal | $V_{3\text{-}16}$ | 2,4 | 2,7 | 3,2 | V |
| **Drop-out detector** | | | | | |
| Input voltage (d.c.) | $V_{12\text{-}16}$ | 2,6 | 2,8 | 3,0 | V |
| Input impedance | $\lvert Z_{12\text{-}16}\rvert$ | – | 1 | – | kΩ |
| Input voltage (a.c.) (peak-to-peak value) | | | | | |
| for negative-going threshold ($t_{PLH}$) | $V_{12(p\text{-}p)}$ | 9 | 18 | 36 | mV |
| for positive-going threshold ($t_{PHL}$) | $V_{12(p\text{-}p)}$ | 11 | 26 | 60 | mV |
| Output pin 11 | | open collector | | | |
| Maximum output current | $I_{11}$ | – | 2,3 | – | mA |
| Output current (d.c.) without input signal | $I_{11}$ | – | 1,3 | – | mA |
| **Schmitt-trigger** (see Fig. 3) | | | | | |
| Threshold voltage: ON | $V_{9\text{-}16}$ | 10,05 | 10,15 | 10,30 | V |
| Threshold voltage: OFF | $V_{9\text{-}16}$ | 9,65 | 9,80 | 9,95 | V |
| Input impedance | $\lvert Z_{9\text{-}13}\rvert$ | – | 1,2 | – | kΩ |
| Output voltage HIGH | $V_{10\text{-}16H}$ | 3,7 | 3,9 | 4,2 | V |
| Output voltage LOW | $V_{10\text{-}16L}$ | 2,1 | 2,4 | 2,7 | V |
| Output impedance | $Z_{10\text{-}16}$ | emitter follower | | | |

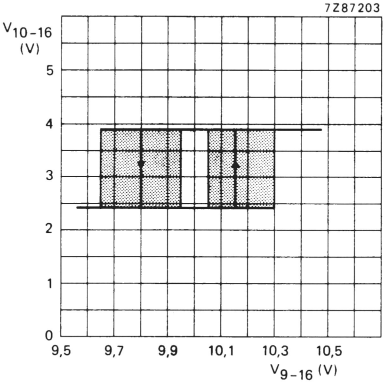


Fig. 3 Schmitt-trigger output voltage as a function of the input voltage.

# TELEVISION SOUND COMBINATION

The TDA2791 contains the following functions:

- Limiter/amplifier
- F.M. detector.
- Physiological d.c. volume control.
- D.C. tone control.

The limiter/amplifier is designed as a four-stage differential amplifier, to obtain good noise and interference suppression. The detector is a balanced quadrature demodulator.

During VTR operation audio signals can be inserted before the tone and volume control circuits. The limiter amplifier and demodulator must be switched off by grounding pin 2. This switching action occurs without a d.c. shift, so that no transients will be noticed in the speaker. The circuit is very flexible in its application because the characteristics of the various controls can be adapted by changing external component values.

## QUICK REFERENCE DATA

| | | | | |
|---|---|---|---|---|
| Supply voltage | $V_{13\text{-}3}$ | typ. | 12 | V |
| Total current drain | $I_{13}$ | typ. | 61 | mA |
| Frequency | $f_o$ | | 5,5 | MHz |
| Input voltage at start of limiting (r.m.s. value) | $V_{i(rms)}$ | typ. | 100 | μV |
| A.M. rejection at $V_i$ = 5 mV | $\alpha$ | typ. | 60 | dB |
| A.F. output voltage at $\Delta f = \pm 27$ kHz (r.m.s. value) (at pin 7 after de-emphasis) | $V_{o(rms)}$ | typ. | 700 | mV |
| D.C. bass control range | | < | + 16<br>−19 | dB |
| D.C. treble control range | | < | + 12<br>−15 | dB |
| D.C. volume control range | | > | −75 | dB |

## PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).

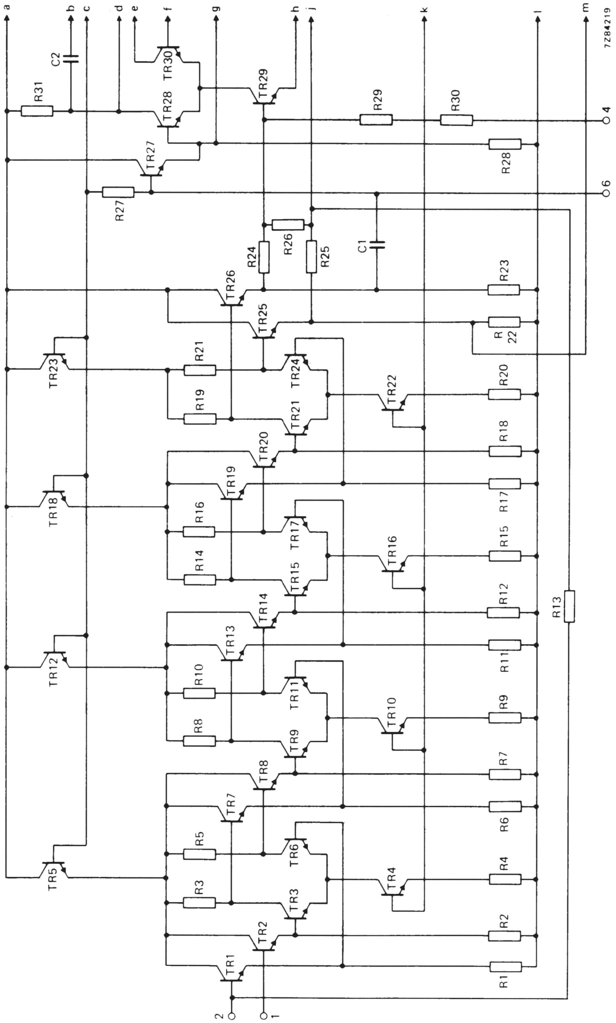

a
b
c
d
e
f
g
h
j
k
l
m
7Z84219
C2
R31
TR30
TR28
TR29
TR27
R29
R30
4
R28
R27
6
R24
R26
R25
C1
TR26
TR25
R23
R
22
TR23
R21
TR24
TR22
R20
R19
TR21
R18
TR20
TR18
TR19
R17
R16
TR17
TR16
R15
R14
TR15
R12
TR14
R13
TR12
TR13
R11
R10
TR11
TR10
R9
R8
TR9
R7
TR8
TR7
R6
R5
TR6
TR5
R4
TR4
R3
TR3
R2
TR2
R1
TR1
2
1

Fig. 1a Circuit diagram; continued in Fig. 1b.

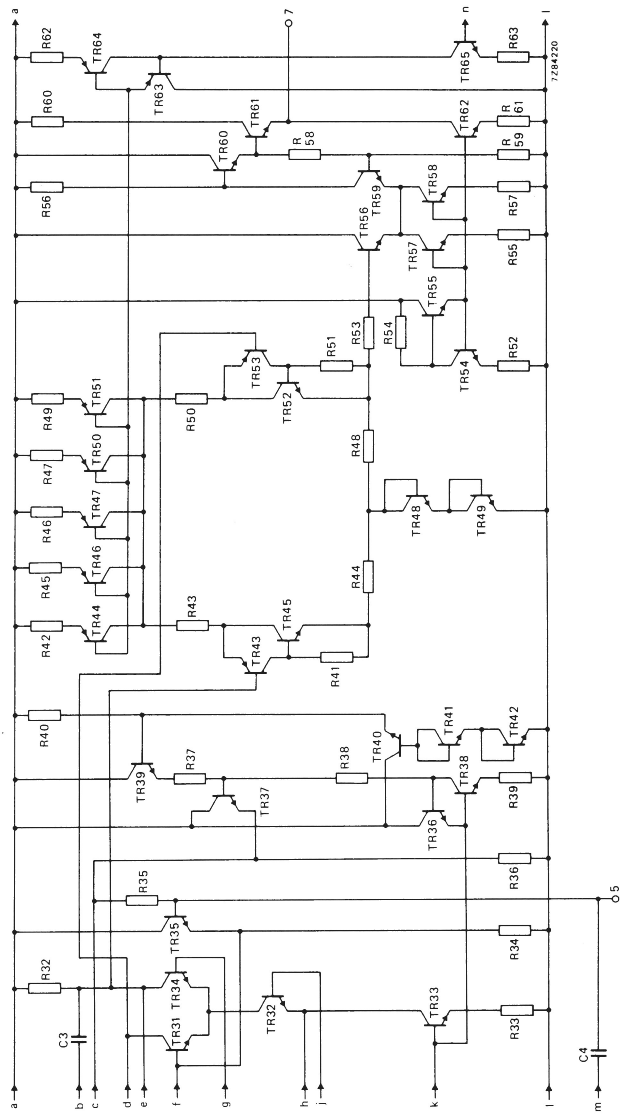

a
b
c
d
e
f
g
h
j
k
l
m
n
5
7
C3
C4
R32
R33
R34
R35
R36
R37
R38
R39
R40
R41
R42
R43
R44
R45
R46
R47
R48
R49
R50
R51
R52
R53
R54
R55
R56
R57
R 58
R 59
R60
R 61
R62
R63
TR31
TR32
TR33
TR34
TR35
TR36
TR37
TR38
TR39
TR40
TR41
TR42
TR43
TR44
TR45
TR46
TR47
TR48
TR49
TR50
TR51
TR52
TR53
TR54
TR55
TR56
TR57
TR58
TR59
TR60
TR61
TR62
TR63
TR64
TR65
7Z84220

Fig. 1b Circuit diagram; continued from Fig. 1a; continued in Fig. 1c, for line 'n' see Fig. 1d.

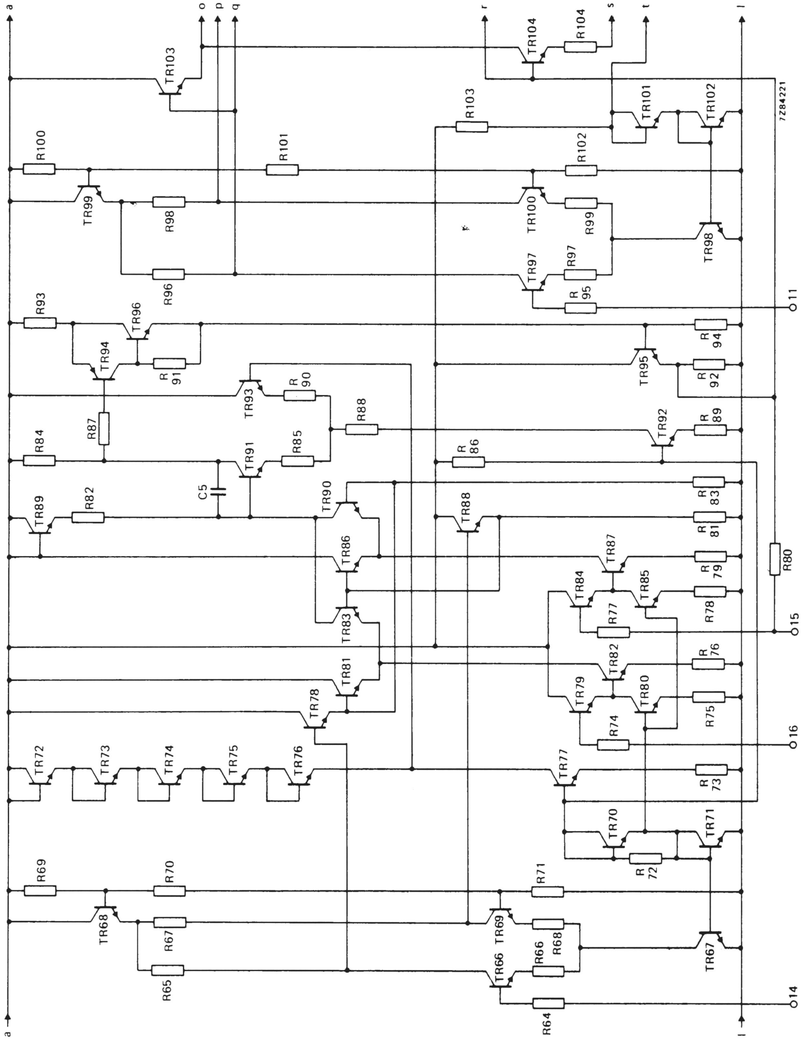

a
o
p
q
r
s
t
l
TR66
TR67
TR68
TR69
TR70
TR71
TR72
TR73
TR74
TR75
TR76
TR77
TR78
TR79
TR80
TR81
TR82
TR83
TR84
TR85
TR86
TR87
TR88
TR89
TR90
TR91
TR92
TR93
TR94
TR95
TR96
TR97
TR98
TR99
TR100
TR101
TR102
TR103
TR104
R64
R65
R66
R67
R68
R69
R70
R71
R72
R73
R74
R75
R76
R77
R78
R79
R80
R81
R82
R83
R84
R85
R86
R87
R88
R89
R90
R91
R92
R93
R94
R95
R96
R97
R98
R99
R100
R101
R102
R103
R104
C5
11
14
15
16
7Z84221

Fig. 1c Circuit diagram; continued from Fig. 1b; continued in Fig. 1d.

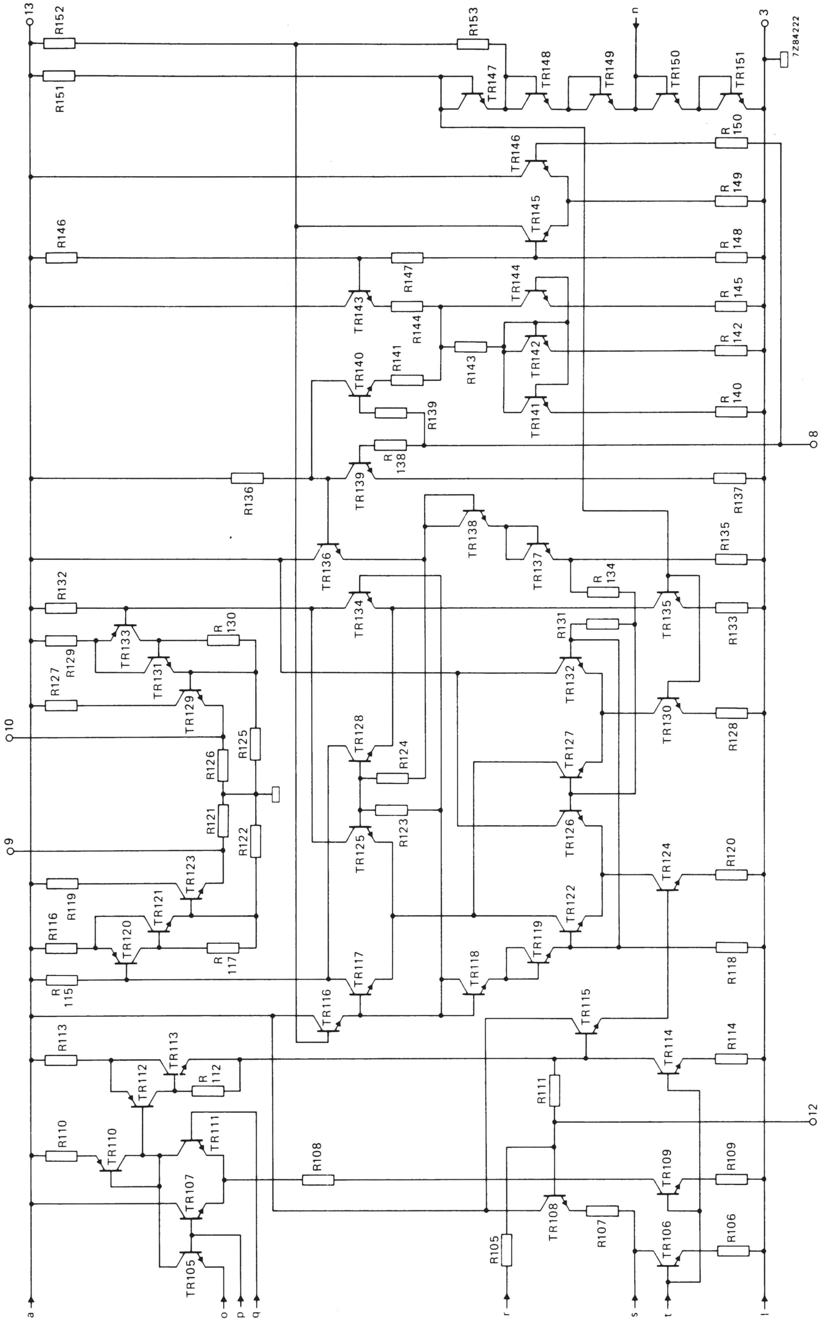

13
10
9
a
o
p
q
r
s
t
l
n
3
8
12
7Z84222
R105
R106
R107
R108
R109
R110
R111
R112
R113
R114
R115
R116
R117
R118
R119
R120
R121
R122
R123
R124
R125
R126
R127
R128
R129
R130
R131
R132
R133
R134
R135
R136
R137
R138
R139
R140
R141
R142
R143
R144
R145
R146
R147
R148
R149
R150
R151
R152
R153
TR105
TR106
TR107
TR108
TR109
TR110
TR111
TR112
TR113
TR114
TR115
TR116
TR117
TR118
TR119
TR120
TR121
TR122
TR123
TR124
TR125
TR126
TR127
TR128
TR129
TR130
TR131
TR132
TR133
TR134
TR135
TR136
TR137
TR138
TR139
TR140
TR141
TR142
TR143
TR144
TR145
TR146
TR147
TR148
TR149
TR150
TR151

Fig. 1d Circuit diagram; continued from Fig. 1c and Fig. 1b.

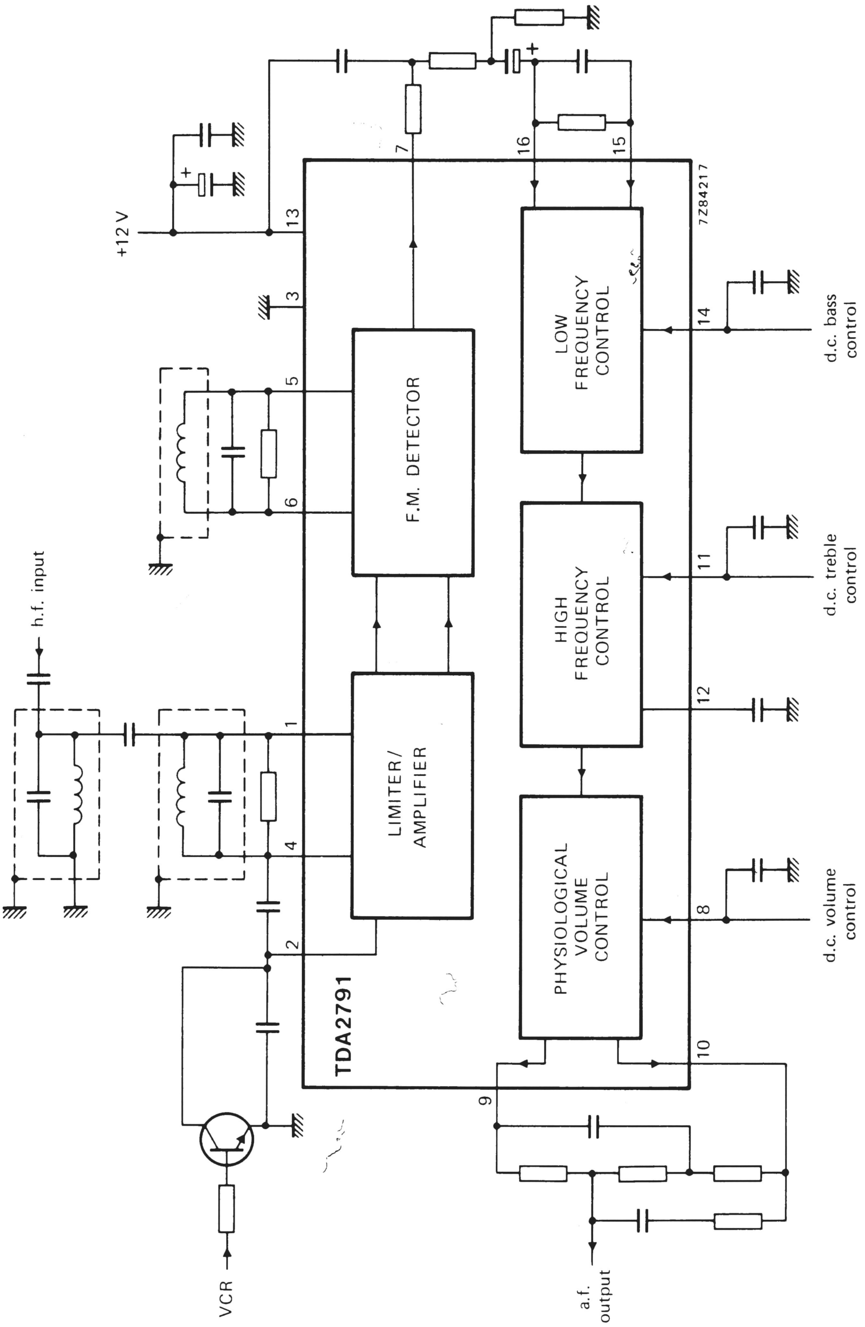

h.f. input
+12 V
13
3
5
6
1
4
2
7
16
15
14
11
12
8
10
9
LIMITER/ AMPLIFIER
F.M. DETECTOR
LOW FREQUENCY CONTROL
HIGH FREQUENCY CONTROL
PHYSIOLOGICAL VOLUME CONTROL
TDA2791
7Z84217
d.c. bass control
d.c. treble control
d.c. volume control
VCR
a.f. output

Fig. 2 Block diagram.

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | |
|---|---|---|---|
| Supply voltage | $V_{13\text{-}3}$ | max. | 13,2 V |

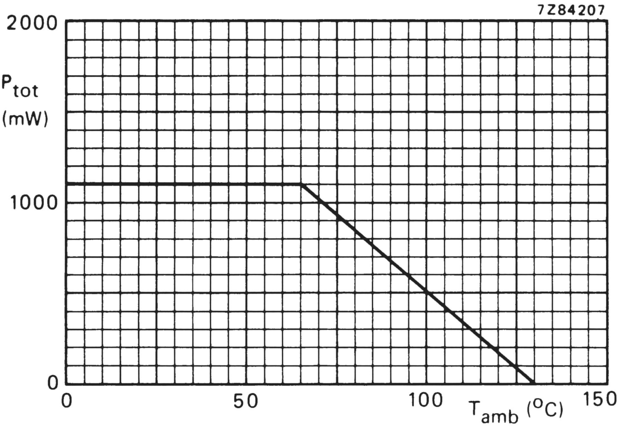


Fig. 3 Power derating curve.

| | | |
|---|---|---|
| Storage temperature | $T_{stg}$ | −25 to + 130 °C |
| Operating ambient temperature | $T_{amb}$ | −25 to + 65 °C |

## CHARACTERISTICS

Measured in Fig. 9 at $T_{amb}$ = 25 °C; $V_{13\text{-}3}$ = 12 V; f = 5,5 MHz (unless otherwise specified)

| | | | |
|---|---|---|---|
| Supply voltage range | $V_{13\text{-}3}$ | | 10,8 to 13,2 V |
| Total current drain | $I_{13}$ | | 43 to 79 mA |
| **Limiter/amplifier/demodulator** (note 1) | | | |
| Input limiting voltage at $V_{7\text{-}3}$ = −3 dB (r.m.s. value) | $V_{i(rms)}$ | typ. | 100 μV |
| Input impedance | $\lvert Z_{1\text{-}3} \rvert$ | typ. | 200 kΩ |
| A.M. rejection | | | |
| $V_i$ = 0,5 mV (note 2) | α | typ. | 50 dB |
| $V_i$ = 1 mV (note 2) | α | typ. | 50 dB |
| $V_i$ = 5 mV (note 2) | α | typ. | 60 dB |
| $V_i$ = 50 mV (note 2) | α | typ. | 55 dB |
| A.F. output voltage at pin 7 (r.m.s. value)<br>$f_m$ = 1 kHz; Δf = ± 27 kHz; $V_i$ = 5 mV; $Q_{L3}$ = 12,5 | $V_{o(rms)}$ | typ. | 700 mV |

Notes

1. The quadrature reference circuit must be tuned in such a way that there is no difference in the demodulator d.c. output voltage when the limiter input is switched from signal to no signal.
2. See test set-up Fig. 4.

**CHARACTERISTICS** (continued)

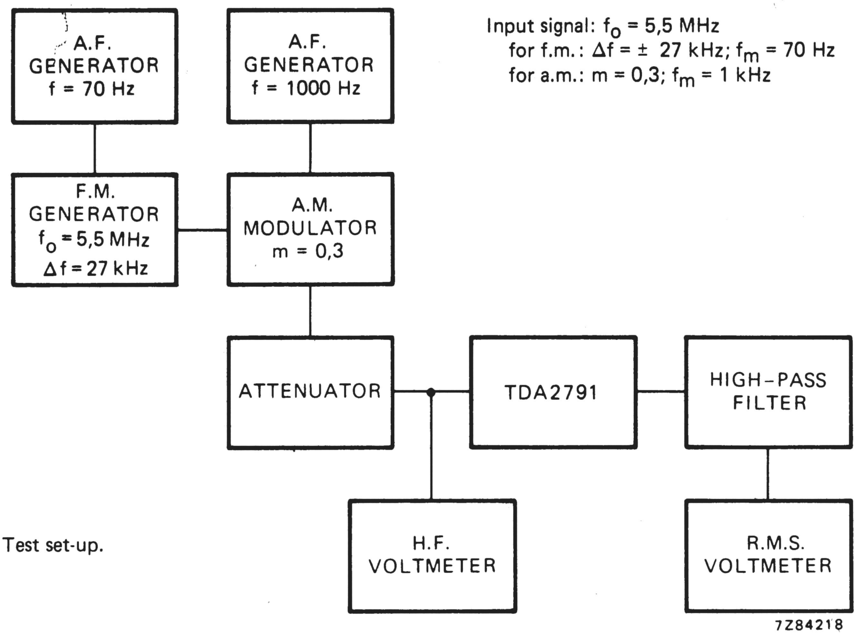
| | | | | |
|---|---|---|---|---|
| Total harmonic distortion at pin 7<br>$f_m$ = 1 kHz; Δf = ± 27 kHz; $V_i$ = 5 mV | $d_{tot}$ | typ. | 0,35 | % |
| Zero-point stability at 30 μV to 10 mV; pin 7 | | typ. | 2 | kHz |
| Hum suppression; pin 7 | | typ. | 20 | dB |
| Signal-to-noise ratio at pin 7<br>$f_m$ = 1 kHz; Δf = ± 27 kHz; $V_i$ = 5 mV (note 1) | S/N | typ. | 63 | dB |
| Demodulator output impedance | $\lvert Z_{7\text{-}3} \rvert$ | typ. | 25 | Ω |

**A.F. amplifier**

| | | | | |
|---|---|---|---|---|
| Input voltage bass control circuit at pin 16 (r.m.s. value)<br>at Δf = ± 27 kHz | $V_{i(rms)}$ | typ. | 215 | mV |
| Bass control | see graph, Fig. 5 | | | |
| Input impedance | $\lvert Z_{14\text{-}3} \rvert$ | typ. | 500 | kΩ |
| Treble control | see graph, Fig. 6 | | | |
| Input impedance | $\lvert Z_{11\text{-}3} \rvert$ | typ. | 500 | kΩ |
| Control voltages for flat frequency characteristic | $V_{11\text{-}3}$ | typ. | 3,2 | V |
| | $V_{14\text{-}3}$ | typ. | 3,2 | V |
| Volume control | see graph, Fig. 7 | | | |
| Input current at $V_{8\text{-}3}$ = 4 V | $I_8$ | typ. | 40 | μA |
| Physiological volume control (bass and treble compensation) | see graph, Fig. 8 | | | |
| Voltage gain of audio part<br>f = 1 kHz; $V_{11\text{-}3}$ = 3,2 V; $V_{14\text{-}3}$ = 3,2 V; $V_{8\text{-}3}$ = 4 V | $G_v$ | typ. | 4 | dB |
| D.C. volume control range | | > | −75 | dB |
| Weighted signal-to-noise ratio<br>$V_{i(rms)}$ = 215 mV; −24 dB volume control (notes 1 and 2) | | typ. | 56 | dB |
| Total harmonic distortion at output<br>f = 1 kHz; $V_{i(rms)}$ = 215 mV<br>(related to max. output; note 2) at:<br>0 dB | $d_{tot}$ | typ. | 0,2 | % |
| −20 dB | $d_{tot}$ | typ. | 0,4 | % |

Notes

1. Specified according to DIN 45405; weighted noise (peak value).
2. Measured at flat-tone control characteristics.


A.F.
GENERATOR
f = 70 Hz
A.F.
GENERATOR
f = 1000 Hz
F.M.
GENERATOR
$f_o$ = 5,5 MHz
Δf = 27 kHz
A.M.
MODULATOR
m = 0,3
ATTENUATOR
TDA2791
HIGH-PASS
FILTER
H.F.
VOLTMETER
R.M.S.
VOLTMETER
7Z84218

Input signal: $f_o$ = 5,5 MHz
for f.m.: Δf = ± 27 kHz; $f_m$ = 70 Hz
for a.m.: m = 0,3; $f_m$ = 1 kHz

Fig. 4 Test set-up.

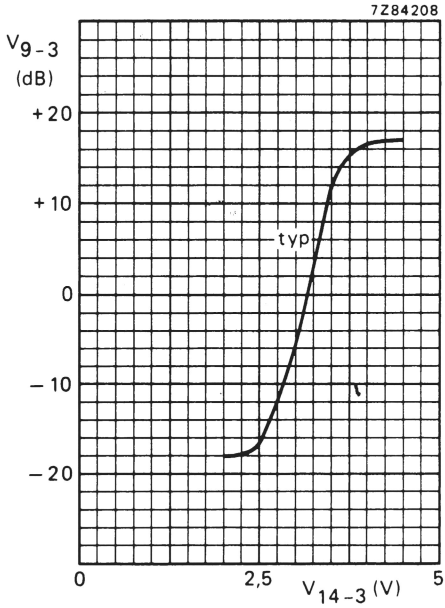


Fig. 5 Bass control curve; f = 40 Hz; $V_{11\text{-}3}$ = 3,2 V; $V_{8\text{-}3}$ = 4 V.

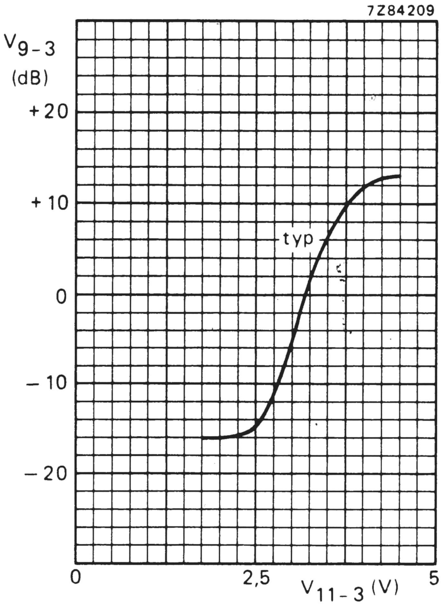
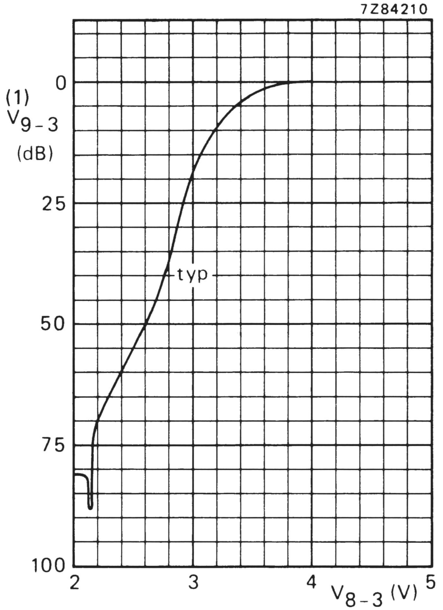
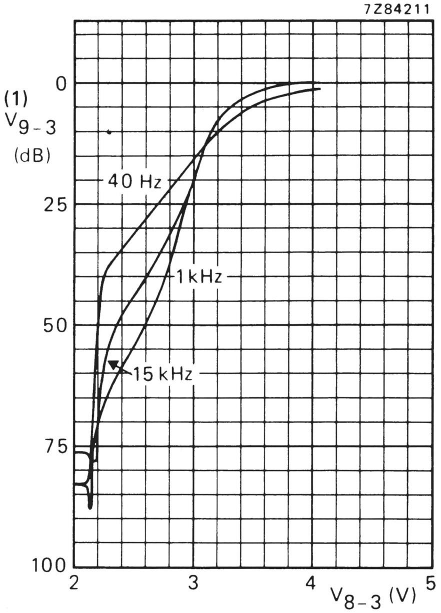


Fig. 6 Treble control curve; f = 15 kHz; $V_{14\text{-}3}$ = 3,2 V; $V_{8\text{-}3}$ = 4 V.





(1) This is actually the a.f. output voltage as shown in Fig. 9.

Fig. 7 Volume control curve; f = 1 kHz. $V_{14\text{-}3}$ = 3,2 V; $V_{11\text{-}3}$ = 3,2 V.

Fig. 8 Physiological volume control curves (typical values); $V_{14\text{-}3}$ = 3,2 V; $V_{11\text{-}3}$ = 3,2 V.

## APPLICATION INFORMATION

**The function is quoted against the corresponding pin number**

| | |
|---|---|
| 1. | Limiter input. |
| 2. | The decoupling capacitor for the internal limiter feedback is connected to this pin. |
| 3. | Negative supply (ground). |
| 4. | Limiter output for external feedback to pin 1. |
| 5 and 6. | External tank circuit (demodulator reference signal). |
| 7. | Demodulator output. |
| 8. | D.C. volume control. |
| 9 and 10. | External circuit for physiological volume control. |
| 11. | D.C. treble control. |
| 12. | External capacitor for treble control. |
| 13. | Positive supply. |
| 14. | D.C. bass control. |
| 15 and 16. | External circuit for bass control. |

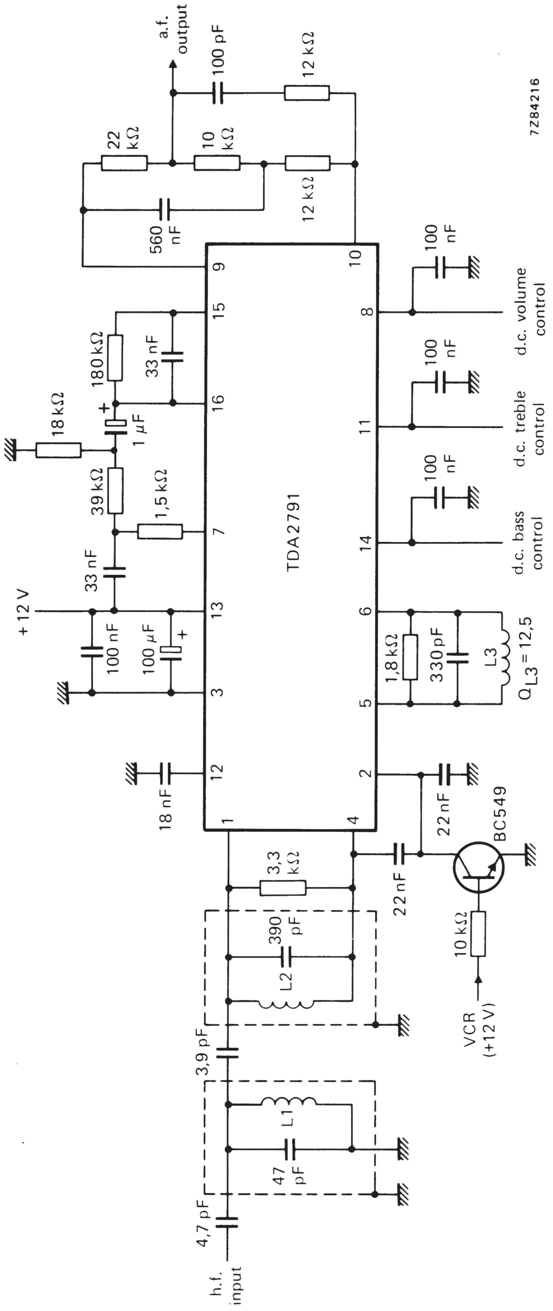

a.f. output
100 pF
12 kΩ
7Z84216
22 kΩ
10 kΩ
560 nF
12 kΩ
TDA2791
180 kΩ
33 nF
18 kΩ
1 μF
39 kΩ
1,5 kΩ
33 nF
+12 V
100 nF
100 μF
18 nF
100 nF
d.c. volume control
100 nF
d.c. treble control
100 nF
d.c. bass control
1,8 kΩ
330 pF
L3
$Q_{L3} = 12,5$
22 nF
BC549
22 nF
10 kΩ
VCR (+12 V)
3,3 kΩ
390 pF
L2
3,9 pF
L1
47 pF
4,7 pF
h.f. input
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16

Fig. 9 Application circuit diagram.

# TV STEREO/DUAL SOUND IDENTIFICATION DECODER

The TDA2795 is a monolithic integrated circuit for stereo/dual sound in television receivers.

The circuit incorporates the following functions:

- Controlled pilot signal amplifier.
- Envelope demodulator.
- Two separate signal paths for processing the identification frequencies: operational amplifier for active filter, integral evaluation circuit with TTL compatible 'open collector' outputs.
- Stereo indicator driver.

## QUICK REFERENCE DATA

| | | | | |
|---|---|---|---|---|
| Supply voltage | $V_S$ | typ. | 12 | V |
| Supply current | $I_S$ | typ. | 8 | mA |
| Nominal input voltage at f = 54,6875 kHz | $V_i$ | typ. | 10 | mV |
| Input impedance | $\|Z_i\|$ | $\geqslant$ | 500 | kΩ |
| Operational amplifier | | | | |
| open loop voltage gain at 200 Hz | $G_o$ | $\geqslant$ | 78 | dB |
| input resistance | $R_i$ | $\geqslant$ | 1 | MΩ |
| output resistance | $R_o$ | $\leqslant$ | 3,5 | kΩ |
| Supply voltage range | $V_S$ | | 10,8 to 13,2 | V |
| Operating ambient temperature range | $T_{amb}$ | | −20 to +70 | °C |

**PACKAGE OUTLINE**

18-lead DIL; plastic (SOT-102DS).

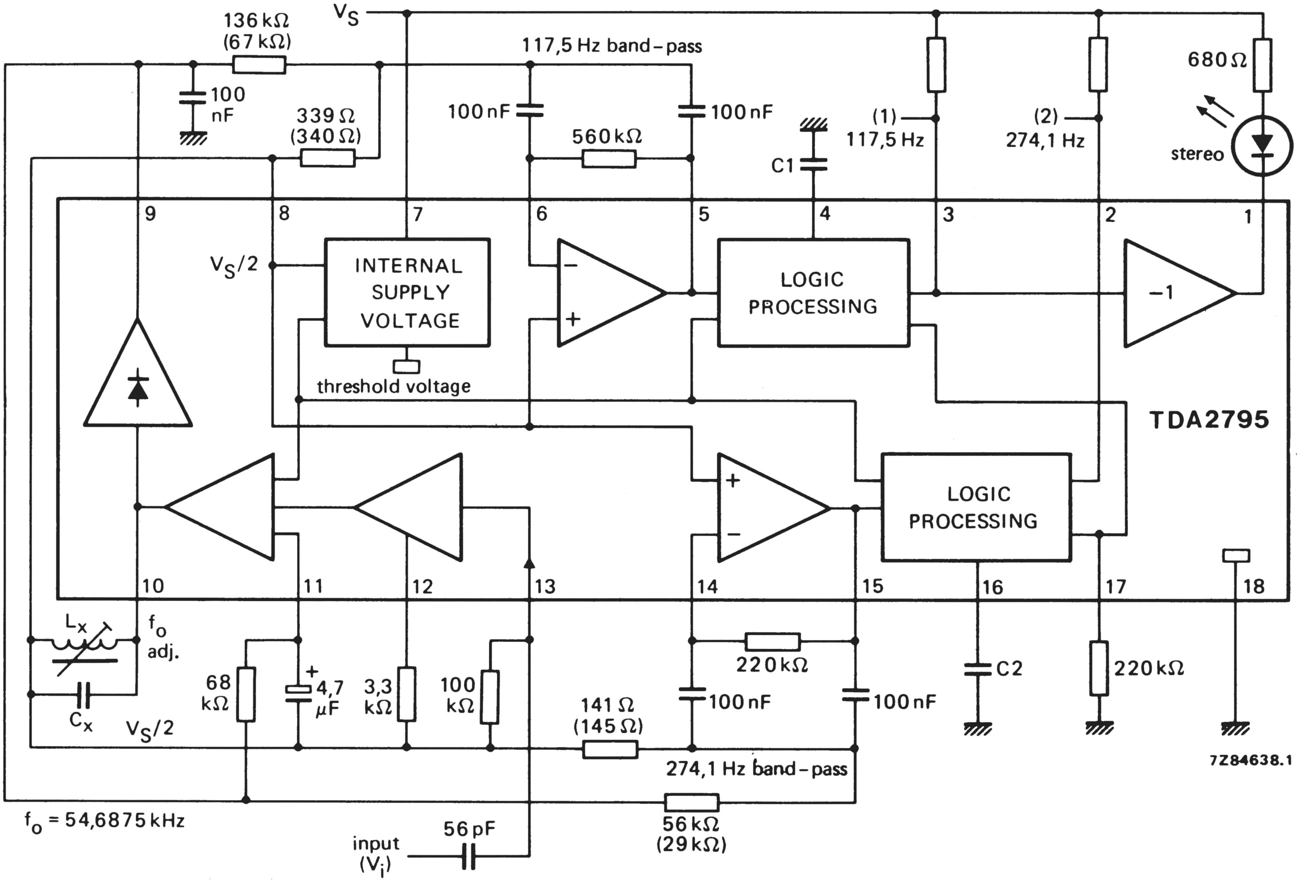

V<sub>S</sub>
136 kΩ
(67 kΩ)
100 nF
339 Ω
(340 Ω)
117,5 Hz band-pass
100 nF
560 kΩ
100 nF
C1
(1) 117,5 Hz
(2) 274,1 Hz
680 Ω
stereo
TDA2795
9
8
7
6
5
4
3
2
1
V_S/2
INTERNAL SUPPLY VOLTAGE
threshold voltage
LOGIC PROCESSING
−1
LOGIC PROCESSING
10
11
12
13
14
15
16
17
18
L_x
f_o adj.
C_x
V_S/2
68 kΩ
4,7 µF
3,3 kΩ
100 kΩ
141 Ω
(145 Ω)
220 kΩ
100 nF
100 nF
C2
220 kΩ
274,1 Hz band-pass
7Z84638.1
f_o = 54,6875 kHz
input (V_i)
56 pF
56 kΩ
(29 kΩ)

Fig. 1 Block diagram; C1 and C2 values 22 to 150 nF (dependent on switching time); values given in parenthesis are for G = 4 at 117,5/274,1 Hz; $C_x$ = 3,3 nF.

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | | |
|---|---|---|---|---|
| Supply voltage (pin 7) | $V_{7\text{-}18} = V_S$ | max. | 15 | V |
| Signal input (pin 13) | $V_{13\text{-}18}$ | max. | $V_S$ | V |
| | $-V_{13\text{-}18}$ | max. | 0,5 | V |
| Switch outputs (pins 1, 2 and 3) | $V_{1\text{-}18}$ | max. | 18 | V |
| | $I_1$ | max. | 50 | mA |
| | $V_{2;3\text{-}18}$ | max. | 15 | V |
| | $I_{2;3}$ | max. | 5 | mA |
| | $-V_{1;2;3\text{-}18}$ | max. | 0,5 | V |
| Total power dissipation | $P_{tot}$ | max. | 800 | mW |
| Storage temperature range | $T_{stg}$ | −25 to | +125 | °C |
| Operating ambient temperature range | $T_{amb}$ | −20 to | +70 | °C |

## CHARACTERISTICS

$V_S = 12$ V; $T_{amb} = 25$ °C, unless otherwise specified; measured in Fig. 1, at $V_i = 10$ mV; f = 54,6875 kHz amplitude modulated with $f_{m1} = 117{,}5$ Hz or $f_{m2} = 274{,}1$ Hz; $m_1 = m_2 = 50\%$.

| | | | | |
|---|---|---|---|---|
| Supply voltage range | $V_S$ | 10,8 to | 13,2 | V |
| Supply current | $I_S$ | typ. | 8 | mA |
| | | ⩽ | 12 | mA |

**Pilot signal amplifier and envelope demodulator**

| | | | | |
|---|---|---|---|---|
| Maximum input voltage (peak-to-peak value) | $V_{i(p\text{-}p)}$ | typ. | 2 | V |
| Input impedance | $\lvert Z_{13\text{-}18}\rvert$ | ⩾ | 500 | kΩ |
| Voltage gain ($V_{9\text{-}18}/V_{13\text{-}18}$) at $V_i = 1$ mV | $G_{v9\text{-}13}$ | typ. | 42 | dB |
| Start of control at $V_i$ | see Fig. 3 | | | |
| Control range | $\Delta G_v$ | ⩾ | 40 | dB |
| Controlled output voltage (r.m.s. value) (pin 9) | $V_{o(rms)}$ | typ. | 550 | mV |

**Operational amplifiers**

| | | | | |
|---|---|---|---|---|
| Input bias current (pins 6 and 14) | $\pm I_6; \pm I_{14}$ | ⩽ | 70 | nA |
| Open loop voltage gain at f = 200 Hz | $G_o$ | ⩾ | 78 | dB |
| Available output current (pins 5 and 15) | $\pm I_5; \pm I_{15}$ | ⩾ | 1,5 | mA |
| Output resistance (pins 5 and 15) | $R_o$ | typ. | 2 | kΩ |
| | | ⩽ | 3,5 | kΩ |
| Allowable load capacitance | $C_L$ | ⩽ | 30 | pF |
| Output offset voltage at $R_{5\text{-}6} = 560$ kΩ | $\pm V_{o5\text{-}8}$ | ⩽ | 70 | mV |

## CHARACTERISTICS (continued)

| | | | |
|---|---|---|---|
| **Evaluation circuitry** | | | |
| Switch-on threshold voltage (pins 5 and 15) | $V_5; V_{15}$ | typ. | 1,0 V |
| Switch hysteresis | $\frac{V_{5on}}{V_{5off}} = \frac{V_{15on}}{V_{15off}}$ | typ. | 3,8 ± 0,5 dB |
| Switch outputs (pins 2 and 3) | | | |
| allowable output current | $I_3; I_2$ | $\leqslant$ | 2 mA |
| saturation voltage at $I_3 = I_2 = 1,5$ mA | $V_{3;2\text{-}18sat}$ | $\leqslant$ | 0,35 V |
| leakage voltage at $I_3 = I_2 \leqslant 5\ \mu A$ | $V_{3;2\text{-}18}$ | $\leqslant$ | 15 V |
| Indicator driver (pin 1) | | | |
| allowable output current | $I_1$ | $\leqslant$ | 40 mA |
| saturation voltage at $I_1 = 20$ mA | $V_{1\text{-}18sat}$ | $\leqslant$ | 0,8 V |
| leakage voltage at $I_1 < 10\ \mu A$ | $V_{1\text{-}18}$ | $\leqslant$ | 18 V |
| **Internal reference voltage** | | | |
| Reference voltage (pin 8) | $V_{8\text{-}18}$ | typ. | 6 V |
| Available output current (pin 8) | $-I_8$ | $\geqslant$ | 2 mA |
| | $+I_8$ | $\geqslant$ | 0,6 mA |
| **Reference current source** | | | |
| Reference voltage (pin 17) | $V_{17\text{-}18}$ | typ. | 5,3 V |
| Internal bias resistor | $R_{i17}$ | typ. | 5 kΩ |
| Allowable load resistor (pin 17) | $R_L$ | | 180 to 270 kΩ |

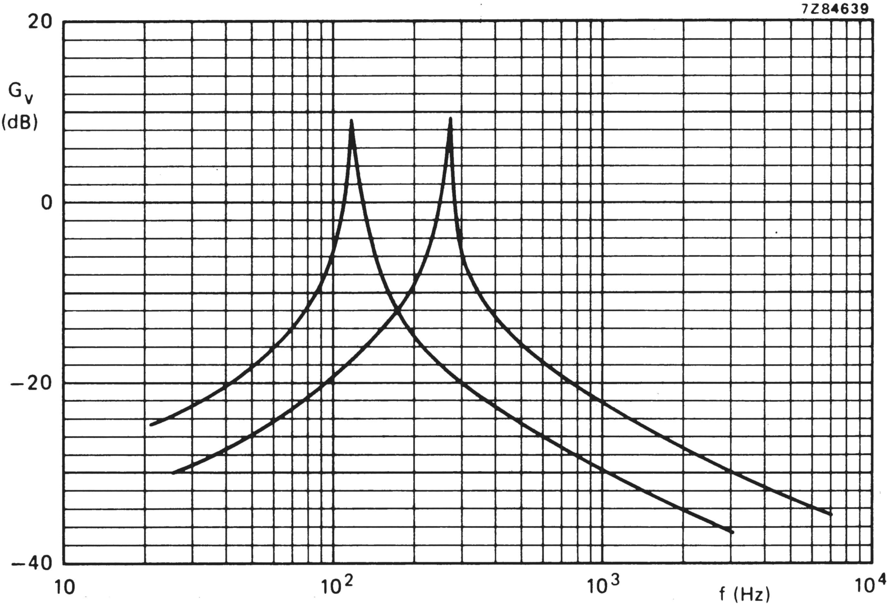


Fig. 2 Band-pass curves for 117,5 Hz and 274,1 Hz.

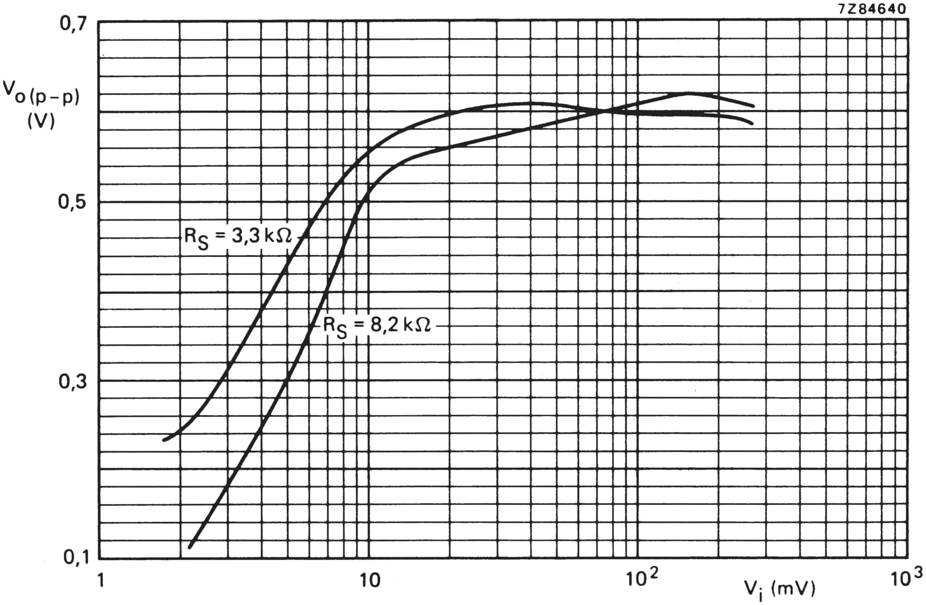


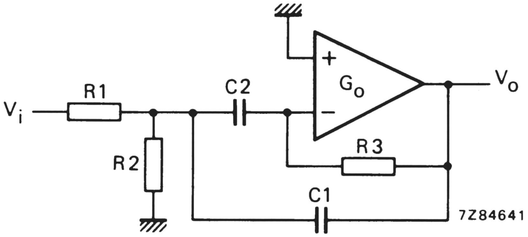
Fig. 3 Controlled output voltage as a function of the input signal ($Q_o$ = 80); pilot frequency $f_o$ = 54,6875 kHz; $R_S$ is source resistance.

## GENERAL FILTER CALCULATIONS

1. Gain

Amplifier conditions: $G_o >> G_v$ and $G_o >> 2 \cdot Q^2$

$$G_v = -\frac{\dfrac{p}{R1 \cdot C1}}{p^2 + p\dfrac{C1 + C2}{R3 \cdot C1 \cdot C2} + \dfrac{R1 + R2}{R1 \cdot R2 \cdot R3 \cdot C1 \cdot C2}}\text{, in which: } p = j\omega;\ G_v = \frac{V_o}{V_i}$$



2. Resonance frequency

$$\omega_r = \frac{1}{\sqrt{\dfrac{R1 \cdot R2}{R1 + R2} \cdot R3 \cdot C1 \cdot C2}}$$

3. Gain at $\omega = \omega_r$

$$-G_{vr} = \frac{C2}{C1 + C2} \cdot \frac{R3}{R1}$$

4. Quality

$$Q = \frac{\sqrt{C1 \cdot C2}}{C1 + C2} \cdot \sqrt{\frac{R3\,(R1 + R2)}{R1 \cdot R2}}$$

5. Recommended components

| | |
|---|---|
| C1 and C2: | 5% MKC (metallized polycarbonate film capacitor) |
| R1, R2 and R3: | 2% MR (metal film resistor) |

or:

| | |
|---|---|
| C1 and C2: | 5% MKT (metallized polyester film capacitor) |
| R1, R2 and R3: | 2% CR (carbon film resistor) |

# INFRARED RECEIVERS

## GENERAL DESCRIPTION

The TDA3047 and TDA3048 are monolithic integrated circuits for infrared reception with low power consumption. The difference between them is the polarity of the output signal. The ICs combine the following functions:

- Amplifier with a control range of 66 dB
- Synchronous demodulator and reference amplifier
- A.G.C. detector
- Pulse shaper
- Q-factor killing of the input selectivity, which is controlled by the a.g.c. circuit
- Input voltage limiter

## FUNCTIONAL DESCRIPTION

### Amplifier

The input signal is amplified by the gain-controlled amplifier. The output signal of the amplifier is applied to the synchronous demodulator inputs and to the reference amplifier.

### Reference amplifier

The reference amplifier amplifies and limits the input signal. The output signal of this amplifier is applied to the synchronous demodulator.

### Synchronous demodulator

The input signal and reference signal are multiplied in the synchronous demodulator. The output signal of the demodulator is applied to the input of a pulse-shaper circuit and to the input of the a.g.c. circuit.

### A.G.C. circuit

The output signal of the synchronous demodulator is applied to the a.g.c. circuit. The top level of the signal is detected by the a.g.c. detector. Noise pulses are integrated by an internal capacitor. The output signal from the a.g.c. detector is amplified and applied to the first and second stages of the amplifier and to the Q-factor killing circuit.

**A COMPLETE DATA SHEET IS AVAILABLE UPON REQUEST**

## FUNCTIONAL DESCRIPTION (continued)

### Pulse-shaper circuit

The output of the synchronous demodulator is also applied to the pulse-shaper circuit. The slicing level of the pulse shaper is lower than the slicing level of the a.g.c. detector. The output of the pulse shaper is applied to the output buffer.

### Output buffer

The output buffer gives an active high level for the *TDA3047* and, for the *TDA3048,* an active low level on the output pin. To obtain a correct RC-5 code, a hysteresis circuit protects the output against spikes.

### Q-factor killing circuit

In the narrow-band application it is necessary to decrease the Q-factor of the input selectivity particularly when large signals occur at the input. The output of the Q-factor killing circuit can be directly coupled to the input.

### Input voltage limiter

In the narrow-band applications high voltage peaks can occur on the input selectivity circuit. The input limiter limits these voltage peaks to about 0,7 V.

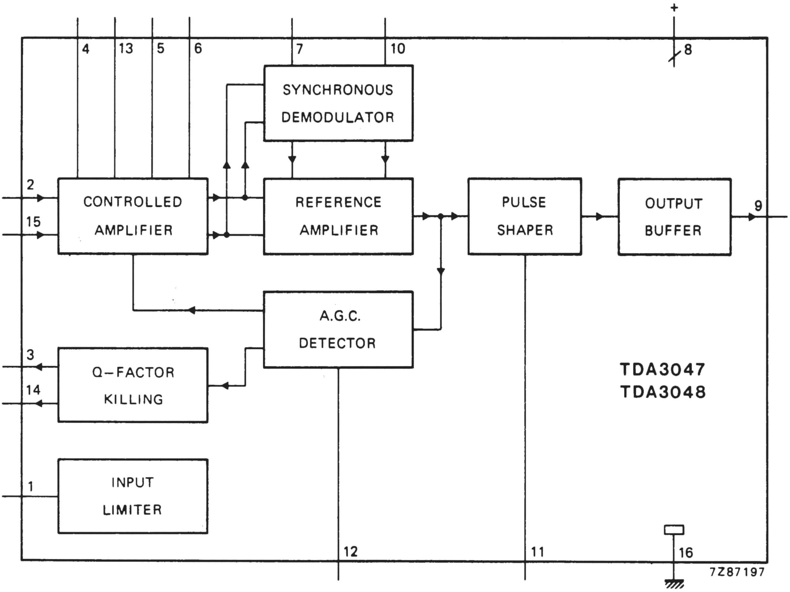

4
13
5
6
7
10
+
8
SYNCHRONOUS DEMODULATOR
2
15
CONTROLLED AMPLIFIER
REFERENCE AMPLIFIER
PULSE SHAPER
OUTPUT BUFFER
9
A.G.C. DETECTOR
3
14
Q–FACTOR KILLING
TDA3047
TDA3048
1
INPUT LIMITER
12
11
16
7Z87197

Fig. 1 Block diagram.

# VIDEO CONTROL COMBINATION

The TDA3500 is a monolithic integrated circuit performing the control functions in a PAL/SECAM decoder which additionally comprises the integrated circuits TDA3510 (PAL decoder) and/or TDA3520 (SECAM decoder).
The required input signals are: luminance and colour difference –(R-Y) and –(B-Y), while linear RGB signals can be inserted from an external source.
RGB signals are provided at the output to drive the video output stages.
The TDA3500 has the following features:

- capacitive coupling of the input signals
- linear saturation control
- (G-Y) and RGB matrix
- insertion possibility of linear RGB signals, e.g. video text, video games, picture-in-picture, camera or slide-scanner
- equal black level for inserted and matrixed signals by clamping
- 3 identical channels for the RGB signals
- linear contrast and brightness control, operating on both the inserted and matrixed RGB signals
- horizontal and vertical blanking (black and ultra-black respectively) and black-level clamping obtained via a 3-level sandcastle pulse
- differential amplifiers with feedback-inputs for stabilization of the RGB output stages
- 3 d.c. gain controls for the RGB output signals (white point adjustment)

## QUICK REFERENCE DATA

| | | | | |
|---|---|---|---|---|
| Supply voltage | $V_{6-24}$ | typ. | 12 | V |
| Supply current | $I_6$ | typ. | 100 | mA |
| Luminance input signal (peak-to-peak value) | $V_{15-24(p-p)}$ | typ. | 0,45 | V |
| Luminance input resistance | $R_{15-24}$ | typ. | 12 | kΩ |
| Colour difference input signals (peak-to-peak values) | | | | |
| –(B-Y) | $V_{18-24(p-p)}$ | typ. | 1,33 | V |
| –(R-Y) | $V_{17-24(p-p)}$ | typ. | 1,05 | V |
| Inserted RGB signals (peak-to-peak values) | $V_{12,13,14-24(p-p)}$ | typ. | 1 | V |
| Three-level sandcastle pulse detector | $V_{10-24}$ | typ. | 2,5/4,5/8,0 | V |
| Control voltage ranges | | | | |
| brightness | $V_{20-24}$ | | 1 to 3 | V |
| contrast | $V_{19-24}$ | | 2 to 4 | V |
| saturation | $V_{16-24}$ | | 2,1 to 4 | V |

## PACKAGE OUTLINE

28-lead DIL; plastic (SOT-117).

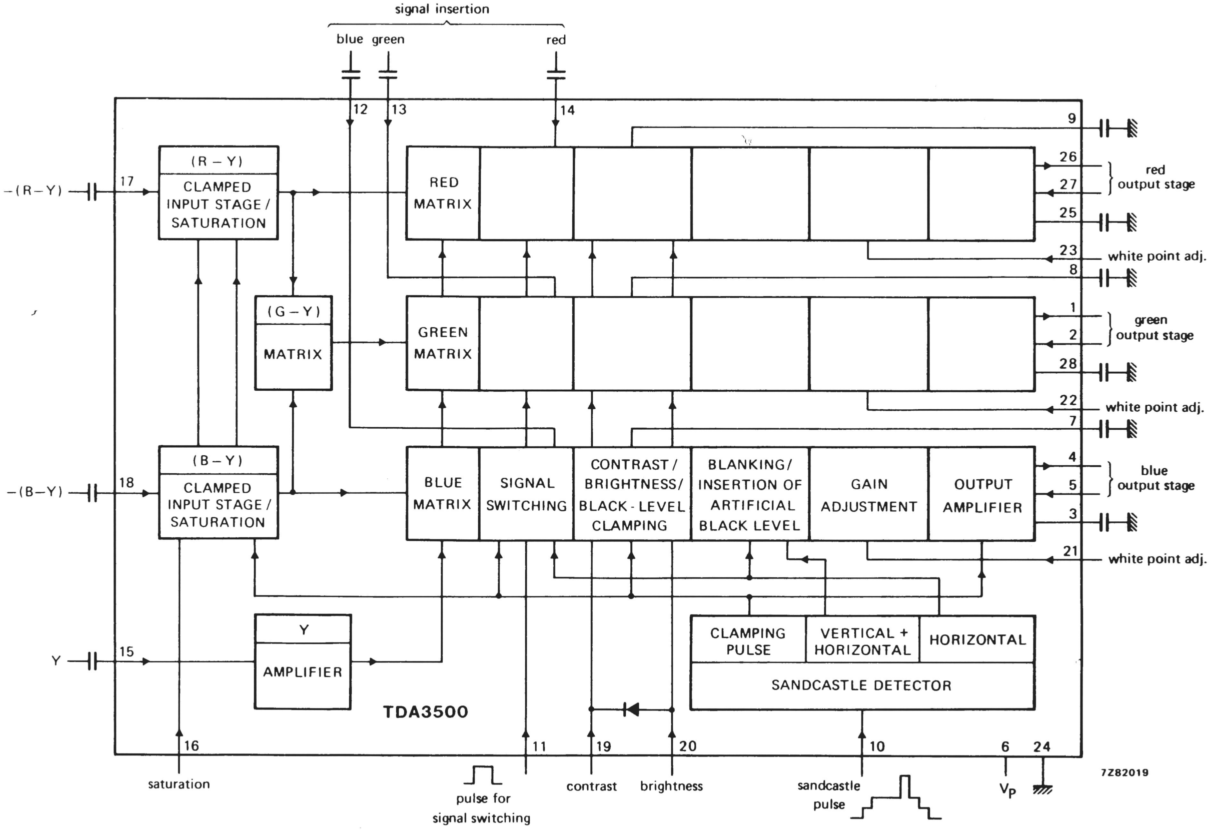

signal insertion
blue
green
red
12
13
14
9
26
27
25
23
8
1
2
28
22
7
4
5
3
21
red output stage
green output stage
blue output stage
white point adj.
white point adj.
white point adj.
−(R−Y)
17
(R − Y)
CLAMPED INPUT STAGE / SATURATION
(G − Y)
MATRIX
−(B−Y)
18
(B − Y)
CLAMPED INPUT STAGE / SATURATION
Y
15
Y
AMPLIFIER
RED MATRIX
GREEN MATRIX
BLUE MATRIX
SIGNAL SWITCHING
CONTRAST / BRIGHTNESS / BLACK - LEVEL CLAMPING
BLANKING / INSERTION OF ARTIFICIAL BLACK LEVEL
GAIN ADJUSTMENT
OUTPUT AMPLIFIER
CLAMPING PULSE
VERTICAL + HORIZONTAL
HORIZONTAL
SANDCASTLE DETECTOR
TDA3500
16
11
19
20
10
6
24
saturation
pulse for signal switching
contrast
brightness
sandcastle pulse
V_P
7Z82019

Fig. 1 Block diagram.

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | min. | max. | |
|---|---|---|---|---|---|
| Supply voltage | $V_P = V_{6-24}$ | | – | 13,2 | V |
| Voltages with respect to pin 24 | | | | | |
| pins 1,4,26 | $V_{1,4,26-24}$ | | ½$V_P$ | $V_P$ + 1 | V |
| pins 2,5,27 | $V_{2,5,27-24}$ | | 0 | $V_P$ | V |
| pin 10 | $V_{10-24}$ | | 0 | $V_P$ | V |
| pin 11 | $V_{11-24}$ | | –0,5 | 3 | V |
| pins 16,19,20 | $V_{16,19,20-24}$ | | 0 | ½$V_P$ | V |
| pins 21,22,23 | $V_{21,22,23-24}$ | | 0 | $V_P$ | V |
| pins 3,25,28; 7,8,9; 12,13,14; 15,17,18 | no external d.c. voltage | | | | |
| Current at pin 20 | $I_{20}$ | max. | | 5 | mA |
| Total power dissipation | $P_{tot}$ | max. | | 1,7 | W |
| Storage temperature | $T_{stg}$ | | | –25 to + 125 | °C |
| Operating ambient temperature | $T_{amb}$ | | | –20 to + 70 | °C |

## CHARACTERISTICS

| | | | | |
|---|---|---|---|---|
| Supply voltage range | $V_P$ | | 10,8 to 13,2 | V |

The following characteristics are measured in Fig. 2; $V_P$ = 12 V; $T_{amb}$ = 25 °C; $V_{18-24(p-p)}$ = 1,33 V; $V_{17-24(p-p)}$ = 1,05 V; $V_{15-24(p-p)}$ = 0,45 V; $V_{12,13,14-24(p-p)}$ = 1 V; unless otherwise specified

| | | | | |
|---|---|---|---|---|
| Current consumption | $I_6$ | typ. | 100 | mA |
| **Colour difference inputs** | | | | |
| –(B-Y) input signal (peak-to-peak value)* | $V_{18-24(p-p)}$ | | 1,33 | V |
| –(R-Y) input signal (peak-to-peak value)* | $V_{17-24(p-p)}$ | | 1,05 | V |
| Internal resistance of colour difference sources | | < | 200 | Ω |
| Input resistance | $R_{17,18-24}$ | > | 100 | kΩ |
| Internal d.c. voltage due to clamping | $V_{17,18-24}$ | typ. | 4,2 | V |
| Saturation control | | | | |
| control voltage range for a change of saturation from –20 dB to + 6 dB | $V_{16-24}$ | | 2,1 to 4 | V |
| control voltage for attenuation > 40 dB | $V_{16-24}$ | < | 1,8 | V |
| nominal saturation (6 dB below max.) | $V_{16-24}$ | typ. | 3 | V |
| input current | $I_{16}$ | < | 20 | μA |

---

* For saturated colour bar with 75% of maximum amplitude.

## CHARACTERISTICS (continued)

### (G-Y) matrix

Matrixed according the equation $V_{(G-Y)} = -0{,}51\ V_{(R-Y)} -0{,}19\ V_{(B-Y)}$

### Luminance amplifier

| | | | | |
|---|---|---|---|---|
| Input signal (peak-to-peak) | $V_{15-24(p-p)}$ | | 0,45 | V |
| Input resistance | $R_{15-24}$ | typ. | 12 | kΩ |
| Internal d.c. voltage | $V_{15-24}$ | typ. | 2,7 | V |

### RGB channels

| | | | | |
|---|---|---|---|---|
| Signal switching input voltage for insertion | | | | |
| on level | $V_{11-24}$ | | 0,9 to 1,5 | V |
| off level | $V_{11-24}$ | | −0,5 to 0,3 | V |
| Input current | $I_{11}$ | | −100 to + 200 | μA |
| Signal insertion | | | | |
| external RGB input signal (peak-to-peak value)* | $V_{12,13,14-24(p-p)}$ | | 1 | V |
| internal d.c. voltage due to clamping | $V_{12,13,14-24}$ | typ. | 3,5 | V |
| input current | $I_{12,13,14}$ | < | 5 | μA |
| Contrast control | | | | |
| control voltage range for a change of contrast from −17 dB to + 3 dB | $V_{19-24}$ | | 2 to 4 | V |
| nominal contrast (3 dB below max.) | $V_{19-24}$ | typ. | 3,4 | V |
| control voltage for −6 dB | $V_{19-24}$ | typ. | 2,7 | V |
| input current | $I_{19}$ | < | 10 | μA |
| Brightness control | | | | |
| control voltage range | $V_{20-24}$ | | 1 to 3 | V |
| nominal brightness voltage | $V_{20-24}$ | | 2 | V |
| input current | $I_{20}$ | < | 10 | μA |
| control voltage for nominal black level which equals the inserted artificial black level | $V_{20-24}$ | typ. | 2 | V |
| change of black level in the control range related to the nominal luminance signal (black-white) | | typ. | ± 50 | % |
| Internal signal limiting ** | | | | |
| signal limiting for nominal luminance (black to white = 100%) | | | | |
| black | | typ. | −25 | % |
| white | | typ. | 125 | % |

---

* During the clamping time (see sandcastle detector Fig. 1), the inserted RGB signals are clamped to the same black level as the internal RGB signals. For proper clamping, the internal resistance of the external signal sources should be < 200 Ω.

** Brightness, contrast and saturation control in nominal position.

### White point adjustment

| | | | | |
|---|---|---|---|---|
| A.C. voltage gain* | | | | |
| at $V_{21,22,23-24}$ = 6 V | | | 100 | % |
| at $V_{21,22,23-24}$ = 0 V | | < | 60 | % |
| at $V_{21,22,23-24}$ = 12 V | | > | 140 | % |
| Input resistance | $R_{21,22,23-24}$ | typ. | 20 | kΩ |

### Differential output amplifier

| | | | | |
|---|---|---|---|---|
| Feedback inputs (pins 2, 5, 27) | | | | |
| d.c. voltage during clamping | $V_{2,5,27-24}$ | typ. | 6 | V |
| voltage difference between the feedback inputs | $\Delta V$ | < | 80 | mV |
| input resistance | $R_{2,5,27-24}$ | > | 100 | kΩ |
| Output amplifiers (pins 1, 4, 26) | | | | |
| transconductance | $\frac{\Delta I_1}{\Delta V_{2-24}} = \frac{\Delta I_4}{\Delta V_{5-24}} = \frac{\Delta I_{26}}{\Delta V_{27-24}}$ | typ. | 20 | mA/V |
| integrated load resistance | $R_{1,4,26-24}$ | typ. | 610 | Ω |
| output current (peak value) at $V_{1,4,26-24}$ = 8,2 V | $\pm I_{1,4,26\,m}$ | typ. | 5 | mA |

### Gain data

| | | | | |
|---|---|---|---|---|
| At nominal contrast, saturation and white point adjustment | | | | |
| Voltage gain between Y-input (pin 15) and feedback inputs (pins 2, 5, 27) | $G_{2,5,27-15}$ | typ. | 10 | dB |
| Frequency response (0 to 5 MHz) | $d_{2,5,27-15}$ | < | 3 | dB |
| Voltage gain between colour difference inputs (pins 17 and 18) and feedback inputs (pins 5 and 27) | $G_{5-18} = G_{27-17}$ | typ. | 0 | dB |
| Frequency response (0 to 2 MHz) | $d_{5-18} = d_{27-17}$ | < | 3 | dB |
| Voltage gain between signal display inputs (pins 12, 13, 14) and feedback inputs (pins 2, 5, 27) | $G_{2-13} = G_{5-12} = G_{27-14}$ | < | 0 | dB |
| Frequency response (0 to 5 MHz) | $d_{2-13} = d_{5-12} = d_{27-14}$ | < | 3 | dB |

---

* With input pins 21, 22 and 23 not connected an internal bias voltage of 6 V is supplied.

**CHARACTERISTICS** (continued)

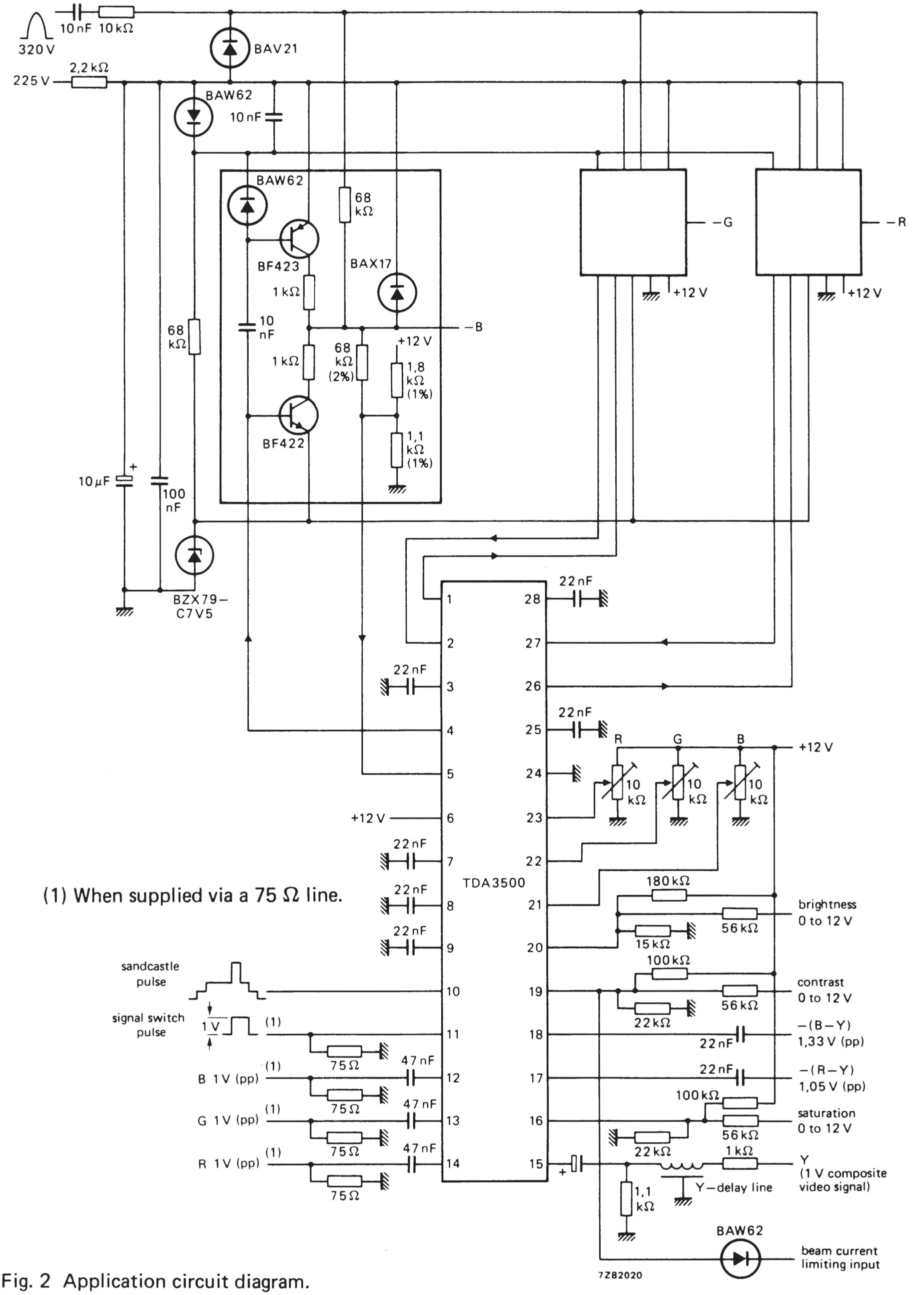
**Sandcastle detector**

There are 3 internal thresholds (proportional to $V_P$) the following amplitudes are required for separating the various pulses:

| | | | |
|---|---|---|---|
| horizontal and vertical blanking pulses (note 1) | $V_{10\text{-}24}$ | $>$<br>$<$ | 2 V<br>3 V |
| horizontal pulse (note 2) | $V_{10\text{-}24}$ | $>$<br>$<$ | 4 V<br>5 V |
| clamping pulse (note 3) | $V_{10\text{-}24}$ | $>$ | 7,5 V |
| d.c. voltage for artificial black level (note 4) (scan and flyback) | $V_{10\text{-}24}$ | $>$ | 7,5 V |
| no keying | $V_{10\text{-}24}$ | $<$ | 1 V |

Notes

1. Blanking to ultra-black (−20%).
2. Insertion of artificial black level.
3. Pulse duration $> 3{,}5$ μs.
4. This function will also be obtained by leaving pin 10 open.


320 V
10 nF
10 kΩ
BAV21
225 V
2,2 kΩ
BAW62
10 nF
BAW62
BF423
68 kΩ
BAX17
1 kΩ
10 nF
1 kΩ
68 kΩ (2%)
+12 V
1,8 kΩ (1%)
1,1 kΩ (1%)
BF422
−B
68 kΩ
10 µF
100 nF
BZX79−C7V5
−G
+12 V
−R
+12 V
TDA3500
1
2
3
4
5
6
7
8
9
10
11
12
13
14
28
27
26
25
24
23
22
21
20
19
18
17
16
15
22 nF
22 nF
22 nF
+12 V
22 nF
22 nF
22 nF
22 nF
R
G
B
10 kΩ
10 kΩ
10 kΩ
+12 V
180 kΩ
56 kΩ
15 kΩ
brightness 0 to 12 V
100 kΩ
56 kΩ
22 kΩ
contrast 0 to 12 V
22 nF
−(B−Y) 1,33 V (pp)
22 nF
−(R−Y) 1,05 V (pp)
100 kΩ
56 kΩ
22 kΩ
saturation 0 to 12 V
1 kΩ
Y (1 V composite video signal)
1,1 kΩ
Y−delay line
BAW62
beam current limiting input
sandcastle pulse
signal switch pulse
1 V
(1)
B 1 V (pp)
G 1 V (pp)
R 1 V (pp)
75 Ω
75 Ω
75 Ω
75 Ω
47 nF
47 nF
47 nF
7Z82020

(1) When supplied via a 75 Ω line.

Fig. 2 Application circuit diagram.

# VIDEO CONTROL COMBINATION

The TDA3501 is a monolithic integrated circuit performing the control functions in a PAL/SECAM decoder which additionally comprises the integrated circuits TDA3510 (PAL decoder) and/or TDA3520 (SECAM decoder).

The required input signals are: luminance and colour difference −(R-Y) and −(B-Y), while linear RGB signals can be inserted from an external source.

RGB signals are provided at the output to drive the video output stages.

The TDA3501 has the following features:

- capacitive coupling of the input signals
- linear saturation control
- (G-Y) and RGB matrix
- insertion possibility of linear RGB signals, e.g. video text, video games, picture-in-picture, camera or slide-scanner
- equal black level for inserted and matrixed signals by clamping
- 3 identical channels for the RGB signals
- linear contrast and brightness control, operating on both the inserted and matrixed RGB signals
- horizontal and vertical blanking (black and ultra-black respectively) and black-level clamping obtained via a 3-level sandcastle pulse
- differential amplifiers with feedback-inputs for stabilization of the RGB output stages
- 2 d.c. gain controls for the green and blue output signals (white point adjustment)
- beam current limiting possibility

## QUICK REFERENCE DATA

| | | | | |
|---|---|---|---|---|
| Supply voltage | $V_{6\text{-}24}$ | typ. | 12 | V |
| Supply current | $I_6$ | typ. | 100 | mA |
| Luminance input signal (peak-to-peak value) | $V_{15\text{-}24(p\text{-}p)}$ | typ. | 0,45 | V |
| Luminance input resistance | $R_{15\text{-}24}$ | typ. | 12 | kΩ |
| Colour difference input signals (peak-to-peak values) | | | | |
| −(B-Y) | $V_{18\text{-}24(p\text{-}p)}$ | typ. | 1,33 | V |
| −(R-Y) | $V_{17\text{-}24(p\text{-}p)}$ | typ. | 1,05 | V |
| Inserted RGB signals (peak-to-peak values) | $V_{12,13,14\text{-}24(p\text{-}p)}$ | typ. | 1 | V |
| Three-level sandcastle pulse detector | $V_{10\text{-}24}$ | typ. | 2,5/4,5/8,0 | V |
| Control voltage ranges | | | | |
| brightness | $V_{20\text{-}24}$ | | 1 to 3 | V |
| contrast | $V_{19\text{-}24}$ | | 2 to 4 | V |
| saturation | $V_{16\text{-}24}$ | | 2,1 to 4 | V |

## PACKAGE OUTLINE

28-lead DIL; plastic (SOT-117).

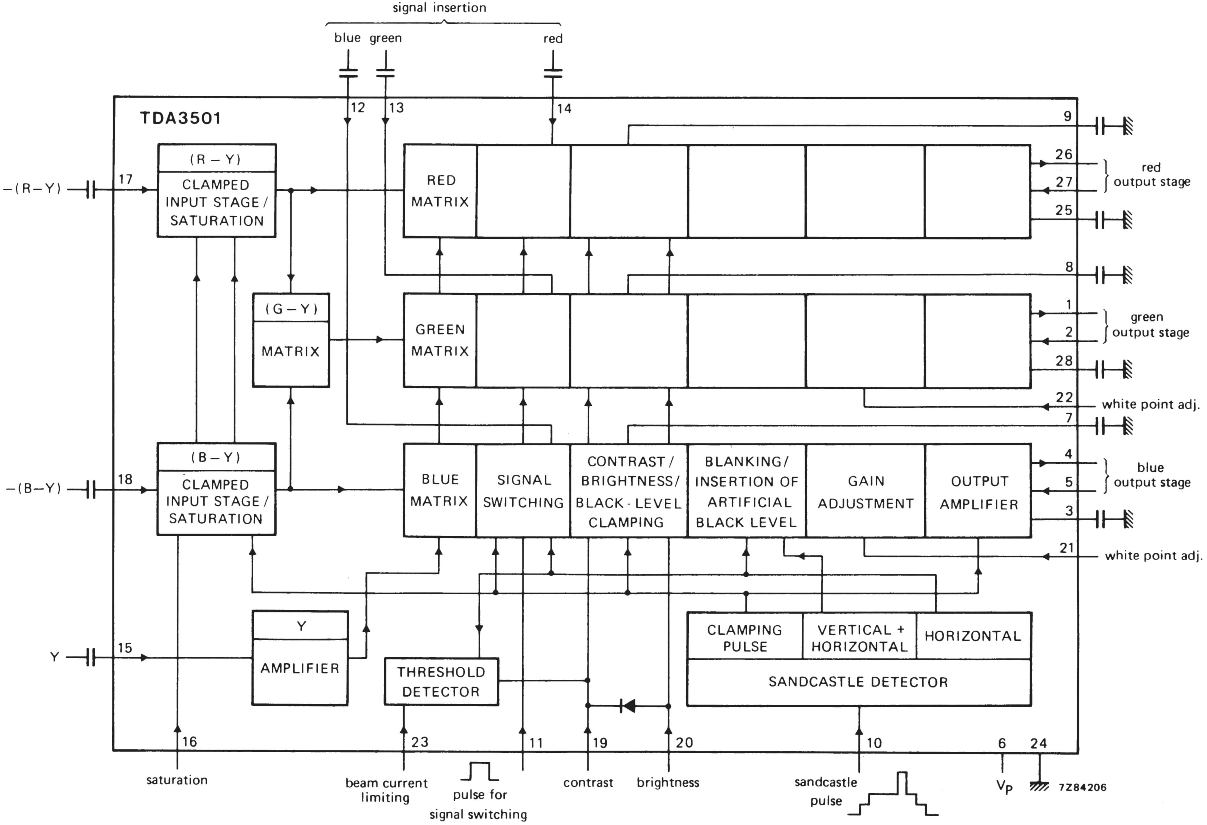

signal insertion
blue
green
red
12
13
14
TDA3501
9
26
27
red output stage
25
8
1
2
green output stage
28
22
white point adj.
7
4
5
blue output stage
3
21
white point adj.
−(R−Y)
17
(R − Y)
CLAMPED INPUT STAGE / SATURATION
RED MATRIX
(G − Y)
MATRIX
GREEN MATRIX
−(B−Y)
18
(B − Y)
CLAMPED INPUT STAGE / SATURATION
BLUE MATRIX
SIGNAL SWITCHING
CONTRAST / BRIGHTNESS / BLACK - LEVEL CLAMPING
BLANKING / INSERTION OF ARTIFICIAL BLACK LEVEL
GAIN ADJUSTMENT
OUTPUT AMPLIFIER
Y
15
Y
AMPLIFIER
THRESHOLD DETECTOR
CLAMPING PULSE
VERTICAL + HORIZONTAL
HORIZONTAL
SANDCASTLE DETECTOR
16
saturation
23
beam current limiting
pulse for signal switching
11
19
contrast
20
brightness
10
sandcastle pulse
6
$V_P$
24
7Z84206

Fig. 1  Block diagram.

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | min. | max. | |
|---|---|---|---|---|---|
| Supply voltage | $V_P = V_{6\text{-}24}$ | | – | 13,2 | V |
| Voltages with respect to pin 24 | | | | | |
| pins 1,4,26 | $V_{1,4,26\text{-}24}$ | | ½$V_P$ | $V_P + 1$ | V |
| pins 2,5,27 | $V_{2,5,27\text{-}24}$ | | 0 | $V_P$ | V |
| pin 10 | $V_{10\text{-}24}$ | | 0 | $V_P$ | V |
| pin 11 | $V_{11\text{-}24}$ | | –0,5 | 3 | V |
| pins 16,19,20 | $V_{16,19,20\text{-}24}$ | | 0 | ½$V_P$ | V |
| pins 21,22 | $V_{21,22\text{-}24}$ | | 0 | $V_P$ | V |
| pin 23 | $V_{23\text{-}24}$ | | 0 | $V_P$ | V |
| pins 3,25,28; 7,8,9; 12,13,14; 15,17,18 | no external d.c. voltage | | | | |
| Current at pin 20 | $I_{20}$ | max. | | 5 | mA |
| Total power dissipation | $P_{tot}$ | max. | | 1,7 | W |
| Storage temperature | $T_{stg}$ | | | –25 to + 125 | °C |
| Operating ambient temperature | $T_{amb}$ | | | –20 to + 70 | °C |

## CHARACTERISTICS

| | | | | |
|---|---|---|---|---|
| Supply voltage range | $V_P$ | | 10,8 to 13,2 | V |

The following characteristics are measured in Fig. 2; $V_P = 12$ V; $T_{amb} = 25$ °C; $V_{18\text{-}24(p\text{-}p)} = 1{,}33$ V; $V_{17\text{-}24(p\text{-}p)} = 1{,}05$ V; $V_{15\text{-}24(p\text{-}p)} = 0{,}45$ V; $V_{12,13,14\text{-}24(p\text{-}p)} = 1$ V; unless otherwise specified

| | | | | |
|---|---|---|---|---|
| Current consumption | $I_6$ | typ. | 100 | mA |

**Colour difference inputs**

| | | | | |
|---|---|---|---|---|
| –(B-Y) input signal (peak-to-peak value)* | $V_{18\text{-}24(p\text{-}p)}$ | | 1,33 | V |
| –(R-Y) input signal (peak-to-peak value)* | $V_{17\text{-}24(p\text{-}p)}$ | | 1,05 | V |
| Internal resistance of colour difference sources | | < | 200 | Ω |
| Input resistance | $R_{17,18\text{-}24}$ | > | 100 | kΩ |
| Internal d.c. voltage due to clamping | $V_{17,18\text{-}24}$ | typ. | 4,2 | V |
| Saturation control | | | | |
| control voltage range for a change of saturation from –20 dB to + 6 dB | $V_{16\text{-}24}$ | | 2,1 to 4 | V |
| control voltage for attenuation > 40 dB | $V_{16\text{-}24}$ | < | 1,8 | V |
| nominal saturation (6 dB below max.) | $V_{16\text{-}24}$ | typ. | 3 | V |
| input current | $I_{16}$ | < | 20 | μA |

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* For saturated colour bar with 75% of maximum amplitude.

**CHARACTERISTICS** (continued)

**(G-Y) matrix**

Matrixed according the equation $V_{(G\text{-}Y)} = -0{,}51\ V_{(R\text{-}Y)} - 0{,}19\ V_{(B\text{-}Y)}$

**Luminance amplifier**

| | | | | |
|---|---|---|---|---|
| Input signal (peak-to-peak) | $V_{15\text{-}24(p\text{-}p)}$ | | 0,45 | V |
| Input resistance | $R_{15\text{-}24}$ | typ. | 12 | kΩ |
| Internal d.c. voltage | $V_{15\text{-}24}$ | typ. | 2,7 | V |

**RGB channels**

| | | | | |
|---|---|---|---|---|
| Signal switching input voltage for insertion | | | | |
| on level | $V_{11\text{-}24}$ | | 0,9 to 1,5 | V |
| off level | $V_{11\text{-}24}$ | | −0,5 to + 0,3 | V |
| Input current | $I_{11}$ | | −100 to + 200 | μA |
| Signal insertion | | | | |
| external RGB input signal (peak-to-peak value)* | $V_{12,13,14\text{-}24(p\text{-}p)}$ | | 1 | V |
| internal d.c. voltage due to clamping | $V_{12,13,14\text{-}24}$ | typ. | 3,5 | V |
| input current | $I_{12,13,14}$ | < | 5 | μA |
| Contrast control | | | | |
| control voltage range for a change of contrast from −17 dB to + 3 dB | $V_{19\text{-}24}$ | | 2 to 4 | V |
| nominal contrast (3 dB below max.) | $V_{19\text{-}24}$ | typ. | 3,4 | V |
| control voltage for −6 dB | $V_{19\text{-}24}$ | typ. | 2,7 | V |
| input current at $V_{23\text{-}24} \geqslant 6$ V | $I_{19}$ | < | 2,5 | μA |
| Beam current limiting | | | | |
| internal d.c. voltage | $V_{23\text{-}24}$ | typ. | 6 | V |
| input resistance | $R_{23\text{-}24}$ | typ. | 10 | kΩ |
| input current contrast control | | | | |
| $V_{23\text{-}24} = 5{,}8$ V | $I_{19}$ | typ. | 0,7 | mA |
| $V_{23\text{-}24} = 5{,}7$ V | $I_{19}$ | typ. | 10 | mA |
| $V_{23\text{-}24} = 5{,}6$ V | $I_{19}$ | typ. | 16 | mA |
| Brightness control | | | | |
| control voltage range | $V_{20\text{-}24}$ | | 1 to 3 | V |
| nominal brightness voltage | $V_{20\text{-}24}$ | | 2 | V |
| input current | $I_{20}$ | < | 10 | μA |
| control voltage for nominal black level which equals the inserted artificial black level | $V_{20\text{-}24}$ | typ. | 2 | V |
| change of black level in the control range related to the nominal luminance signal (black-white) | | typ. | ± 50 | % |

---

* During the clamping time (see sandcastle detector Fig. 1), the inserted RGB signals are clamped to the same black level as the internal RGB signals. For proper clamping, the internal resistance of the external signal sources should be < 200 Ω.

| | | | | |
|---|---|---|---|---|
| Internal signal limiting* | | | | |
| signal limiting for nominal luminance (black to white = 100%) | | | | |
| black | | typ. | −25 | % |
| white | | typ. | 125 | % |

**White point adjustment**

| | | | | |
|---|---|---|---|---|
| A.C. voltage gain ** | | | | |
| at $V_{21,22\text{-}24} = 6$ V | | | 100 | % |
| at $V_{21,22\text{-}24} = 0$ V | | < | 60 | % |
| at $V_{21,22\text{-}24} = 12$ V | | > | 140 | % |
| Input resistance | $R_{21,22\text{-}24}$ | typ. | 20 | kΩ |

**Differential output amplifier**

| | | | | |
|---|---|---|---|---|
| Feedback inputs (pins 2,5,27) | | | | |
| d.c. voltage during clamping | $V_{2,5,27\text{-}24}$ | | 5,79 to 5,95 | V |
| voltage difference between the feedback inputs | $\Delta V$ | < | 80 | mV |
| input resistance | $R_{2,5,27\text{-}24}$ | > | 100 | kΩ |
| Output amplifiers (pins 1,4,26) transconductance | $\frac{\Delta I_1}{\Delta V_{2\text{-}24}} = \frac{\Delta I_4}{\Delta V_{5\text{-}24}} = \frac{\Delta I_{26}}{\Delta V_{27\text{-}24}}$ | typ. | 20 | mA/V |
| integrated load resistance | $R_{1,4,26\text{-}24}$ | typ. | 610 | Ω |
| output current (peak value) at $V_{1,4,26\text{-}24} = 8{,}2$ V | $\pm I_{1,4,26\,m}$ | typ. | 5 | mA |

**Gain data**

| | | | | |
|---|---|---|---|---|
| At nominal contrast, saturation and white point adjustment | | | | |
| Voltage gain between Y-input (pin 15) and feedback inputs (pins 2,5,27) | $G_{2,5,27\text{-}15}$ | typ. | 10 | dB |
| Frequency response (0 to 5 MHz) | $d_{2,5,27\text{-}15}$ | < | 3 | dB |
| Voltage gain between colour difference inputs (pins 17 and 18) and feedback inputs (pin 5 and 27) | $G_{5\text{-}18} = G_{27\text{-}17}$ | typ. | 0 | dB |
| Frequency response (0 to 2 MHz) | $d_{5\text{-}18} = d_{27\text{-}17}$ | < | 3 | dB |
| Voltage gain between signal display inputs (pins 12,13,14) and feedback inputs (pins 2,5,27) | $G_{2\text{-}13} = G_{5\text{-}12} = G_{27\text{-}14}$ | typ. | 0 | dB |
| Frequency response (0 to 5 MHz) | $d_{2\text{-}13} = d_{5\text{-}12} = d_{27\text{-}14}$ | < | 3 | dB |

* Brightness, contrast and saturation control in nominal position.

** With input pins 21 and 22 not connected an internal bias voltage of 6 V is supplied.

## CHARACTERISTICS (continued)

**Sandcastle detector**

There are 3 internal thresholds (proportional to $V_P$) the following amplitudes are required for separating the various pulses:

| | | | |
|---|---|---|---|
| horizontal and vertical blanking pulses (note 1) | $V_{10-24}$ | $>$<br>$<$ | 2 V<br>3 V |
| horizontal pulse (note 2) | $V_{10-24}$ | $>$<br>$<$ | 4 V<br>5 V |
| clamping pulse (note 3) | $V_{10-24}$ | $>$ | 7,5 V |
| d.c. voltage for artificial black level (note 4) (scan and flyback) | $V_{10-24}$ | $>$ | 7,5 V |
| no keying | $V_{10-24}$ | $<$ | 1 V |
| Input current | $-I_{10}$ | $<$ | 100 μA |

Notes

1. Blanking to ultra-black (—20%).
2. Insertion of artificial black level.
3. Pulse duration $> 3,5$ μs.
4. This function will also be obtained by leaving pin 10 open.

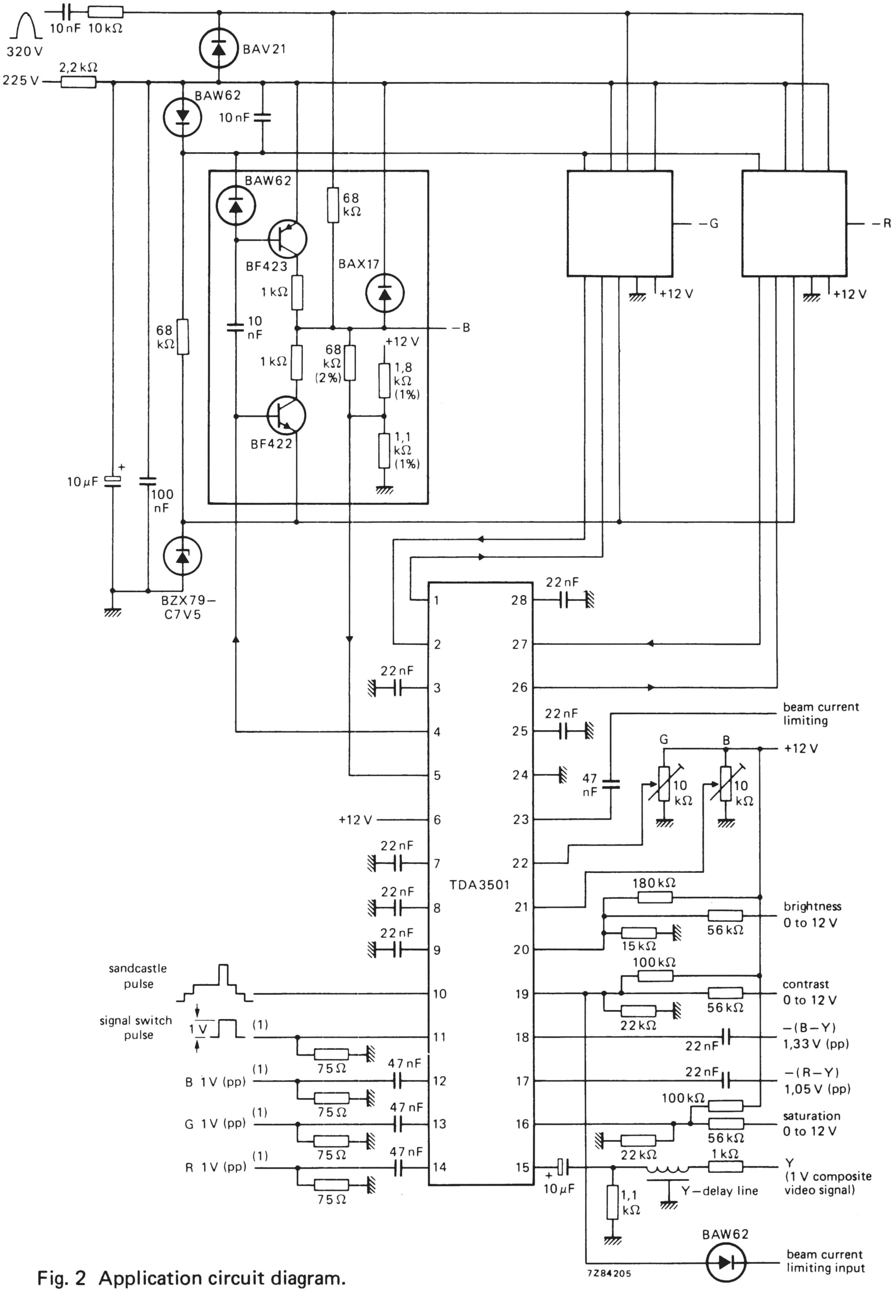

320 V
10 nF
10 kΩ
225 V
2,2 kΩ
BAV21
BAW62
10 nF
BAW62
68 kΩ
BF423
1 kΩ
BAX17
–B
68 kΩ
10 nF
1 kΩ
68 kΩ (2%)
+12 V
1,8 kΩ (1%)
1,1 kΩ (1%)
BF422
10 µF
100 nF
BZX79–C7V5
–G
+12 V
–R
+12 V
TDA3501
1
2
3
4
5
6
7
8
9
10
11
12
13
14
28
27
26
25
24
23
22
21
20
19
18
17
16
15
22 nF
22 nF
22 nF
+12 V
22 nF
22 nF
22 nF
22 nF
beam current limiting
G
B
+12 V
47 nF
10 kΩ
10 kΩ
180 kΩ
brightness 0 to 12 V
56 kΩ
15 kΩ
100 kΩ
contrast 0 to 12 V
56 kΩ
22 kΩ
22 nF
–(B–Y) 1,33 V (pp)
22 nF
–(R–Y) 1,05 V (pp)
100 kΩ
saturation 0 to 12 V
56 kΩ
22 kΩ
1 kΩ
Y (1 V composite video signal)
Y–delay line
10 µF
1,1 kΩ
BAW62
beam current limiting input
sandcastle pulse
signal switch pulse
1 V
(1)
75 Ω
B 1 V (pp)
(1)
47 nF
75 Ω
G 1 V (pp)
(1)
47 nF
75 Ω
R 1 V (pp)
(1)
47 nF
75 Ω
7Z84205

Fig. 2 Application circuit diagram.

# VIDEO CONTROL COMBINATION CIRCUIT

with automatic cut-off control

The TDA3505 performs the control functions in a PAL/SECAM decoder, which also comprises the TDA3510 (PAL decoder) and/or TDA3530 (SECAM decoder).

The required input signals are: luminance and colour difference −(R-Y) and −(B-Y), while linear RGB signals can be inserted from external sources. RGB output signals are delivered for driving the video output stages. This circuit provides automatic cut-off control of the picture tube. The TDA3505 has the following features:

- capacitive coupling of the colour difference and luminance input signals with black level clamping in the input stages
- linear saturation control in the colour difference stages
- (G-Y) and RGB matrix
- linear transmission of inserted signals
- equal black levels for inserted and matrixed signals
- 3 identical channels for the RGB signals
- linear contrast and brightness control, operating on both the inserted and matrixed RGB signals
- peak beam current limiting input
- horizontal and vertical blanking and clamping of the three input signals obtained via a 3-level sandcastle pulse
- d.c. gain controls for each of the RGB output signals (white point adjustment)
- emitter-follower outputs for driving the RGB output stages
- input for automatic cut-off control of the picture tube
- compensation for leakage current of the picture tube

## QUICK REFERENCE DATA

| | | | | |
|---|---|---|---|---|
| Supply voltage | $V_{6\text{-}24} = V_P$ | typ. | 12 | V |
| Supply current | $I_6 = I_P$ | typ. | 85 | mA |
| Composite video input signal (peak-to-peak value) | $V_{15\text{-}24(p\text{-}p)}$ | typ. | 0,45 | V |
| Input resistance | $R_{15\text{-}24}$ | > | 100 | kΩ |
| Colour difference input signals (peak-to-peak values) | | | | |
| −(B-Y) | $V_{18\text{-}24(p\text{-}p)}$ | typ. | 1,33 | V |
| −(R-Y) | $V_{17\text{-}24(p\text{-}p)}$ | typ. | 1,05 | V |
| Inserted RGB signals (black-to-white values) | $V_{12,13,14\text{-}24(p\text{-}p)}$ | typ. | 1 | V |
| Three-level sandcastle pulse (required input voltage) | $V_{10\text{-}24}$ | typ. | 2,5/4,5/8,0 | V |
| Control voltage ranges | | | | |
| brightness | $V_{20\text{-}24}$ | | 1,0 to 3,0 | V |
| contrast | $V_{19\text{-}24}$ | | 2,0 to 4,3 | V |
| saturation | $V_{16\text{-}24}$ | | 2,0 to 4,3 | V |

**PACKAGE OUTLINE** 28-lead DIL; plastic (SOT-117).

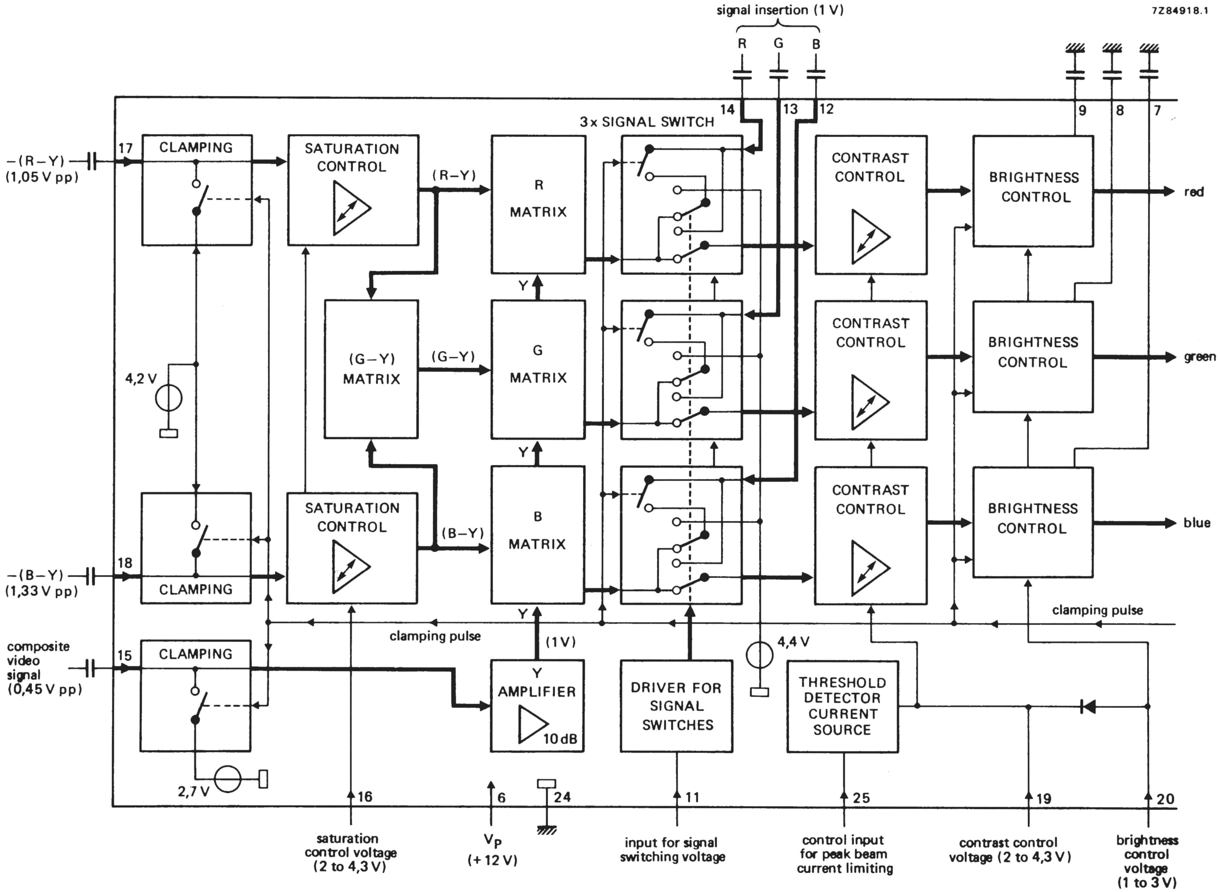

7Z84918.1
signal insertion (1 V)
R
G
B
14
13
12
9
8
7
3x SIGNAL SWITCH
−(R−Y)
(1,05 V pp)
17
CLAMPING
SATURATION CONTROL
(R−Y)
R MATRIX
CONTRAST CONTROL
BRIGHTNESS CONTROL
red
4,2 V
(G−Y) MATRIX
(G−Y)
Y
G MATRIX
CONTRAST CONTROL
BRIGHTNESS CONTROL
green
−(B−Y)
(1,33 V pp)
18
CLAMPING
SATURATION CONTROL
(B−Y)
Y
B MATRIX
CONTRAST CONTROL
BRIGHTNESS CONTROL
blue
clamping pulse
clamping pulse
Y
(1V)
4,4 V
composite video signal
(0,45 V pp)
15
CLAMPING
Y AMPLIFIER
10 dB
DRIVER FOR SIGNAL SWITCHES
THRESHOLD DETECTOR CURRENT SOURCE
2,7 V
16
6
24
11
25
19
20
saturation control voltage (2 to 4,3 V)
V$_P$ (+ 12 V)
input for signal switching voltage
control input for peak beam current limiting
contrast control voltage (2 to 4,3 V)
brightness control voltage (1 to 3 V)

Fig. 1a Part of block diagram; continued in Fig. 1b.

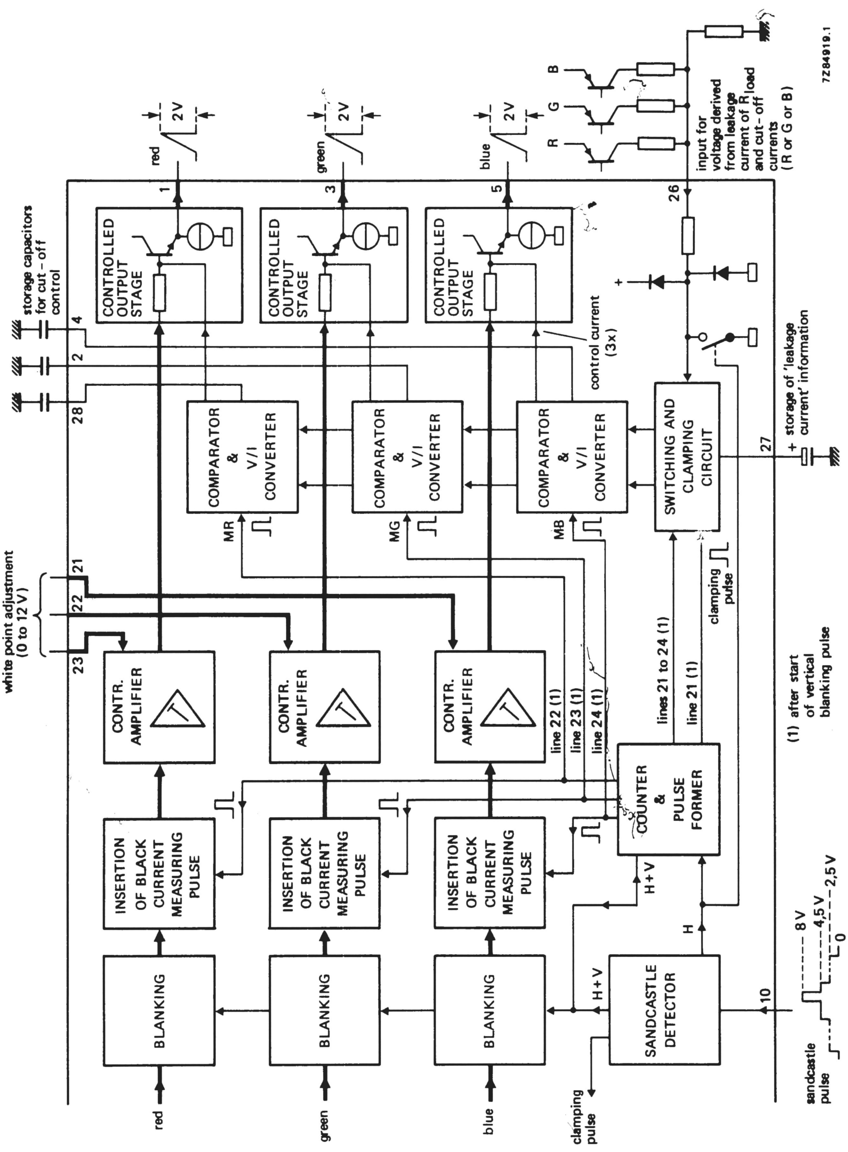

storage capacitors for cut-off control
28
2
4
white point adjustment (0 to 12 V)
21
22
23
red
green
blue
BLANKING
INSERTION OF BLACK CURRENT MEASURING PULSE
CONTR. AMPLIFIER
CONTROLLED OUTPUT STAGE
COMPARATOR & V/I CONVERTER
MR
MG
MB
control current (3x)
1
3
5
2V
R
G
B
input for voltage derived from leakage current of $R_{load}$ and cut-off currents (R or G or B)
26
SWITCHING AND CLAMPING CIRCUIT
27
storage of 'leakage current' information
clamping pulse
lines 21 to 24 (1)
line 21 (1)
line 22 (1)
line 23 (1)
line 24 (1)
COUNTER & PULSE FORMER
H + V
H
SANDCASTLE DETECTOR
10
sandcastle pulse
8 V
4,5 V
2,5 V
0
(1) after start of vertical blanking pulse
7Z84919.1

Fig. 1b Part of block diagram; continued from Fig. 1a.

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | min. | max. | |
|---|---|---|---|---|
| Supply voltage | $V_P = V_{6\text{-}24}$ | – | 13,2 | V |
| Voltages with respect to pin 24 | | | | |
| pin 26 | $V_{26\text{-}24}$ | 0 | $V_P$ | V |
| pin 25 | $V_{25\text{-}24}$ | 0 | $V_P$ | V |
| pin 10 | $V_{10\text{-}24}$ | 0 | $V_P$ | V |
| pin 11 | $V_{11\text{-}24}$ | –0,5 | 3 | V |
| pins 16, 19, 20 | $V_{16,19,20\text{-}24}$ | 0 | 0,5 $V_P$ | V |
| pins 21, 22, 23 | $V_{21,22,23\text{-}24}$ | 0 | $V_P$ | V |
| pins 1, 3, 5; 2, 4, 28; 7, 8, 9; 12, 13, 14; 15, 17, 18; 27 | no external d.c. voltage | | | |
| Currents | | | | |
| pins 1, 3, 5 | $-I_{1,\,3,\,5}$ | max. | 3 | mA |
| pin 19 | $I_{19}$ | max. | 10 | mA |
| pin 20 | $I_{20}$ | max. | 5 | mA |
| pin 25 | $-I_{25}$ | max. | 5 | mA |
| Total power dissipation | $P_{tot}$ | max. | 1,7 | W |
| Storage temperature range | $T_{stg}$ | | –25 to +125 | °C |
| Operating ambient temperature range | $T_{amb}$ | | –20 to +70 | °C |

## CHARACTERISTICS

| | | | | |
|---|---|---|---|---|
| Supply voltage range | $V_P = V_{6\text{-}24}$ | | 10,8 to 13,2 | V |

The following characteristics are measured in a circuit similar to Fig. 2; $V_P = 12$ V; $T_{amb} = 25$ °C; $V_{18\text{-}24(p\text{-}p)} = 1{,}33$ V; $V_{17\text{-}24(p\text{-}p)} = 1{,}05$ V; $V_{15\text{-}24(p\text{-}p)} = 0{,}45$ V; $V_{12,13,14\text{-}24(p\text{-}p)} = 1$ V; unless otherwise specified

| | | | | |
|---|---|---|---|---|
| Supply current | $I_6 = I_P$ | typ. | 85 | mA |
| **Colour difference inputs** | | | | |
| –(B-Y) input signal at pin 18 (peak-to-peak value)* | $V_{18\text{-}24(p\text{-}p)}$ | typ. | 1,33 | V |
| –(R-Y) input signal at pin 17 (peak-to-peak value)* | $V_{17\text{-}24(p\text{-}p)}$ | typ. | 1,05 | V |
| Input current during scanning | $I_{17,\,18}$ | < | 1 | μA |
| Input resistance | $R_{17,18\text{-}24}$ | > | 100 | kΩ |
| Internal d.c. voltage due to clamping | $V_{17,18\text{-}24}$ | typ. | 4,2 | V |
| Saturation control at pin 16 | | | | |
| control voltage range for a change of saturation from –20 dB to +6 dB | $V_{16\text{-}24}$ | | 2,1 to 4,3 | V |
| control voltage for attenuation > 40 dB | $V_{16\text{-}24}$ | < | 1,8 | V |
| nominal saturation (6 dB below max.) | $V_{16\text{-}24}$ | typ. | 3,1 | V |
| input current | $I_{16}$ | < | 20 | μA |

---

* For saturated colour bar with 75% of maximum amplitude.

**(G-Y) matrix**

Matrixed according to the equation $V_{(G-Y)} = -0{,}51\ V_{(R-Y)} - 0{,}19\ V_{(B-Y)}$

**Luminance amplifier** (pin 15)

| | | | | |
|---|---|---|---|---|
| Composite video input signal (peak-to-peak value) | $V_{15-24(p-p)}$ | typ. | 0,45 | V |
| Input resistance | $R_{15-24}$ | > | 100 | kΩ |
| Internal d.c. voltage | $V_{15-24}$ | typ. | 2,7 | V |
| Input current during scanning | $I_{15}$ | < | 1 | μA |

**RGB channels**

| | | | | |
|---|---|---|---|---|
| Signal switching input voltage for insertion (pin 11) | | | | |
| on level | $V_{11-24}$ | | 0,9 to 3 | V |
| off level | $V_{11-24}$ | < | 0,4 | V |
| Input current | $I_{11}$ | | −100 to + 200 | μA |
| Signal insertion (pin 12: blue; pin 13: green; pin 14: red) | | | | |
| external RGB input signal (black-to-white values) | $V_{12,13,14-24(p-p)}$ | = | 1 | V |
| internal d.c. voltage due to clamping* | $V_{12,13,14-24}$ | typ. | 4,4 | V |
| input current during scanning | $I_{12,13,14}$ | < | 1 | μA |
| Contrast control (pin 19) | | | | |
| control voltage range for a change of contrast from −18 dB to + 3 dB | $V_{19-24}$ | | 2 to 4,3 | V |
| nominal contrast (3 dB below max.) | $V_{19-24}$ | typ. | 3,6 | V |
| control voltage for −6 dB | $V_{19-24}$ | typ. | 2,8 | V |
| input current at $V_{25-24} > 6$ V | $I_{19}$ | < | 2 | μA |
| Peak beam current limiting (pin 25) | | | | |
| internal d.c. bias voltage | $V_{25-24}$ | typ. | 5,5 | V |
| input resistance | $R_{25-24}$ | typ. | 10 | kΩ |
| input current at contrast control input at $V_{25-24} = 5{,}1$ V | $I_{19}$ | typ. | 17 | mA |
| Brightness control (pin 20) | | | | |
| control voltage range | $V_{20-24}$ | | 1 to 3 | V |
| input current | $-I_{20}$ | < | 10 | μA |
| control voltage for nominal black level which equals the inserted artificial black level | $V_{20-24}$ | typ. | 2 | V |
| change of black level in the control range related to the nominal luminance signal (black-white) for $\Delta V_{20-24} = 1$ V | | typ. | 50 | % |

---

* $V_{11-24} < 0{,}4$ V during clamping time: the black levels of the inserted RGB signals are clamped on the black levels of the internal RGB signals.
$V_{11-24} > 0{,}9$ V during clamping time: the black levels of the inserted signals are clamped on an internal d.c. voltage.
Correct clamping of the external RGB signals is only possible when they are synchronous with the sandcastle pulse.

## CHARACTERISTICS (continued)

| | | | | |
|---|---|---|---|---|
| Internal signal limiting | | | | |
| signal limiting for nominal luminance (black to white = 100%) | | | | |
| black | | typ. | –25 | % |
| white | | typ. | 120 | % |

**White point adjustment** (pin 21: blue; pin 22: green; pin 23: red)

| | | | | |
|---|---|---|---|---|
| A.C. voltage gain (note 1) | | | | |
| at $V_{21,22,23\text{-}24} = 5{,}5$ V | | typ. | 100 | % |
| at $V_{21,22,23\text{-}24} = 0$ V | | = | 60 | % |
| at $V_{21,22,23\text{-}24} = 12$ V | | = | 140 | % |
| Input resistance | $R_{21,22,23\text{-}24}$ | typ. | 20 | kΩ |

**Emitter-follower outputs** (pin 1: red; pin 3: green; pin 5: blue)

At nominal contrast, saturation and white point adjustment

| | | | | |
|---|---|---|---|---|
| Output voltage (black-to-white signal, positive) | $V_{1,3,5\text{-}24(p\text{-}p)}$ | typ. | 2 | V |
| Black level without automatic cut-off control ($V_{28,2,4\text{-}24} = 10$ V) | $V_{1,3,5\text{-}24}$ | typ. | 6,7 | V |
| Internal current source | $I_{source}$ | typ. | 3 | mA |
| Cut-off current control range | $-\Delta V_{1,3,5\text{-}24}$ | typ. | 4,6 | V |

**Automatic cut-off control** (pin 26)

The measurement occurs in the following lines after start of the vertical blanking pulse:
line 21: measurement of leakage current
line 22: measurement of red cut-off current
line 23: measurement of green cut-off current
line 24: measurement of blue cut-off current

| | | | | |
|---|---|---|---|---|
| Input voltage range | $V_{26\text{-}24}$ | | 0 to + 6,5 | V |
| Voltage difference between cut-off current measurement (note 2) and leakage current measurement (note 3) | $\Delta V_{26\text{-}24}$ | typ. | 0,7 | V |

Input 26 switches to ground during horizontal flyback

**Notes**

1. With input pins 21, 22 and 23 not connected an internal bias voltage of 5,5 V is supplied.
2. Black level of measured channel is nominal; the other two channels are blanked to ultra-black.
3. All three channels blanked to ultra-black.
   The cut-off control cycle occurs when the vertical blanking part of the sandcastle pulse contains more than 3 line pulses.
   The internal signal blanking continues until the end of the last measurement line.
   The vertical blanking pulse is not allowed to contain more than 34 line pulses otherwise another control cycle begins.

## Gain data

At nominal contrast, saturation and white point adjustment

| | | | |
|---|---|---|---|
| Voltage gain with respect to Y-input (pin 15) | $G_{1,3,5\text{-}15}$ | typ. | 16 dB |
| Frequency response (0 to 5 MHz) | $d_{1,3,5\text{-}15}$ | $\leqslant$ | 3 dB |
| Voltage gain with respect to colour difference inputs (pins 17 and 18) | $G_{5\text{-}18} = G_{1\text{-}17}$ | typ. | 6 dB |
| Frequency response (0 to 2 MHz) | $d_{5\text{-}18} = d_{1\text{-}17}$ | $\leqslant$ | 3 dB |
| Voltage gain of inserted signals | $G_{1\text{-}14} = G_{3\text{-}13} = G_{5\text{-}12}$ | typ. | 6 dB |
| Frequency response (0 to 6 MHz) | $d_{1\text{-}14} = d_{3\text{-}13} = d_{5\text{-}12}$ | $\leqslant$ | 3 dB |

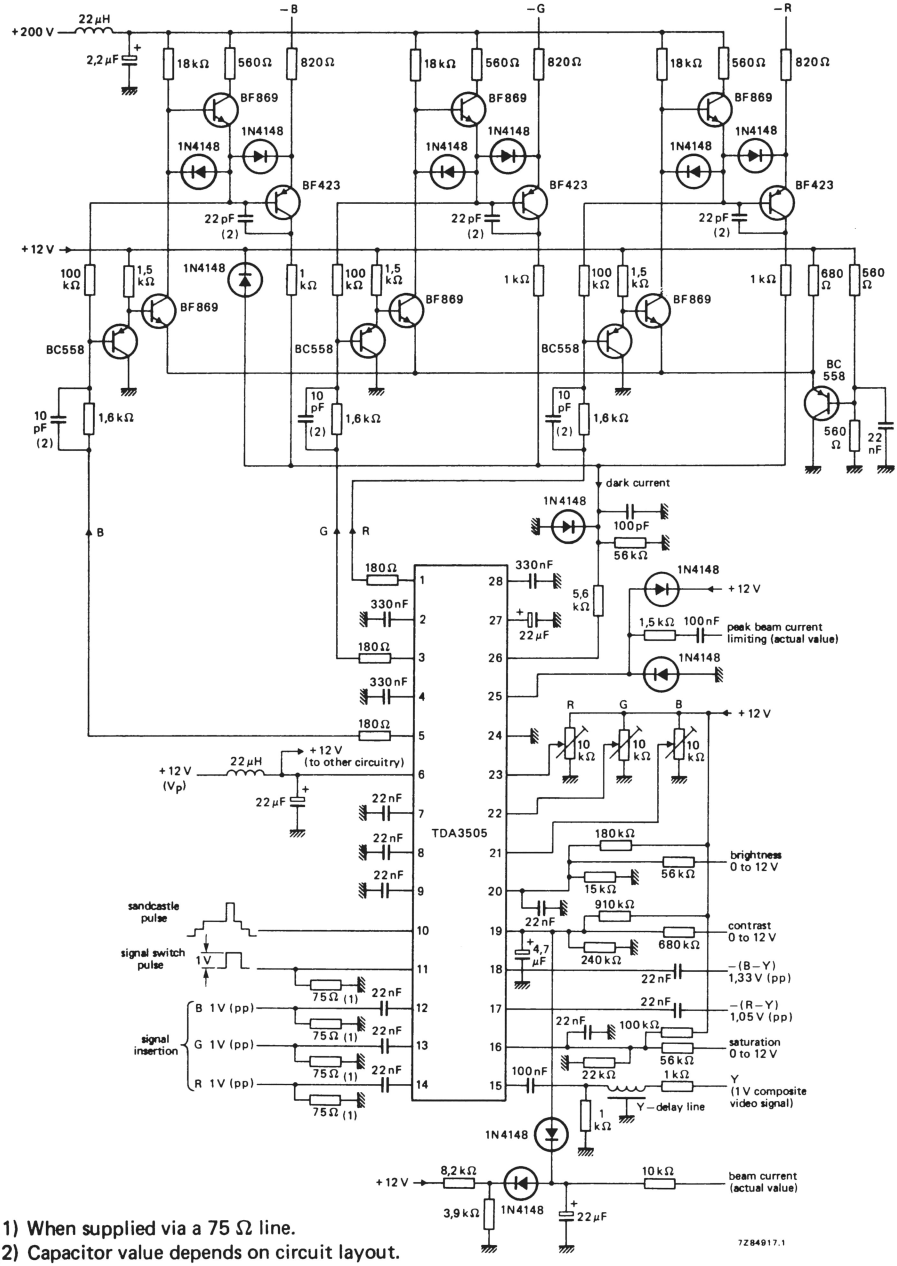
**Sandcastle detector** (pin 10)

There are 3 internal thresholds (proportional to $V_P$); note 1. The following amplitudes are required for separating the various pulses:

| | | | |
|---|---|---|---|
| horizontal and vertical blanking pulses (note 2) | $V_{10\text{-}24}$ | $>$<br>$<$ | 2 V<br>3 V |
| horizontal pulse | $V_{10\text{-}24}$ | $>$<br>$<$ | 4 V<br>5 V |
| clamping pulse (note 3) | $V_{10\text{-}24}$ | $>$ | 7,5 V |
| d.c. voltage for artificial black level (scan and flyback) | $V_{10\text{-}24}$ | $>$ | 7,5 V |
| no keying | $V_{10\text{-}24}$ | $<$ | 1 V |
| input current | $-I_{10}$ | $<$ | 110 μA |

**Notes**

1. The thresholds are for
   horizontal and vertical blanking: $V_{10\text{-}24} = 1{,}5$ V
   horizontal pulse: $V_{10\text{-}24} = 3{,}5$ V
   clamping pulse: $V_{10\text{-}24} = 7{,}0$ V
2. Blanking to ultra-black (−25%).
3. Pulse duration $\geqslant 3{,}5$ μs.


+200 V
22 μH
2,2 μF
−B
−G
−R
18 kΩ
560 Ω
820 Ω
BF869
1N4148
BF423
22 pF
(2)
+12 V
100 kΩ
1,5 kΩ
1 kΩ
BC558
10 pF
1,6 kΩ
680 Ω
560 Ω
BC 558
22 nF
dark current
100 pF
56 kΩ
5,6 kΩ
B
G
R
180 Ω
330 nF
22 μF
peak beam current limiting (actual value)
1,5 kΩ
100 nF
10 kΩ
+12 V (to other circuitry)
+12 V (V_p)
TDA3505
sandcastle pulse
signal switch pulse
1 V
signal insertion
B 1 V (pp)
G 1 V (pp)
R 1 V (pp)
75 Ω (1)
180 kΩ
brightness 0 to 12 V
15 kΩ
910 kΩ
contrast 0 to 12 V
680 kΩ
240 kΩ
4,7 μF
−(B−Y) 1,33 V (pp)
−(R−Y) 1,05 V (pp)
100 kΩ
saturation 0 to 12 V
22 kΩ
1 kΩ
Y (1 V composite video signal)
Y−delay line
8,2 kΩ
3,9 kΩ
10 kΩ
beam current (actual value)
7Z84917.1

(1) When supplied via a 75 Ω line.
(2) Capacitor value depends on circuit layout.

Fig. 2 Typical application circuit diagram using the TDA3505.

# PAL DECODER

The TDA3510 is a monolithic integrated colour decoder for the PAL standard.
The circuit incorporates the following functions:

**Chrominance part**

- Controlled chrominance amplifier
- Chrominance output stage with automatic standard switch for driving the 64 μs delay line
- Blanking circuit for the colour burst signal

**Reference voltage and control voltage part**

- 8,8 MHz reference oscillator with divider stage to obtain both the 4,4 MHz reference signals
- Gated phase comparison for an optimum noise ratio
- Circuit for obtaining the chrominance control voltage and a reference voltage
- Circuit for generating the colour killer signal and the identification signal

**Demodulator part**

- Two synchronous demodulators for the (B-Y) and (R-Y) signals
- PAL flip-flop and PAL switch
- Flyback blanking incorporated in the synchronous demodulators
- (R-Y) and (B-Y) signal output stages, which are controlled by the colour killer with switchable d.c. voltage levels

## QUICK REFERENCE DATA

| | | | | |
|---|---|---|---|---|
| Supply voltage | $V_P = V_{9\text{-}24}$ | typ. | 12 | V |
| Supply current | $I_9$ | typ. | 58 | mA |
| Chrominance input signal (peak-to-peak value) | $V_{1\text{-}24(p\text{-}p)}$ | | 10 to 200 | mV |
| Sandcastle pulse | | | | |
| burst gating level | $V_{20\text{-}24}$ | > | 7,5 | V |
| blanking level | $V_{20\text{-}24}$ | > | 1,8 | V |
| Colour difference output signals | | | | |
| peak-to-peak values | | | | |
| −(R-Y) signal | $V_{11\text{-}24(p\text{-}p)}$ | typ. | 1,05 V ± 3 | dB |
| −(B-Y) signal | $V_{10\text{-}24(p\text{-}p)}$ | typ. | 1,33 V ± 3 | dB |

## PACKAGE OUTLINE

24-lead DIL; plastic (SOT-101A).

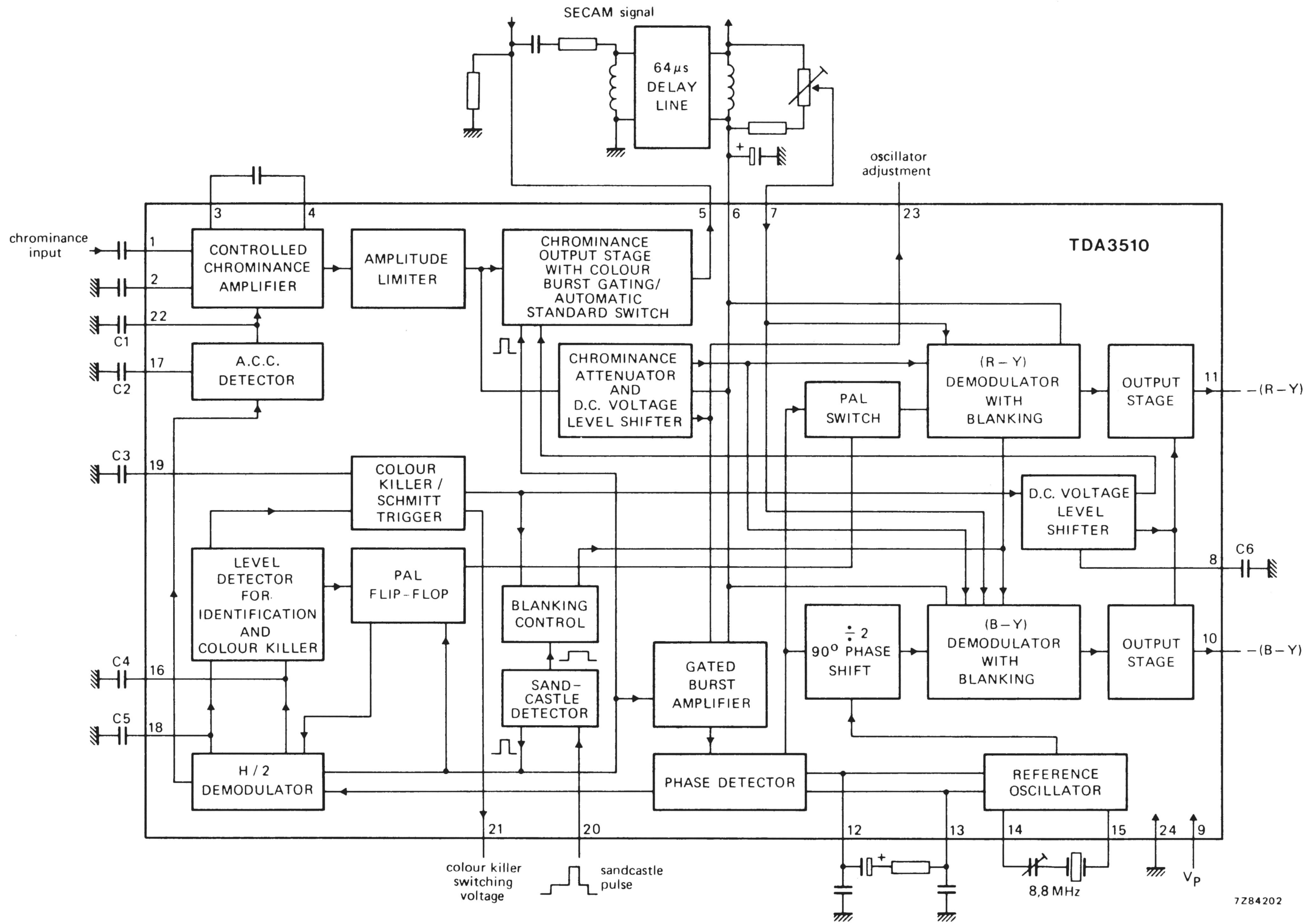

SECAM signal
64 μs DELAY LINE
oscillator adjustment
chrominance input
TDA3510
CONTROLLED CHROMINANCE AMPLIFIER
AMPLITUDE LIMITER
CHROMINANCE OUTPUT STAGE WITH COLOUR BURST GATING/ AUTOMATIC STANDARD SWITCH
CHROMINANCE ATTENUATOR AND D.C. VOLTAGE LEVEL SHIFTER
A.C.C. DETECTOR
PAL SWITCH
(R – Y) DEMODULATOR WITH BLANKING
OUTPUT STAGE
–(R – Y)
COLOUR KILLER / SCHMITT TRIGGER
D.C. VOLTAGE LEVEL SHIFTER
LEVEL DETECTOR FOR IDENTIFICATION AND COLOUR KILLER
PAL FLIP-FLOP
BLANKING CONTROL
SAND-CASTLE DETECTOR
GATED BURST AMPLIFIER
÷ 2 90° PHASE SHIFT
(B – Y) DEMODULATOR WITH BLANKING
OUTPUT STAGE
–(B – Y)
H / 2 DEMODULATOR
PHASE DETECTOR
REFERENCE OSCILLATOR
C1
C2
C3
C4
C5
C6
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
colour killer switching voltage
sandcastle pulse
8,8 MHz
V_P
7Z84202

Fig. 1 Block diagram; for external capacitors see next page.

External capacitors in Fig. 1

| capacitor | pins | |
|---|---|---|
| C1 | 22 – 24 | filter capacitor for control voltage |
| C2 | 17 – 24 | time constant for control voltage |
| C3 | 19 – 24 | time constant for colour ON |
| C4 | 16 – 24 | identification signal and colour OFF time constant |
| C5 | 18 – 24 | load capacitor for the reference voltage |
| C6 | 8 – 24 | time constant for the rise or fall time of the d.c. voltage level of the colour difference signal |

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | | |
|---|---|---|---|---|
| Supply voltage range | $V_P = V_{9\text{-}24}$ | | 10,8 to 13,2 | V |
| Currents | | | | |
| at pin 5 | $-I_5$ | max. | 10 | mA |
| at pins 10 and 11 | $-I_{10}, -I_{11}$ | max. | 1 | mA |
| at pin 21 | $I_{21}$ | max. | 10 | mA |
| Total power dissipation | $P_{tot}$ | max. | 1,1 | W |
| Storage temperature | $T_{stg}$ | | –20 to + 125 | °C |
| Operating ambient temperature | $T_{amb}$ | | –20 to + 65 | °C |

## CHARACTERISTICS

$V_P = 12$ V; $T_{amb} = 25$ °C

| | | | | |
|---|---|---|---|---|
| Supply current | $I_9$ | typ. | 58 | mA |

### Chrominance part

Chrominance signal is asymmetric (pins 1, 2)

| | | | | |
|---|---|---|---|---|
| Input voltage range (peak-to-peak value) | $V_{1\text{-}24(p\text{-}p)}$ | | 10 to 200 | mV |
| Nominal input voltage (peak-to-peak value) with 75% colour bar signal | $V_{1\text{-}24(p\text{-}p)}$ | typ. | 100 | mV |
| Input impedance | $\|Z_i\|$ | typ. | 3,3 | kΩ |
| Colour ON | | | | |
| chrominance output voltage (peak-to-peak value) with 75% colour bar signal | $V_{5\text{-}24(p\text{-}p)}$ | typ. | 2 | V |
| d.c. voltage at chrominance output | $V_{5\text{-}24}$ | typ. | 8 | V |
| Colour OFF | | | | |
| chrominance suppression | | > | 56 | dB |
| d.c. voltage at chrominance output | $V_{5\text{-}24}$ | typ. | 4 | V |

**CHARACTERISTICS** (continued)

**Reference voltage and control voltage part**

| | | | | |
|---|---|---|---|---|
| Oscillator (8,8 MHz) | | | | |
| Gain | $G_{14\text{-}15}$ | > | 8 | dB |
| Input resistance | $R_{15\text{-}24}$ | typ. | 270 | Ω |
| Output resistance | $R_{14\text{-}24}$ | < | 200 | Ω |
| Catching range | $\Delta f$ | typ. | 500 | Hz |
| Sandcastle pulse (pin 20) | | | | |
| Burst gating level | $V_{20\text{-}24}$ | > | 7,5 | V |
| Blanking level | $V_{20\text{-}24}$ | > | 1,8 | V |
| Colour switching voltage (open collector) | | | | |
| Maximum output current | $I_{21max}$ | typ. | 10 | mA |
| Colour ON | $V_{21\text{-}24}$ | typ. | $V_P$ | |
| Colour OFF | $V_{21\text{-}24}$ | < | 0,5 | V |
| Reference output voltage | $V_{18\text{-}24}$ | typ. | 5,5 | V |
| Colour killer voltages | | | | |
| colour OFF at | $V_{18\text{-}16}$ | typ. | 0 | V |
| or at | $V_{19\text{-}24}$ | > | 6 | V |
| colour ON at | $V_{18\text{-}16}$ | typ. | 1,5 | V |
| or at | $V_{19\text{-}24}$ | < | 4 | V |
| Colour unkill delay; depends on C3 | $t_d$ | typ. | 20 | ms/μF |
| Identification ON | $V_{16\text{-}18}$ | < | 200 | mV |

**Demodulator part**

| | | | | |
|---|---|---|---|---|
| Delayed chrominance input signal (peak-to-peak value) with 75% colour bar signal | $V_{7\text{-}24(p\text{-}p)}$ | typ. | 250 | mV |
| Colour difference output signals (peak-to-peak values) | | | | |
| −(R-Y) signal | $V_{11\text{-}24(p\text{-}p)}$ | typ. | 1,05 V ± 3 | dB |
| −(B-Y) signal | $V_{10\text{-}24(p\text{-}p)}$ | typ. | 1,33 V ± 3 | dB |
| Ratio of colour difference output signals (R-Y)/(B-Y) | $\frac{V_{11\text{-}24}}{V_{10\text{-}24}}$ | typ. | 0,79 ± 10 | % |
| D.C. voltage at colour difference outputs | | | | |
| at colour ON | $V_{10;\,11\text{-}24}$ | typ. | 8 | V |
| at colour OFF | $V_{10;\,11\text{-}24}$ | typ. | 4 | V |
| Signal attenuation at colour OFF | | > | 60 | dB |
| Residual 4,4 MHz signal | $V_{10;\,11\text{-}24}$ | < | 20 | mV |
| H/2 ripple at (R-Y) output (peak-to-peak value) without input signal | $V_{11\text{-}24(p\text{-}p)}$ | < | 10 | mV |

# SECAM DECODER

The TDA3520 is a monolithic integrated circuit which contains all the functions necessary for decoding the SECAM signal from the composite video and which offers the colour difference signals – (R–Y) and – (B–Y) to the video circuits TDA3500 or TDA 3501 in order to complete the SECAM decoding system.

By simply adding the PAL decoder circuit TDA3510, the SECAM system can be extended to receive SECAM/PAL signals as well. The 64 μs delay line is used in common and all system switching functions are performed automatically.

One of the main features of the TDA3520 is that only the clock filter has to be adjusted; all the other adjustments can be left out due to usage of PLL–type FM demodulators, the system of horizontal identification and the gain controlled chrominance amplifier.

The TDA3520 incorporates the following main functions:

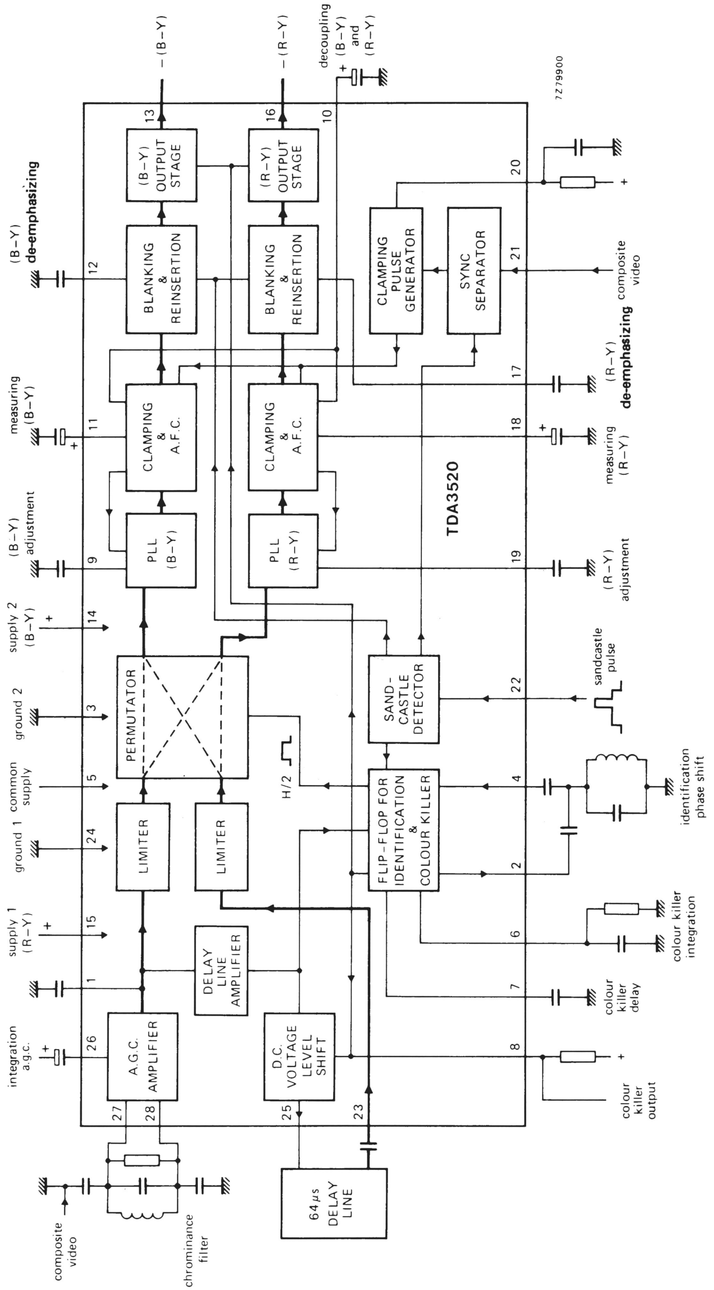
- gain controlled chrominance amplifier
- delay line amplifier (fixed gain of nom. 8), controlled by the colour killer (black–white/colour and SECAM/PAL commutation)
- limiter stages for direct signals and delayed signals
- permutator
- horizontal identification system; in PAL/SECAM receivers automatic standard switching is obtained if only a fixed phase shift circuit is added
- internal clamping generator and identification (1 μs) triggered either by the sandcastle pulse or by the video signal via the internal sync separator together with the flyback pulse
- (B–Y) and (R–Y) demodulators (without control) with burst level memory by means of an external capacitor
- circuits for horizontal and vertical blanking, during which de-emphasizing and restoring of black levels in the (R–Y) and (B–Y) signals occurs
- low-impedance output stages controlled by the colour killer (black/white/colour and SECAM/PAL switches)
- possibility for vertical identification by adding a simple external circuit
- colour killer output with H/2 information is available to control the luminance suppression filter from line to line.

## QUICK REFERENCE DATA

| | | | | |
|---|---|---|---|---|
| Supply voltage (pins 5, 14, 15) | $V_P$ | typ. | 12 | V |
| Supply current ($I_5 + I_{14} + I_{15}$) | $I_P$ | typ. | 90 | mA |
| Input voltage range (peak-to-peak value) | $V_{27\text{-}28\,(p\text{-}p)}$ | 10 to | 200 | mV |
| A.G.C. control range | | > | 26 | dB |
| Colour killer output current (SECAM not identified) | $I_8$ | < | 5 | mA |
| PLL demodulator catching range | $\Delta f$ | > | 1 | MHz |
| –(R–Y) output voltage (peak-to-peak value) | $V_{16\text{-}24\,(p\text{-}p)}$ | typ. | 1,05 | V |
| –(B–Y) output voltage (peak-to-peak value) | $V_{13\text{-}24\,(p\text{-}p)}$ | typ. | 1,33 | V |

## PACKAGE OUTLINE

28-lead DIL; plastic (SOT-117).


TDA3520
A.G.C. AMPLIFIER
DELAY LINE AMPLIFIER
D.C. VOLTAGE LEVEL SHIFT
LIMITER
LIMITER
PERMUTATOR
FLIP-FLOP FOR IDENTIFICATION & COLOUR KILLER
SAND-CASTLE DETECTOR
PLL (B−Y)
PLL (R−Y)
CLAMPING & A.F.C.
CLAMPING & A.F.C.
BLANKING & REINSERTION
BLANKING & REINSERTION
(B−Y) OUTPUT STAGE
(R−Y) OUTPUT STAGE
CLAMPING PULSE GENERATOR
SYNC SEPARATOR
64 μs DELAY LINE
H/2
composite video
chrominance filter
integration a.g.c.
supply 1 (R−Y)
ground 1
common supply
ground 2
supply 2 (B−Y)
(B−Y) adjustment
measuring (B−Y)
(B−Y) de-emphasizing
−(B−Y)
−(R−Y)
decoupling (B−Y) and (R−Y)
7Z79900
composite video
(R−Y) de-emphasizing
measuring (R−Y)
(R−Y) adjustment
sandcastle pulse
identification phase shift
colour killer integration
colour killer delay
colour killer output
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
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19
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23
24
25
26
27
28

Fig. 1 Block diagram.

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | | |
|---|---|---|---|---|
| Supply voltage (pins 5 and 14) | $V_P = V_{5,14,15\text{-}3,24}$ | max. | 13,2 | V |
| Total power dissipation | $P_{tot}$ | max. | 1,7 | W |
| Storage temperature | $T_{stg}$ | | −25 to + 125 | °C |
| Operating ambient temperature | $T_{amb}$ | | −20 to + 70 | °C |

## CHARACTERISTICS

| | | | | |
|---|---|---|---|---|
| Supply voltage range (pins 5,14 and 15) | $V_P$ | | 10,8 to 13,2 | V |

The following characteristics are measured in Fig. 2; $V_P = 12$ V; $T_{amb} = 25$ °C

| | | | | |
|---|---|---|---|---|
| Supply current | $I_P = I_5 + I_{14} + I_{15}$ | typ. | 90 | mA |

**Chrominance amplifier** (pins 27 and 28)

| | | | | |
|---|---|---|---|---|
| Input voltage range (peak-to-peak value) | $V_{27\text{-}28\,(p\text{-}p)}$ | | 10 to 200 | mV |
| Input resistance | $R_{27\text{-}28}$ | > | 50 | kΩ |
| A.G.C. control range<br>at 3 dB output signal variation at pin 25 | | > | 26 | dB |

**Delay line amplifier** (pin 25)

| | | | | |
|---|---|---|---|---|
| Output voltage (peak-to-peak value) | $V_{25\text{-}24\,(p\text{-}p)}$ | typ. | 2,6 | V |
| Output impedance | $\lvert Z_{25\text{-}24}\rvert$ | < | 100 | Ω |
| D.C. output voltage | | | | |
| SECAM identified | $V_{25\text{-}24}$ | typ. | 8 | V |
| SECAM not identified | $V_{25\text{-}24}$ | typ. | 4,5 | V |
| Attenuation (SECAM not identified) | | typ. | 60 | dB |

**Delay line input** (pin 23)

| | | | | |
|---|---|---|---|---|
| Input voltage (peak-to-peak value) * | $V_{23\text{-}24\,(p\text{-}p)}$ | typ. | 325 | mV |
| Input resistance | $R_{23\text{-}24}$ | > | 3 | kΩ |

**Identification circuit** (pins 2 and 4)

| | | | | |
|---|---|---|---|---|
| Output voltage (phase-shift circuit input)<br>(peak-to-peak value) | $V_{2\text{-}24\,(p\text{-}p)}$ | typ. | 2,8 | V |
| Output resistance | $R_{2\text{-}24}$ | < | 200 | Ω |
| Input voltage (phase-shift circuit output)<br>(peak-to-peak value) | $V_{4\text{-}24\,(p\text{-}p)}$ | typ. | 300 | mV |
| Input resistance | $R_{4\text{-}24}$ | > | 1 | kΩ |

---

* Corresponds with an attenuation of nom. 18 dB at pins 23 and 25 (delay line).

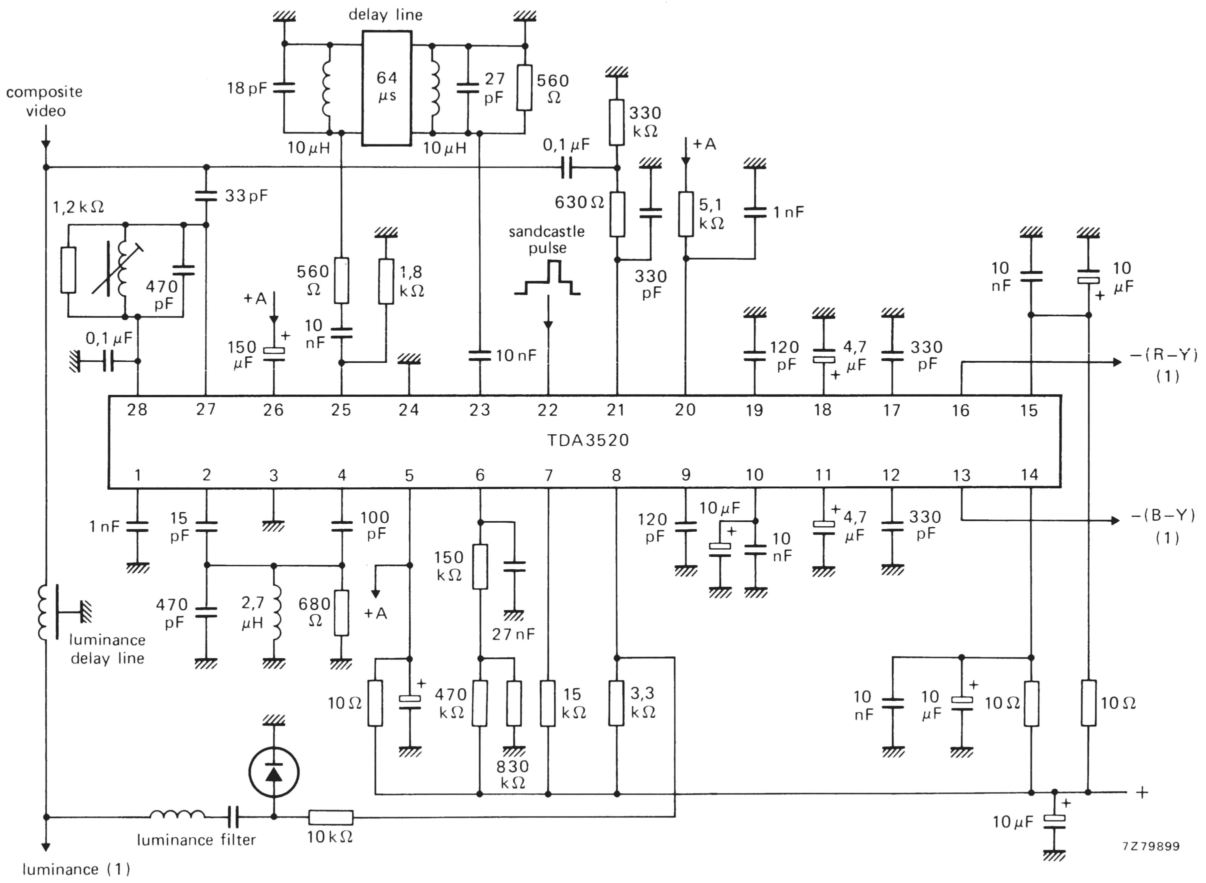
## CHARACTERISTICS (continued)

| | | | |
|---|---|---|---|
| **Colour killer output** (pin 8; open collector) | | | |
| Saturation voltage (SECAM not identified) | $V_{8-24}$ | typ. | 300 mV |
| Output current (SECAM not identified) | $-I_8$ | < | 5 mA |
| Output current (SECAM identified; blue line) | $-I_8$ | typ. | 0 mA |
| Output current (SECAM identified; red line) | $-I_8$ | typ. | 0,5 mA |
| **Sync separator** (pin 21) | | | |
| Slicing level * | $V_{21-24}$ | typ. | 2,5 V |
| Video input voltage (peak-to-peak value) ** | $V_{21-24}$ (p-p) | typ. | 1 V |
| **Sandcastle input (or flyback pulse)** (pin 22) | | | |
| Blanking level for driving the sync separator | $V_{22-24}$ | | 1,0 to 2,0 V * |
| Flip-flop slicing level | $V_{22-24}$ | | 3,0 to 4,0 V * |
| Maximum input current | $I_{22\ max}$ | < | 100 μA |
| **Demodulators** (pins 9 and 19) | | | |
| PLL demodulator catching range | $\Delta f$ | > | 1 MHz |
| Equivalent error at the reinserted reference levels | $\Delta f_o$ | < | 4 kHz |
| **Colour difference output stages** (pins 13 and 16) | | | |
| Output voltages (peak-to-peak values) | | | |
| −(R−Y) signal | $V_{16-24}$ (p-p) | typ. | 1,05 V |
| −(B−Y) signal | $V_{13-24}$ (p-p) | typ. | 1,33 V |
| D.C. output voltage | $V_{13,16-24}$ | typ. | 6 V * |
| Output resistance | $R_{13,16-24}$ | < | 100 Ω |
| Attenuation (SECAM not identified) | | typ. | 62 dB |
| H/Z ripple at the outputs (peak-to-peak value) | $V_{13,16-24}$ (p-p) | < | 10 mV |

---

*Proportional to the supply voltage.

** Capacitive coupling; see Fig. 2.


composite video
delay line
64 µs
18 pF
10 µH
10 µH
27 pF
560 Ω
330 kΩ
0,1 µF
+A
33 pF
1,2 kΩ
470 pF
0,1 µF
630 Ω
330 pF
5,1 kΩ
1 nF
sandcastle pulse
560 Ω
1,8 kΩ
+A
150 µF
10 nF
10 nF
120 pF
4,7 µF
330 pF
10 nF
10 µF
−(R−Y) (1)
28
27
26
25
24
23
22
21
20
19
18
17
16
15
TDA3520
1
2
3
4
5
6
7
8
9
10
11
12
13
14
1 nF
15 pF
100 pF
150 kΩ
120 pF
10 µF
10 nF
4,7 µF
330 pF
−(B−Y) (1)
470 pF
2,7 µH
680 Ω
+A
27 nF
luminance delay line
10 Ω
470 kΩ
15 kΩ
3,3 kΩ
830 kΩ
10 nF
10 µF
10 Ω
10 Ω
+
10 µF
luminance filter
10 kΩ
luminance (1)
7Z79899

(1) To TDA3500 or TDA3501

Fig. 2 Application diagram.

# TELEVISION I.F. AMPLIFIERS AND DEMODULATORS

The TDA3540 and TDA3541 are i.f. amplifier and demodulator circuits for colour and black and white television receivers, using n-p-n tuners for the TDA3540 and p-n-p tuners for the TDA3541.

They incorporate the following functions:

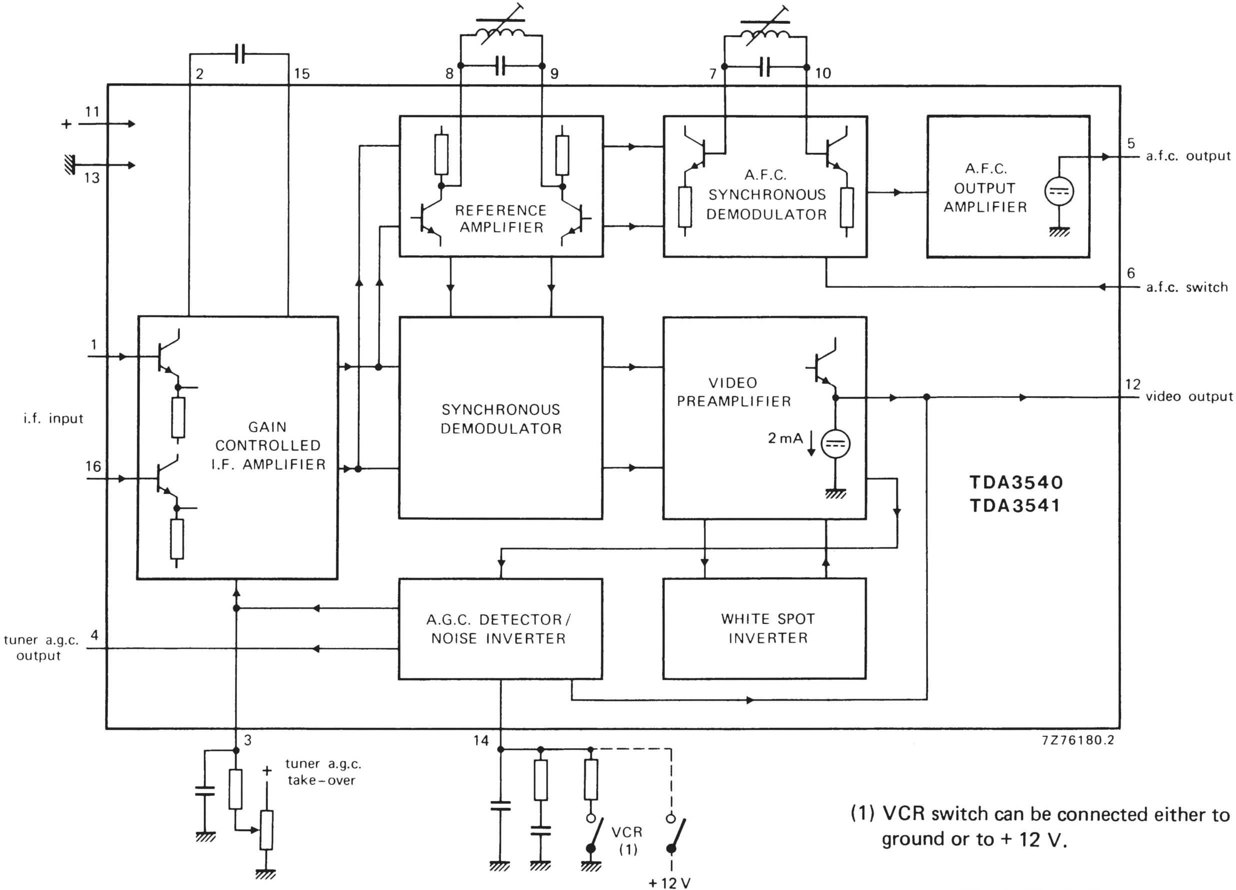
- gain-controlled wide-band amplifier, providing complete i.f. gain
- synchronous demodulator with excellent intermodulation
- white spot inverter
- video preamplifier with noise protection
- a.f.c. circuit with a.f.c. on/off switch
- a.g.c. circuit with noise gating
- tuner a.g.c. output (n-p-n tuners: **TDA3540**; p-n-p tuners: **TDA3541**)
- external video switch which switches off the video output; e.g. for insertion of a VCR playback signal, by either a high or a low level.

## QUICK REFERENCE DATA

| | | | | |
|---|---|---|---|---|
| Supply voltage | $V_{11\text{-}13}$ | typ. | 12 | V |
| Supply current | $I_{11}$ | typ. | 50 | mA |
| I.F. input sensitivity at 38,9 MHz (r.m.s. value) | $V_{1\text{-}16(rms)}$ | typ. | 60 | μV |
| Video output voltage (white at 10% of top sync) | $V_{12\text{-}13(p\text{-}p)}$ | typ. | 2,7 | V |
| I.F. voltage gain control range | $G_v$ | typ. | 64 | dB |
| Signal-to-noise ratio at $V_i$ = 10 mV | S/N | typ. | 58 | dB |
| A.F.C. output voltage swing (peak-to-peak value) | $V_{5\text{-}13(p\text{-}p)}$ | typ. | 10,7 | V |

## PACKAGE OUTLINES

TDA3540; TDA3541: 16-lead DIL; plastic (SOT-38).
TDA3540Q; TDA3541Q: 16-lead QIL; plastic (SOT-58).


TDA3540
TDA3541
GAIN CONTROLLED I.F. AMPLIFIER
REFERENCE AMPLIFIER
SYNCHRONOUS DEMODULATOR
A.F.C. SYNCHRONOUS DEMODULATOR
A.F.C. OUTPUT AMPLIFIER
VIDEO PREAMPLIFIER
2 mA
A.G.C. DETECTOR / NOISE INVERTER
WHITE SPOT INVERTER
1
16
i.f. input
2
15
8
9
7
10
11
+
13
5
a.f.c. output
6
a.f.c. switch
12
video output
4
tuner a.g.c. output
3
tuner a.g.c. take-over
+
14
VCR (1)
+ 12 V
7Z76180.2

(1) VCR switch can be connected either to ground or to + 12 V.

Fig. 1 Block diagram.

## PINNING

| | |
|---|---|
| 1 - 16 | Balanced i.f. input. |
| 2 - 15 | Decoupling capacitor for the d.c. feedback loop of the i.f. amplifier. |
| 3 | Adjusting pin for starting point of tuner a.g.c. |
| 4 | Tuner a.g.c. output. |
| 5 | A.F.C. output. |
| 6 | A.F.C. on/off switch. |
| 7 - 10 | A.F.C. circuitry to obtain $\pi/2$ phase shift of the reference carrier. |
| 8 - 9 | Circuitry for passive regeneration of the i.f. picture carrier. |
| 11 | Positive power supply. |
| 12 | Video output. |
| 13 | Ground. |
| 14 | I.F. a.g.c.; VCR switch. |

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | | |
|---|---|---|---|---|
| Supply voltage | $V_{11-13}$ | max. | 13,2 | V |
| I.F. a.g.c. voltage/VCR switch | $V_{14-13}$ | max. | 13,2 | V |
| Tuner a.g.c. voltage | $V_{4-13}$ | max. | 12 | V |
| A.F.C. switch voltage | $V_{6-13}$ | max. | 13,2 | V |
| Maximum voltage level at pin 12 with VCR switch active | $V_{12-13}$ | max. | 5,0 | V |
| D.C. output current at video output | $I_{12}$ | max. | 10 | mA |
| Total power dissipation | $P_{tot}$ | max. | 1,2 | W |
| Storage temperature range | $T_{stg}$ | | −65 to + 150 | °C |
| Operating ambient temperature range | $T_{amb}$ | | −25 to + 70 | °C |

DEVELOPMENT SAMPLE DATA

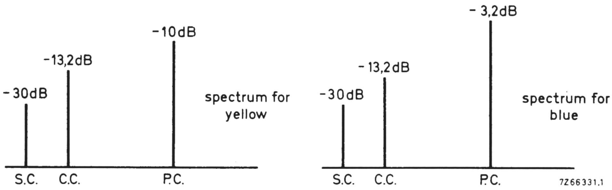
**CHARACTERISTICS** (measured in Fig. 8)

| | | | |
|---|---|---|---|
| Supply voltage range | $V_{11\text{-}13}$ | typ.<br> | 12 V<br>10,2 to 13,2 V |

The following characteristics are measured at $T_{amb}$ = 25 °C; $V_{11\text{-}13}$ = 12 V

| | | | |
|---|---|---|---|
| Current consumption (no input signal) | $I_{11}$ | typ.<br> | 50 mA<br>35 to 70 mA |
| **I.F. amplifier** (note 1) | | | |
| I.F. sensitivity (onset of a.g.c.) | $V_{1\text{-}16}$ | typ.<br>$<$ | 60 μV<br>100 μV |
| Input resistance (differential) | $R_{1\text{-}16}$ | typ.<br> | 2 kΩ<br>1,5 to 3 kΩ |
| Input capacitance (differential) | $C_{1\text{-}16}$ | typ.<br>$<$ | 2 pF<br>5 pF |
| Gain control range | $G_v$ | typ. | 64 dB |
| Output signal expansion for 50 dB input signal variation (note 2) | $\Delta V_{12\text{-}13}$ | $<$ | 0,5 dB |
| Maximum input signal | $V_{1\text{-}16}$ | $>$ | 70 mV |
| **Tuner a.g.c.** (note 1) | | | |
| Starting point tuner a.g.c.; adjustable (note 3) pin 3 connected with 39 kΩ to pin 11 | | | |
| **TDA3540** | $V_{1\text{-}16}$ | $<$ | 3 mV |
| **TDA3541** | $V_{1\text{-}16}$ | $<$ | 3 mV |
| pin 3 connected with 39 kΩ to ground | $V_{1\text{-}16}$ | $>$ | 70 mV |
| Maximum tuner a.g.c. output current swing | $I_4$ | $>$ | 10 mA |
| Input signal variation (note 4) for a tuner a.g.c. current variation of: | | | |
| 9 mA to 1 mA (**TDA3540**) | $\Delta V_{1\text{-}16}$ | typ. | 5 dB |
| 1 mA to 9 mA (**TDA3541**) | $\Delta V_{1\text{-}16}$ | typ. | 5 dB |
| Output saturation voltage at $I_4$ = 7 mA | $V_{4\text{-}13sat}$ | typ.<br>$<$ | 200 mV<br>300 mV |
| Leakage current at $V_{4\text{-}13}$ = 12 V | $I_4$ | $<$ | 1 μA |
| Tuner a.g.c. characteristic | see Fig. 5 | | |
| **Video output** (note 5) | | | |
| Zero-signal output level (note 6) | $V_{12\text{-}13}$ | typ.<br> | 6 V<br>5,7 to 6,3 V |
| Top sync output level | $V_{12\text{-}13}$ | typ.<br> | 2,95 V<br>2,80 to 3,10 V |
| Video output signal (peak-to-peak value) white at 10% of top sync | $V_{12\text{-}13(p\text{-}p)}$ | typ. | 2,7 V |

| | | | | |
|---|---|---|---|---|
| Internal bias current of n-p-n emitter-follower output transistor | | typ. | 2 | mA |
| | | | 1 to 3 | mA |
| Bandwidth of demodulated output signal | B | > | 5,5 | MHz |
| | | typ. | 6,5 | MHz |
| Differential gain (note 7) | dG | typ. | 3 | % |
| | | < | 10 | % |
| Differential phase (note 8) | d$\varphi$ | typ. | 2° | |
| | | < | 10° | |
| Residual carrier signal (r.m.s. value) | $V_{12\text{-}13(rms)}$ | typ. | 3,5 | mV |
| | | < | 30,0 | mV |
| Residual 2nd harmonic of carrier signal (r.m.s. value) | $V_{12\text{-}13(rms)}$ | typ. | 15 | mV |
| | | < | 30 | mV |
| Intermodulation (see Figs 2 and 3) at 1,1 MHz: blue (note 9) | | > | 56 | dB |
| | | typ. | 62 | dB |
| yellow (note 9) | | > | 53 | dB |
| | | typ. | 57 | dB |
| at 3,3 MHz (note 10) | | > | 66 | dB |



S.C. : sound carrier level
C.C. : chrominance carrier level
P.C. : picture carrier level

with respect to top sync level

Fig. 2 Input conditions for intermodulation measurements; standard colour bar with 75% contrast.

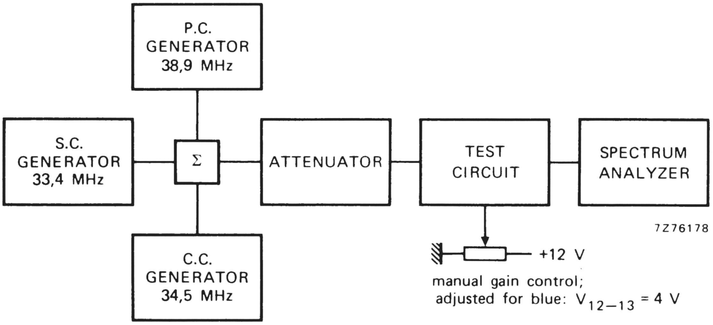

P.C. GENERATOR 38,9 MHz
S.C. GENERATOR 33,4 MHz
Σ
ATTENUATOR
TEST CIRCUIT
SPECTRUM ANALYZER
C.C. GENERATOR 34,5 MHz
7Z76178
+12 V
manual gain control; adjusted for blue: $V_{12-13}$ = 4 V

Fig. 3 Test set-up for intermodulation.

**CHARACTERISTICS** (continued)

| | | | |
|---|---|---|---|
| Signal-to-noise ratio (note 11) | | | |
| at 10 mV input signal | S/N | > | 50 dB |
| | | typ. | 58 dB |
| at end of gain control range | S/N | > | 54 dB |
| | | typ. | 61 dB |
| as a function of the input signal | see Fig. 6 | | |

**White spot and noise inverter** (see Fig. 4)

| | | | |
|---|---|---|---|
| White spot inverter threshold level | $V_{12\text{-}13}$ | typ. | 6,8 V |
| | | | 6,3 to 7,3 V |
| White spot insertion level | $V_{12\text{-}13}$ | typ. | 4,5 V |
| | | | 4,2 to 4,8 V |
| Noise inverter threshold level | $V_{12\text{-}13}$ | typ. | 1,8 V |
| | | | 1,6 to 2,0 V |
| Noise insertion level | $V_{12\text{-}13}$ | typ. | 3,8 V |
| | | | 3,4 to 4,1 V |

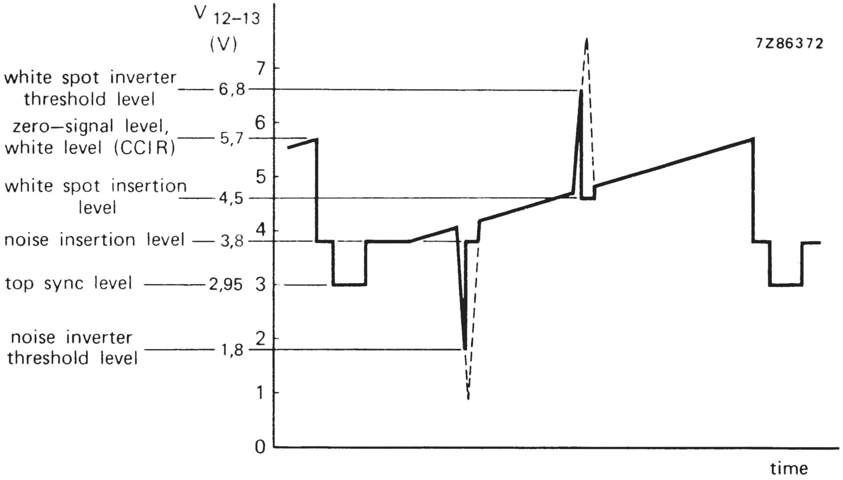


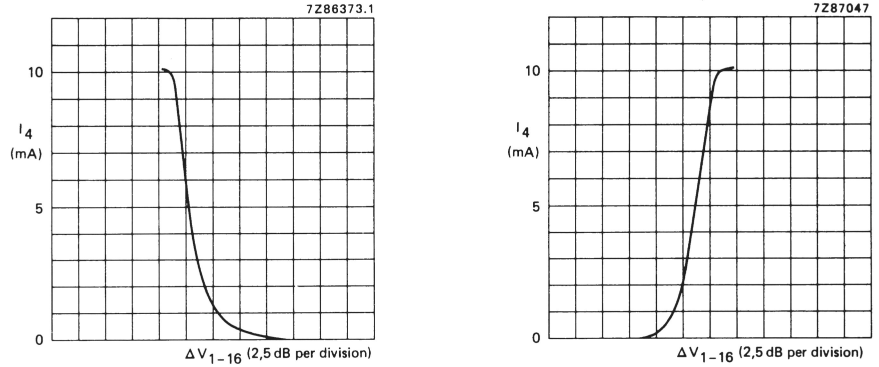
Fig. 4 Video output waveform showing white spot and noise inverter threshold levels.

**VCR switch**

| | | | |
|---|---|---|---|
| Switches the output off: | | | |
| below | $V_{14\text{-}13}$ | typ. | 1,9 V |
| | | | 1,4 to 2,4 V |
| above | $V_{14\text{-}13}$ | typ. | 10,7 V |
| | | | 10 to 11,3 V |

**A.F.C.** (note 12)

| | | | | |
|---|---|---|---|---|
| A.F.C. output voltage swing (peak-to-peak value) | $V_{5\text{-}13(p\text{-}p)}$ | > | 10 | V |
| | | typ. | 10,7 | V |
| Change of frequency for an a.f.c. output voltage swing of 10 V | | | | |
| at 100% picture carrier | $\Delta f$ | typ. | 70 | kHz |
| | | < | 150 | kHz |
| at 10% picture carrier | $\Delta f$ | typ. | 100 | kHz |
| | | < | 200 | kHz |
| A.F.C. output voltage when tuned at 38,9 MHz | $V_{5\text{-}13}$ | typ. | 6 | V |
| A.F.C. output voltage (no input signal) | $V_{5\text{-}13}$ | typ. | 6 | V |
| | | | 4 to 8 | V |
| A.F.C. switch switches off below | $V_{6\text{-}13}$ | typ. | 2,9 | V |
| | | | 1,6 to 3,5 | V |
| Recommended a.f.c. active voltage | $V_{6\text{-}13}$<br>or: pin 6 floating | | 3,5 to 6 | V |
| A.F.C. switch leakage current at $V_{6\text{-}13} = 6$ V | $I_6$ | < | 1 | μA |
| A.F.C. output current during a.f.c. off measured with $f_o \pm 300$ kHz and $V_{6\text{-}13} = 1,5$ V | $I_5$ | | −2,5 to + 2,5 | μA |
| A.F.C. output current during a.f.c. on | $I_5$ | > | 1 | mA |
| | | typ. | 2 | mA |



(a)

(b)

Fig. 5 Typical tuner a.g.c. characteristics;
pin 3 connected to the supply voltage (pin 11) with 39 kΩ.

a: TDA3540
b: TDA3541

**CHARACTERISTICS** (continued)

**Notes to characteristics**

1. All input signals are measured r.m.s. at top sync and 38,9 MHz.
2. Measured with 0 dB = 200 $\mu$V.
3. Starting point of the tuner a.g.c. is defined as the input signal level where the tuner a.g.c. current is 9 mA for the **TDA3540** and 1 mA for the **TDA3541**.
4. Measured with pin 3 connected with 39 k$\Omega$ to the supply voltage (pin 11).
5. Measured at 10 mV r.m.s. top sync input signal.
6. So-called 'projected zero point', e.g. with switched demodulator.
7. Measured according to EBU test, line 330.
   The differential gain is expressed as a percentage of the difference in peak amplitudes between the largest and smallest section relative to the sub-carrier amplitude at blanking level.
8. Measured according to EBU test, line 330.
   The differential phase is defined as the difference in degrees between the largest and smallest phase angle of the six sections.
9. $20 \log \frac{V_o \text{ at } 4{,}4 \text{ MHz}}{V_o \text{ at } 1{,}1 \text{ MHz}} + 3{,}6 \text{ dB}$.
10. $20 \log \frac{V_o \text{ at } 4{,}4 \text{ MHz}}{V_o \text{ at } 3{,}3 \text{ MHz}}$.
11. Measured with a 75 $\Omega$ source; $S/N = 20 \log \frac{V_o \text{ black-to-white}}{V_{n(rms)} \text{ at } B = 5 \text{ MHz}}$.
12. Measured with an input signal $V_{1\text{-}16}$ = 10 mV and a.f.c. output pin 5 symmetrically loaded with 100 k$\Omega$ to the supply voltage ($V_{11\text{-}13}$) and 100 k$\Omega$ to ground.

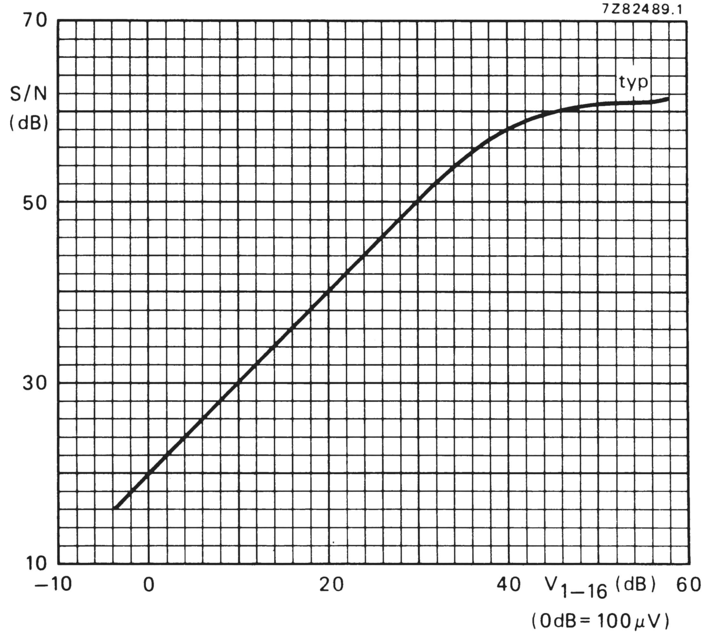


Fig. 6 Signal-to-noise ratio as a function of the input voltage ($V_{1-16}$).

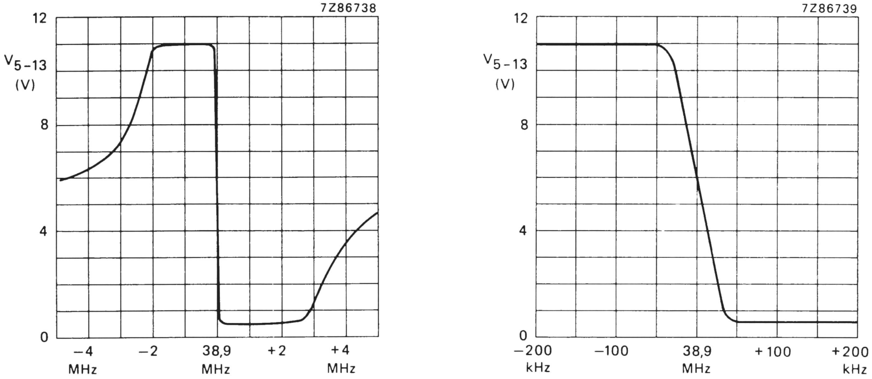


Fig. 7 A.F.C. output voltage ($V_{5-13}$) as a function of deviation of the i.f. vision carrier from its nominal frequency.

## APPLICATION INFORMATION

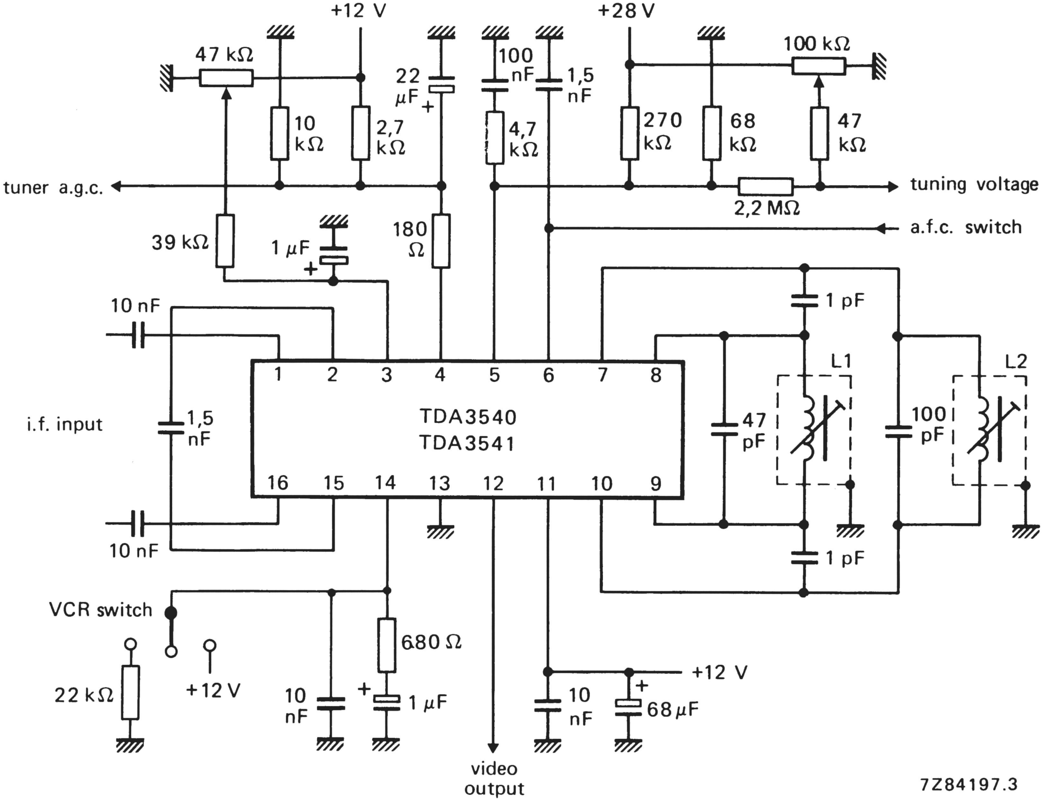

+12 V
+28 V
47 kΩ
10 kΩ
2,7 kΩ
22 µF
100 nF
4,7 kΩ
1,5 nF
270 kΩ
68 kΩ
100 kΩ
47 kΩ
tuner a.g.c.
tuning voltage
2,2 MΩ
a.f.c. switch
39 kΩ
1 µF
180 Ω
10 nF
1 pF
L1
L2
i.f. input
1,5 nF
TDA3540
TDA3541
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
47 pF
100 pF
10 nF
1 pF
VCR switch
680 Ω
+12 V
22 kΩ
+12 V
10 nF
1 µF
10 nF
68 µF
video output
7Z84197.3

Fig. 8 Typical application circuit diagram; Q of L1 and L2 = 80; $f_o$ = 38,9 MHz.

# PAL DECODER

The TDA3560 is a monolithic integrated colour decoder for the PAL standard. It combines all functions required for the identification and demodulation of PAL signals. Furthermore it contains a luminance amplifier, an RGB-matrix and amplifier. These amplifiers supply output signals up to 5 V peak-to-peak (picture information) enabling direct drive of the output stages. The circuit also contains separate inputs for data insertion, analogue as well as digital, which can be used for Teletext information, channel number display, etc.

## QUICK REFERENCE DATA

| | | | | |
|---|---|---|---|---|
| Supply voltage | $V_{1\text{-}27}$ | typ. | 12 | V |
| Supply current | $I_1$ | typ. | 85 | mA |
| Luminance input signal (peak-to-peak value) | $V_{10\text{-}27(p\text{-}p)}$ | typ. | 0,45 | V |
| Chrominance input signal (peak-to-peak value) | $V_{3\text{-}27(p\text{-}p)}$ | 55 to | 1100 | mV |
| Data input signals (peak-to-peak value) | $V_{13,15,17\text{-}27(p\text{-}p)}$ | typ. | 1 | V |
| RGB output signals at nominal contrast and saturation (peak-to-peak value) | $V_{12,14,16\text{-}27(p\text{-}p)}$ | typ. | 5 | V |
| Contrast control range | | typ. | 20 | dB |
| Saturation control range | | typ. | 50 | dB |
| Input for fast video-data signal switching | $V_{9\text{-}27}$ | typ. | 1 | V |
| Blanking input voltage | $V_{8\text{-}27}$ | typ. | 1,5 | V |
| Burst gating and black-level gating input voltage | $V_{8\text{-}27}$ | typ. | 7 | V |

## PACKAGE OUTLINE

28-lead DIL; plastic (SOT-117).

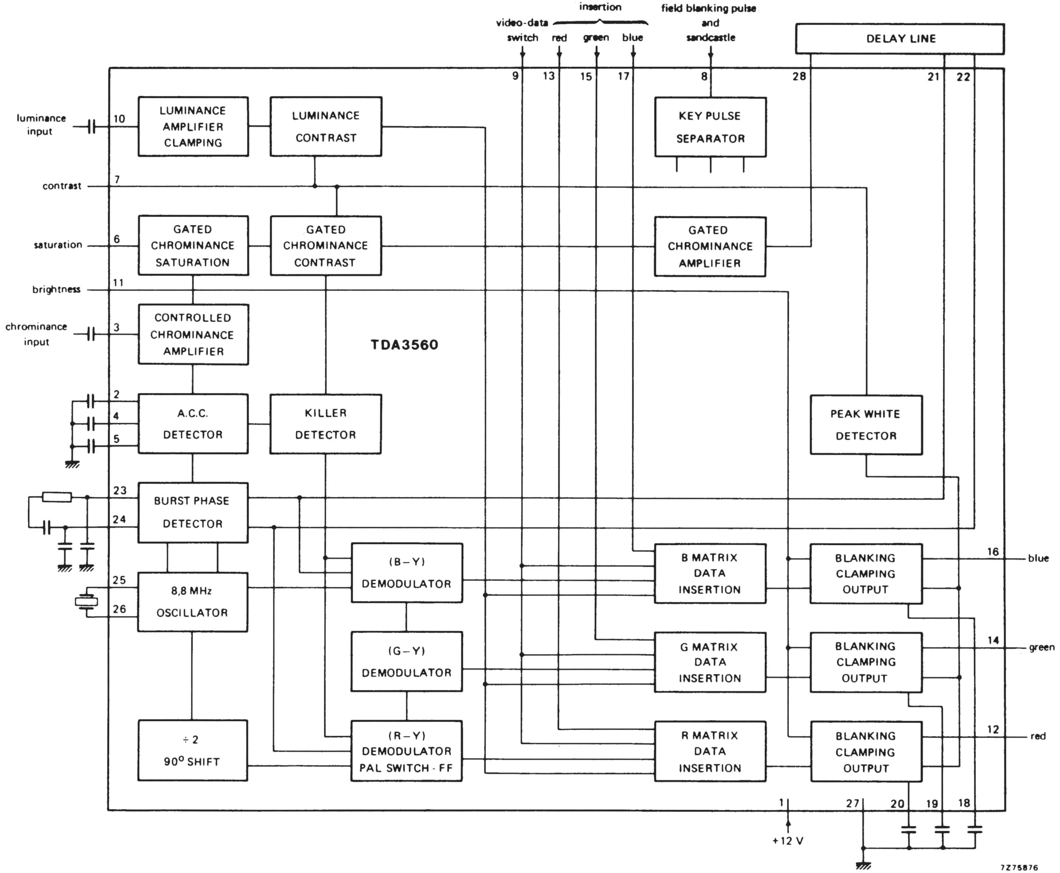

video-data switch
insertion
red
green
blue
field blanking pulse and sandcastle
DELAY LINE
9
13
15
17
8
28
21
22
luminance input
10
LUMINANCE AMPLIFIER CLAMPING
LUMINANCE CONTRAST
KEY PULSE SEPARATOR
contrast
7
saturation
6
GATED CHROMINANCE SATURATION
GATED CHROMINANCE CONTRAST
GATED CHROMINANCE AMPLIFIER
brightness
11
chrominance input
3
CONTROLLED CHROMINANCE AMPLIFIER
TDA3560
2
4
5
A.C.C. DETECTOR
KILLER DETECTOR
PEAK WHITE DETECTOR
23
24
BURST PHASE DETECTOR
25
26
8,8 MHz OSCILLATOR
(B – Y) DEMODULATOR
(G – Y) DEMODULATOR
(R – Y) DEMODULATOR PAL SWITCH - FF
÷ 2 90° SHIFT
B MATRIX DATA INSERTION
G MATRIX DATA INSERTION
R MATRIX DATA INSERTION
BLANKING CLAMPING OUTPUT
BLANKING CLAMPING OUTPUT
BLANKING CLAMPING OUTPUT
16
blue
14
green
12
red
1
+12 V
27
20
19
18
7Z75876

Fig. 1 Block diagram.

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | min. | max. | |
|---|---|---|---|---|
| Supply voltage | $V_P = V_{1\text{-}27}$ | – | 13,2 | V |
| Input saturation voltage | $V_{6\text{-}27}$ | 0 | $V_P$ | V |
| Input contrast voltage | $V_{7\text{-}27}$ | 0 | $V_P$ | V |
| Input blanking pulse and sandcastle | $V_{8\text{-}27}$ | 0 | $V_P$ | V |
| Input video-data switch voltage | $V_{9\text{-}27}$ | 0 | $V_P$ | V |
| Input brightness voltage | $V_{11\text{-}27}$ | 0 | $V_P$ | V |
| Power dissipation | see Fig. 2 | | | |
| Storage temperature | $T_{stg}$ | –25 to | + 150 | °C |
| Operating ambient temperature | $T_{amb}$ | –25 to | + 65 | °C |

## CHARACTERISTICS

$V_{1\text{-}27} = 12$ V; $V_{10\text{-}27(p\text{-}p)} = 0{,}45$ V; $V_{3\text{-}27(p\text{-}p)} = 500$ mV; $T_{amb} = 25\ ^{\circ}C$; measured in Fig. 6; unless otherwise specified

| | | | | |
|---|---|---|---|---|
| Supply voltage range | $V_P$ | typ. | 12<br>8 to 13,2 | V<br>V |
| Supply current | $I_1$ | typ. | 85 | mA |
| **Luminance amplifier** | | | | |
| Input voltage (peak-to-peak value) | $V_{10\text{-}27(p\text{-}p)}$ | typ. | 0,45 | V |
| Input current | $I_{10}$ | < | 1 | μA |
| Contrast control range | | | –17 to + 3 | dB |
| Contrast control voltage range | see Fig. 3 | | | |
| **Chrominance amplifier** | | | | |
| Input voltage (peak-to-peak value) | $V_{3\text{-}27(p\text{-}p)}$ | | 55 to 1100 | mV |
| A.C.C. control range | | > | 30 | dB |
| Output signal (peak-to-peak value) *<br>burst signal (peak-to-peak value) = 0,5 V | $V_{28\text{-}27(p\text{-}p)}$ | typ. | 1,7 | V |
| Saturation control range | | > | 50 | dB |
| Saturation control voltage range | see Fig. 4 | | | |
| Phase shift between burst and chrominance * | | < | 5° | |
| Tracking between luminance and chrominance with contrast control over a range of 10 dB, starting at maximum contrast | | typ. | 1 | dB |

---

* At nominal contrast and saturation setting. Nominal setting = maximum contrast –3 dB; maximum saturation –6 dB.

## CHARACTERISTICS (continued)

### Reference oscillator

| | | | | |
|---|---|---|---|---|
| Phase locked loop: | | | | |
| – catching range (note 1) | | > | 500 | Hz |
| – phase shift (note 2) | | < | 5° | |
| Oscillator: | | | | |
| – input resistance | $R_{26\text{-}27}$ | typ. | 300 | Ω |
| – input capacitance | $C_{26\text{-}27}$ | < | 10 | pF |
| – output resistance | $R_{25\text{-}27}$ | typ. | 200 | Ω |
| A.C.C. generation: | | | | |
| – reference voltage | $V_{4\text{-}27}$ | typ. | 4,6 | V |
| – control voltage at nominal input signal | $V_{2\text{-}27}$ | typ. | 4,7 | V |
| – control voltage without burst | $V_{2\text{-}27}$ | typ. | 2,4 | V |

### Demodulator circuit

| | | | | |
|---|---|---|---|---|
| Input burst signal amplitude (peak-to-peak value) | $V_{21,22\text{-}27(p\text{-}p)}$ | typ. | 60 | mV |
| Ratio of demodulated signals without luminance input signal | | | | |
| (B-Y)/(R-Y) | $\frac{V_{16\text{-}27}}{V_{12\text{-}27}}$ | typ. | 1,78 | |
| (G-Y)/(R-Y) | $\frac{V_{14\text{-}27}}{V_{12\text{-}27}}$ | typ. | –0,51 | |
| (G-Y)/(B-Y) | $\frac{V_{14\text{-}27}}{V_{16\text{-}27}}$ | typ. | –0,19 | |

### RGB matrix and amplifiers

| | | | | |
|---|---|---|---|---|
| Output voltage (peak-to-peak value) (note 3) | $V_{12,14,16\text{-}27(p\text{-}p)}$ | typ. | 5 | V |
| Maximum white level | | typ. | 9,3 | V |
| Birghtness control voltage range | see Fig. 5 | | | |
| Relative spread between R, G and B output signals | | < | 10 | % |
| Variation of black level with contrast control | $\Delta V$ | < | 200 | mV |
| Relative black-level variation between the three stages during variation of contrast saturation, brightness and supply voltage | | < | 20 | mV |
| Differential black-level drift over a temperature range of 40 °C | | < | 20 | mV |
| Blanking level at RGB outputs | | typ. | 2,1 | V |
| Signal-to-noise ratio of output signals (note 4) | S/N | > | 62 | dB |

Notes

1. Frequency referred to 4,4 MHz carrier frequency.
2. For ± 400 Hz deviation of the oscillator frequency.
3. For nominal setting of the controls.
4. The signal-to-noise ratio is specified as the nominal peak-to-peak output signal with respect to r.m.s. noise.

| | | | | | |
|---|---|---|---|---|---|
| Residual 8,8 MHz and higher harmonics on RGB-outputs (peak-to-peak value) | | < | 150 | mV | |
| Output impedance RGB outputs | $\|Z_o\|$ | typ. | 50 | Ω | |
| Frequency response of total luminance and RGB amplifier circuits for f = 0 to 5 MHz | | < | –3 | dB | |

**Signal insertion**

| | | | | | |
|---|---|---|---|---|---|
| Input signals for an RGB output voltage of 5 V (peak-to-peak value) | $V_{13,15,17\text{-}27(p\text{-}p)}$ | typ. | 1 | V | |
| Difference between the black levels of the RGB signals and the inserted signals at the output | ΔV | < | 260 | mV | ← |
| Output rise time | $t_r$ | typ. | 50 | ns | |
| Differential delay time for the three channels | $t_d$ | < | 40 | ns | |

**Video-data switching**

| | | | | |
|---|---|---|---|---|
| Input voltage for switching from video to inserted signals | $V_{9\text{-}27}$ | | 0,9 to 2 | V |
| Input voltage for no data insertion | $V_{9\text{-}27}$ | < | 0,3 | V |
| Delay between signal switching at the output and the signal switching input pulse at pin 9 | $t_d$ | < | 20 | ns |

**Sandcastle and field blanking input** (pin 8)

| | | | | |
|---|---|---|---|---|
| Burst gate and clamping pulse | $V_{8\text{-}27}$ | > | 7,5 | V |
| RGB blanking level | | | | |
| on | $V_{8\text{-}27}$ | | 2 to 6,5 | V |
| off | $V_{8\text{-}27}$ | < | 0,8 | V |

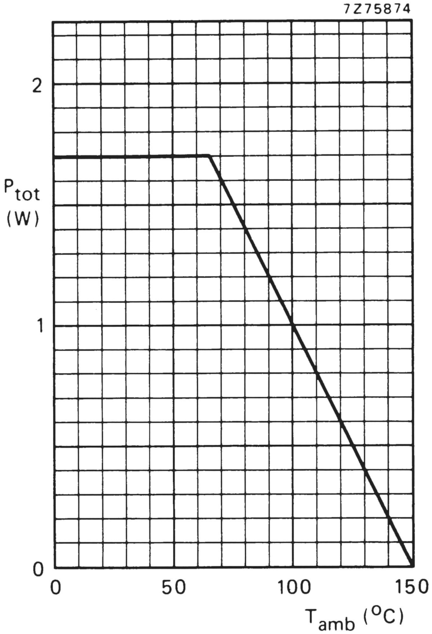


Fig. 2 Power derating curve.

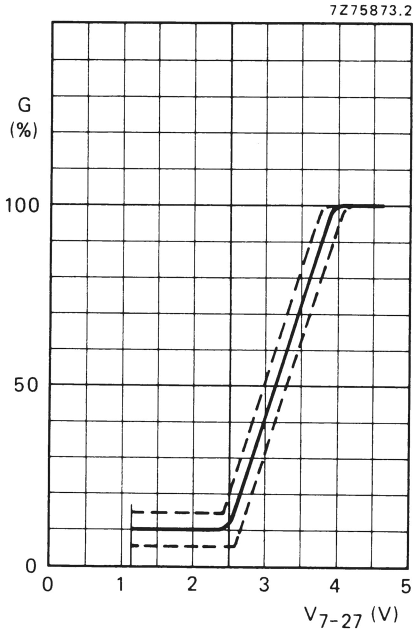


Fig. 3 Contrast control voltage range.

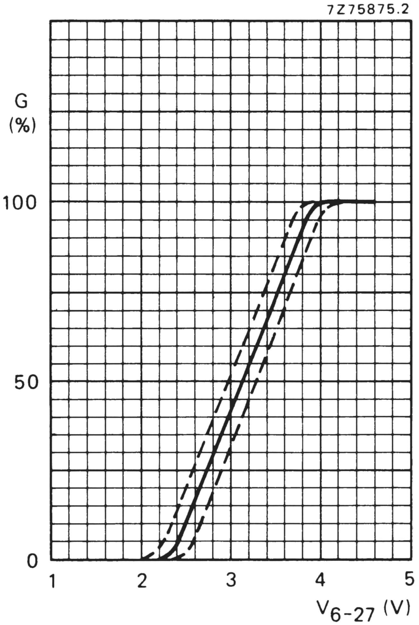


Fig. 4 Saturation control voltage range.

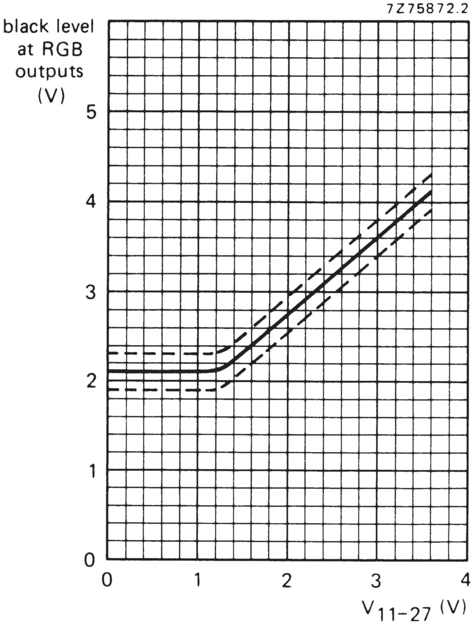


Fig. 5 Brightness control voltage range.

## APPLICATION INFORMATION

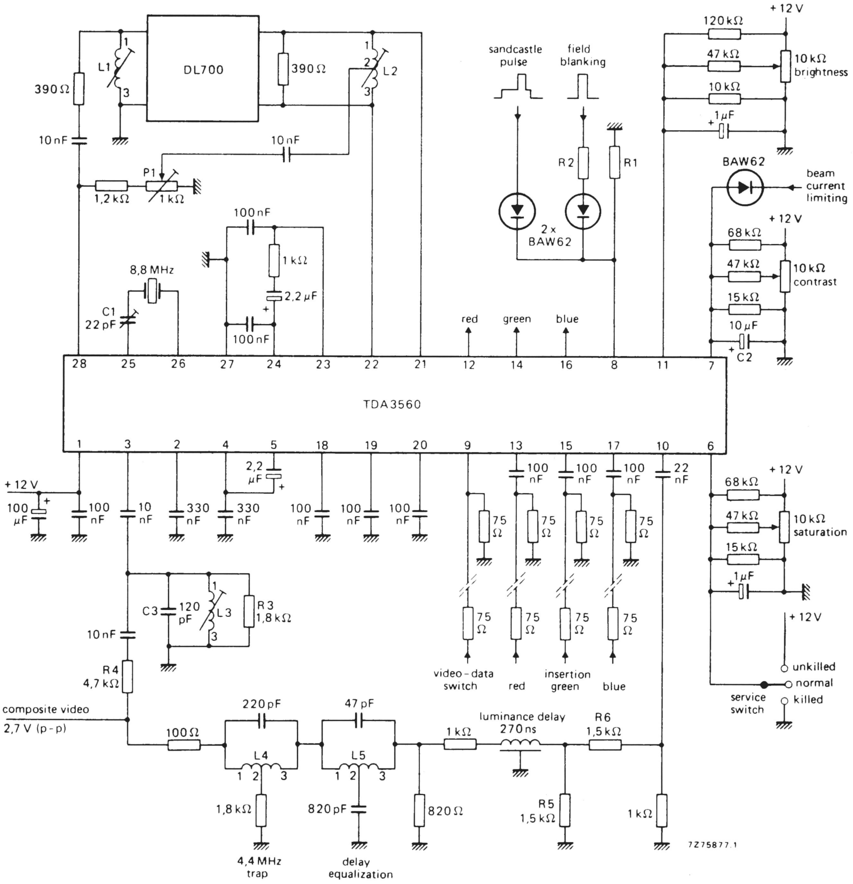

DL700
L1
1
3
390 Ω
390 Ω
1
2
3
L2
10 nF
10 nF
P1
1,2 kΩ
1 kΩ
100 nF
1 kΩ
2,2 μF
100 nF
8,8 MHz
C1
22 pF
sandcastle pulse
field blanking
R2
R1
2 x BAW62
red
green
blue
+ 12 V
120 kΩ
47 kΩ
10 kΩ
1 μF
10 kΩ brightness
BAW62
beam current limiting
+ 12 V
68 kΩ
47 kΩ
15 kΩ
10 μF
C2
10 kΩ contrast
28
25
26
27
24
23
22
21
12
14
16
8
11
7
TDA3560
1
3
2
4
5
18
19
20
9
13
15
17
10
6
+ 12 V
100 μF
100 nF
10 nF
330 nF
330 nF
2,2 μF
100 nF
100 nF
100 nF
100 nF
100 nF
100 nF
22 nF
75 Ω
75 Ω
75 Ω
75 Ω
75 Ω
75 Ω
75 Ω
75 Ω
video-data switch
red
insertion green
blue
+ 12 V
68 kΩ
47 kΩ
15 kΩ
1 μF
10 kΩ saturation
+ 12 V
unkilled
normal
killed
service switch
C3
120 pF
L3
1
3
R3
1,8 kΩ
10 nF
R4
4,7 kΩ
composite video
2,7 V (p-p)
100 Ω
220 pF
L4
1
2
3
1,8 kΩ
4,4 MHz trap
47 pF
L5
1
2
3
820 pF
delay equalization
820 Ω
1 kΩ
luminance delay
270 ns
R6
1,5 kΩ
R5
1,5 kΩ
1 kΩ
7Z75877.1

Fig. 6 Application circuit.
For adjustments see page 10.

## APPLICATION INFORMATION

The function is described against the corresponding pin number.

### 1. + 12 V power supply

The circuit gives good operation in a supply voltage range between 8 and 13,2 V provided that the supply voltage for the controls is equal to the supply voltage for the TDA3560. All signal and control levels have a linear dependency on the supply voltage. The current taken by the device at 12 V is typically 85 mA. It is linearly dependent on the supply voltage.

### 2. Control voltage for identification

This pin requires a detection capacitor of about 330 nF for correct operation. The voltages available under various signal conditions are given in the specification.

### 3. Chrominance input

The chroma signal must be a.c.-coupled to the input. Its amplitude must be between 55 mV and 1100 mV peak-to-peak (25 mV to 500 mV peak-to-peak burst signal). All figures for the chroma signals are based on a colour bar signal with 75% saturation, that is the burst-to-chroma ratio of the input signal is 1 : 2,25.

### 4. Reference voltage A.C.C. detector

This pin must be decoupled by a capacitor of about 330 nF. The voltage at this pin is 4,6 V.

### 5. Control voltage A.C.C.

The A.C.C. is obtained by synchronous detection of the burst signal followed by a peak detector. A good noise immunity is obtained in this way and an increase of the colour for weak input signals is prevented. The recommended capacitor value at this pin is 2,2 μF.

### 6. Saturation control

The saturation control range is in excess of 50 dB. The control voltage range is 2 to 4 V. Saturation control is a linear function of the control voltage.

When the colour killer is active, the saturation control voltage is reduced to a low level if the resistance of the external saturation control network is sufficiently high. Then the chroma amplifier supplies no signal to the demodulator. Colour switch-on can be delayed by proper choice of the time constant for the saturation control setting circuit.

When the saturation control pin is connected to the power supply the colour killer circuit is overruled so that the colour signal is visible on the screen. In this way it is possible to adjust the oscillator frequency without using a frequency counter (see also pins 25 and 26).

### 7. Contrast control

The contrast control range is 20 dB for a control voltage change from + 2 to + 4 V. Contrast control is a linear function of the control voltage. The output signal is suppressed when the control voltage is 1 V or less. If one or more output signals surpasses the level of 9 V the peak white limiter circuit becomes active and reduces the output signals via the contrast control by discharging C2 via an internal current sink.

### 8. Sandcastle and field blanking input

The output signals are blanked if the amplitude of the input pulse is between 2 and 6,5 V. The burst gate and clamping circuits are activated if the input pulse exceeds a level of 7,5 V.
The higher part of the sandcastle pulse should start just after the sync pulse to prevent clamping of video signal on the sync pulse. The width should be about 4 μs for proper A.C.C. operation.

### 9. Video-data switching

The insertion circuit is activated by means of this input by an input pulse between 1 V and 2 V. In that condition, the internal RGB signals are switched off and the inserted signals are supplied to the output amplifiers. If only normal operation is wanted this pin should be connected to the negative supply. The switching times are very short (< 20 ns) to avoid coloured edges of the inserted signals on the screen.

### 10. Luminance signal input

The input signal should have a peak-to-peak amplitude of 0,45 V (peak white to sync) to obtain a black-white output signal of 5 V at nominal contrast. It must be a.c.-coupled to the input by a capacitor of about 22 nF. The signal is clamped at the input to an internal reference voltage.
A 1 kΩ luminance delay line can be applied because the luminance input impedance is made very high. Consequently the charging and discharging currents of the coupling capacitor are very small and do not influence the signal level at the input noticeably. Additionally the coupling capacitor value may be small.

### 11. Brightness control

The black level of the RGB outputs can be set by the voltage on this pin (see Fig. 5). The minimum black level is identical to the blanking level. The black level can be set higher than 4 V however the available output signal amplitude is reduced (see pin 7). Brightness control also operates on the black level of the inserted signals.

### 12, 14, 16. RGB outputs

The output circuits for red, green and blue are identical. Output signals are 5 V (black-white) for nominal input signals and control settings. The black levels of the three outputs have the same value. The blanking level at the outputs is 2 V. The peak white level is limited to 9 V. When this level is exceeded the output signal amplitude is reduced via the contrast control (see pin 7).

### 13, 15, 17. Inputs for external RGB signals

The external signals must be a.c.-coupled to the inputs via a coupling capacitor of about 100 nF. Source impedance should not exceed 150 Ω. The input signal required for a 5 V peak-to-peak output signal is 1 V peak -to-peak. At the RGB outputs the black level of the inserted signal is identical to that of normal RGB signals. When these inputs are not used the coupling capacitors have to be connected to the negative supply.

### 18, 19, 20. Black level clamp capacitors

The black level clamp capacitors for the three channels are connected to these pins. The value of each capacitor should be about 100 nF.

### 21, 22. Inputs (B-Y) and (R-Y) demodulators

The input signal is automatically fixed to the required level by means of the burst phase detector and A.C.C. generator which are connected to this pin and pin 22. As the burst (applied differentially to those pins) is kept constant by the A.C.C., the colour difference signals automatically have the correct value.

## APPLICATION INFORMATION (continued)

### 23, 24. Burst phase detector outputs

At these pins the output of the burst phase detector is filtered and controls the reference oscillator. An adequate catching range is obtained with the time constants given in the application circuit (see Fig. 6).

### 25, 26. Reference oscillator

The frequency of the oscillator is adjusted by the variable capacitor C1. For frequency adjustment interconnect pin 23 and pin 24. The frequency can be measured by connecting a suitable frequency counter to pin 25.

### 28. Output of the chroma amplifier

Both burst and chroma signals are available at the output. The burst-to-chroma ratio at the output is identical to that at the input for nominal control settings. The burst signal is not affected by the controls. The amplitude of the input signal to the demodulator is kept constant by the A.C.C. Therefore the output signal at pin 28 will depend on the signal loss in the delay line.

Adjustments (see Fig. 6)

| | | |
|---|---|---|
| C1 | 8,8 MHz oscillator | |
| L1 | phase delay line | = 10,7 $\mu$H |
| L2 | nominal value | = 10,7 $\mu$H |
| L3 | 4,4 MHz chrominance input filter | = 10,7 $\mu$H = L1 |
| L4 | 4,4 MHz trap in luminance signal line | = 5,6 $\mu$H |
| L5 | delay equalization | = 66,1 $\mu$H |
| P1 | amplitude of direct chroma signal | |
| R1<br>R2 | field blanking $\frac{R1}{R1 + R2}$ x field blanking amplitude 2,0 V to 6,5 V. | |

For a video input voltage of 1 V peak-to-peak: R4 = 1 k$\Omega$; R3, R5 and R6 can be omitted.

# PAL DECODER

The TDA3561A is a decoder for the PAL colour television standard. It combines all functions required for the identification and demodulation of PAL signals. Furthermore it contains a luminance amplifier, an RGB-matrix and amplifier. These amplifiers supply output signals up to 5 V peak-to-peak (picture information) enabling direct drive of the discrete output stages. The circuit also contains separate inputs for data insertion, analogue as well as digital, which can be used for text display systems (e.g. (Teletext/ broadcast antiope), channel number display, etc. Additional to the TDA3560, the circuit includes the following features:

- The peak white limiter is only active during the time that the 9,3 V level at the output is exceeded. The start of the limiting function is delayed by one line period. This avoids peak white limiting by test patterns which have abrupt transitions from colour to white signals.
- The brightness control is obtained by inserting a variable pulse in the luminance channel. Therefore the ratio of brightness variation and signal amplitude at the three outputs will be identical and independent of the difference in gain of the three channels. Thus discolouring due to adjustment of contrast and brightness is avoided.
- Improved suppression of the internal RGB signals when the device is switched to external signals, and vice versa.
- Non-synchronized external RGB signals do not disturb the black level of the internal signals.
- Improved suppression of the residual 4,4 MHz signal in the RGB output stages.
- Cascoded stages in the demodulators and burst phase detector minimize the radiation of the colour demodulator inputs.
- High current capability of the RGB outputs and the chrominance output.

## QUICK REFERENCE DATA

| | | | | |
|---|---|---|---|---|
| Supply voltage | $V_{1-27}$ | type. | 12 | V |
| Supply current | $I_1$ | typ. | 85 | mA |
| Luminance input signal (peak-to-peak value) | $V_{10-27(p-p)}$ | typ. | 0,45 | V |
| Chrominance input signal (peak-to-peak value) | $V_{3-27(p-p)}$ | | 55 to 1100 | mV |
| Data input signals (peak-to-peak value) | $V_{13,15,17-27(p-p)}$ | typ. | 1 | V |
| RGB output signals at nominal contrast and saturation (peak-to-peak value) | $V_{12,14,16-27(p-p)}$ | typ. | 5,25 | V |
| Contrast control range | | typ. | 20 | dB |
| Saturation control range | | min. | 50 | dB |
| Input voltage for data insertion | $V_{9-27}$ | min. | 0,9 | V |
| Blanking input voltage | $V_{8-27}$ | typ. | 1,5 | V |
| Burst gating and black-level gating input voltage | $V_{8-27}$ | typ. | 7 | V |

## PACAAGE OUTLINE

28-lead DIL; plastic (SOT-117).

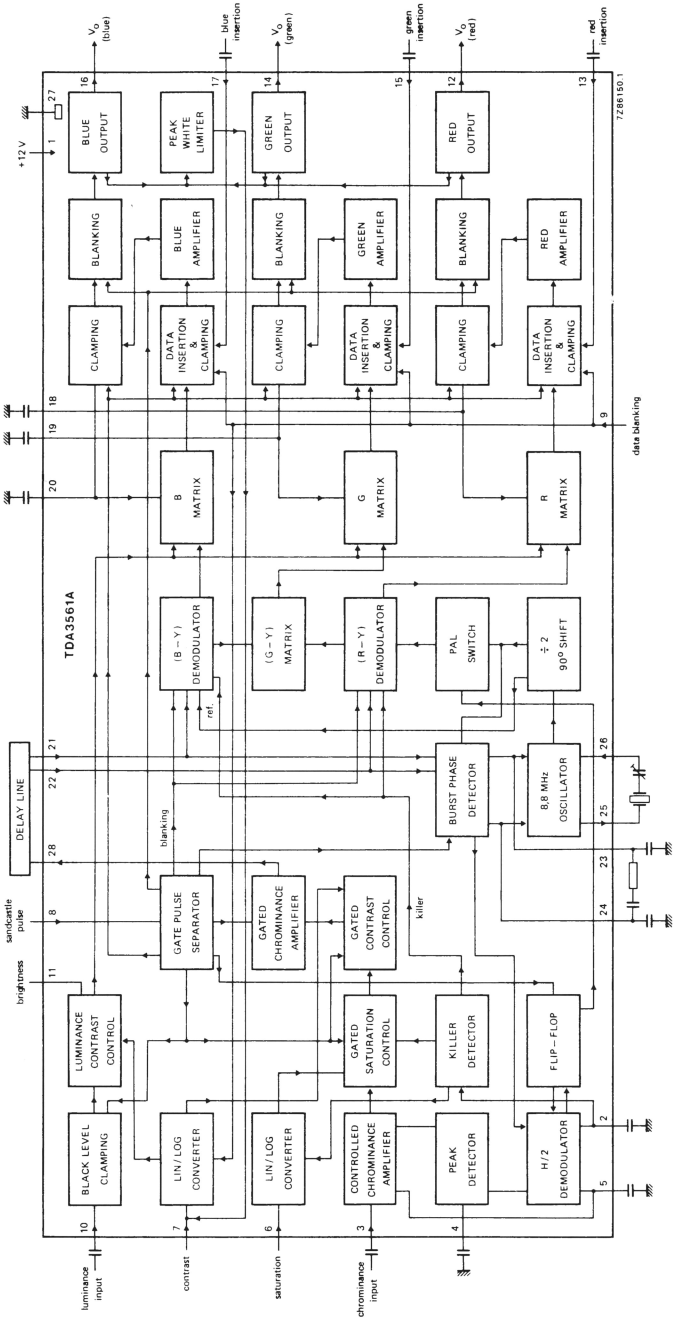

TDA3561A
7Z86150.1
BLUE OUTPUT
PEAK WHITE LIMITER
GREEN OUTPUT
RED OUTPUT
BLANKING
BLUE AMPLIFIER
GREEN AMPLIFIER
RED AMPLIFIER
CLAMPING
DATA INSERTION & CLAMPING
B MATRIX
G MATRIX
R MATRIX
(B − Y) DEMODULATOR
(G − Y) MATRIX
(R − Y) DEMODULATOR
PAL SWITCH
÷ 2 90° SHIFT
DELAY LINE
BURST PHASE DETECTOR
8,8 MHz OSCILLATOR
GATE PULSE SEPARATOR
GATED CHROMINANCE AMPLIFIER
GATED CONTRAST CONTROL
LUMINANCE CONTRAST CONTROL
GATED SATURATION CONTROL
KILLER DETECTOR
FLIP-FLOP
BLACK LEVEL CLAMPING
LIN/LOG CONVERTER
LIN/LOG CONVERTER
CONTROLLED CHROMINANCE AMPLIFIER
PEAK DETECTOR
H/2 DEMODULATOR
$V_o$ (blue)
blue insertion
$V_o$ (green)
green insertion
$V_o$ (red)
red insertion
+12 V
data blanking
blanking
ref.
killer
sandcastle pulse
brightness
luminance input
contrast
saturation
chrominance input
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28

Fig. 1 Block diagram.

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | | |
|---|---|---|---|---|
| Supply voltage | $V_P = V_{1\text{-}27}$ | max. | 13,2 | V |
| Total power dissipation; see also Fig. 2 | $P_{tot}$ | max. | 1,7 | W |
| Storage temperature range | $T_{stg}$ | | −25 to + 150 | °C |
| Operating ambient temperature range | $T_{amb}$ | | −25 to + 65 | °C |

## THERMAL RESISTANCE

| | | | | |
|---|---|---|---|---|
| From junction to ambient | $R_{th\ j\text{-}a}$ | = | 50 | K/W |

## CHARACTERISTICS

$V_P = V_{1\text{-}27} = 12$ V; $T_{amb} = 25$ °C; unless otherwise specified

| | | | | |
|---|---|---|---|---|
| Supply voltage | $V_P = V_{1\text{-}27}$ | typ. | 12 | V |
| | | | 8 to 13,2 | V |
| Supply current | | typ. | 85 | mA |
| | | $<$ | 115 | mA |
| Total power dissipation | $P_{tot}$ | typ. | 1,0 | W |
| | | $<$ | 1,4 | W |
| **Luminance input** (pin 10) | | | | |
| Input voltage (peak-to-peak value); note 1 | $V_{10\text{-}27(p\text{-}p)}$ | typ. | 0,45 | V |
| Input level before clipping | $V_{10\text{-}27}$ | $<$ | 2 | V |
| Input current; input level 2 V, clamp not active | $I_{10}$ | typ. | 0,15 | μA |
| | | $<$ | 1 | μA |
| Contrast control range (see Fig. 3) | | | −17 to + 3 | dB |
| Control voltage for 40 dB attenuation | $V_{7\text{-}27}$ | typ. | 1,2 | V |
| Input current contrast control at $V_{7\text{-}27} = 3$ V | $I_7$ | $<$ | 10 | μA |
| **Chrominance amplifier** | | | | |
| Input voltage (peak-to-peak value); note 2 | $V_{3\text{-}27(p\text{-}p)}$ | typ. | 550 | mV |
| | | | 55 to 1100 | mV |
| Input impedance | $\lvert Z_{3\text{-}27}\rvert$ | typ. | 9 | kΩ |
| | | | 6 to 12 | kΩ |
| Input capacitance | $C_{3\text{-}27}$ | typ. | 4 | pF |
| | | $<$ | 6 | pF |
| A.C.C. control range | | $>$ | 30 | dB |
| Change of the burst signal at the output over the whole control range | | $<$ | 1,5 | dB |
| Gain at nominal contrast/saturation pin 3 to pin 28; note 3 | | $>$ | 32 | dB |
| Output signal (peak-to-peak value) at nominal contrast/saturation; burst signal: 0,5 V peak to peak | $V_{28\text{-}27(p\text{-}p)}$ | typ. | 1,7 | V |
| Maximum output voltage (peak-to-peak value) $R_L = 2$ kΩ | $V_{28\text{-}27(p\text{-}p)}$ | typ. | 4,0 | V |

DEVELOPMENT SAMPLE DATA

## CHARACTERISTICS (continued)

### Chrominance amplifier (continued)

| | | | | |
|---|---|---|---|---|
| Distortion of chrominance amplifier at $V_{28\text{-}27(p\text{-}p)}$ = 2 V up to $V_{3\text{-}27(p\text{-}p)}$ = 1 V | d | typ. | 1,5 | % |
| | | < | 5 | % |
| Frequency response between 0 and 5 MHz | | | −2 | dB |
| Saturation control range (see Fig. 4) | | > | 50 | dB |
| Input current saturation control at $V_{6\text{-}27}$ = 3 V | $I_6$ | < | 15 | μA |
| Tracking between luminance and chrominance with contrast control over a range of 10 dB | | < | 2 | dB |
| Cross-coupling between luminance and chrominance amplifier; note 10 | | < | −46 | dB |
| Signal-to-noise ratio at nominal input signal; note 11 | S/N | > | 56 | dB |
| Phase shift between burst and chrominance at nominal contrast/saturation | $\Delta\varphi$ | < | ± 5° | |
| Output impedance of chrominance amplifier | $\lvert Z_{28\text{-}27} \rvert$ | typ. | 25 | Ω |
| Maximum output current | $I_{28}$ | < | 15 | mA |

### Reference part

| | | | | |
|---|---|---|---|---|
| Phase locked loop: | | | | |
| – catching range; note 4 | | > | 500 | Hz |
| | | typ. | 700 | Hz |
| – phase shift; note 5 | | < | 5° | |
| Oscillator: | | | | |
| – temperature coefficient of oscillator frequency; note 4 | | typ. | −1,5 | Hz/K |
| – frequency deviation for $V_P$ changing from 10 to 13,2 V; note 4 | | typ. | 40 | Hz |
| – input resistance (pin 26) | $R_{26\text{-}27}$ | typ. | 340 | Ω |
| | | | 260 to 420 | Ω |
| – input capacitance (pin 26) | $C_{26\text{-}27}$ | < | 10 | pF |
| – output resistance (pin 25) | $R_{25\text{-}27}$ | typ. | 150 | Ω |
| | | | 100 to 200 | Ω |
| – output voltage (peak-to-peak value; pin 25) | $V_{25\text{-}27(p\text{-}p)}$ | typ. | 700 | mV |
| A.C.C. generation: | | | | |
| – reference voltage (pin 4) | $V_{4\text{-}27}$ | typ. | 4,9 | V |
| – control voltage at nominal input signal (pin 2) | $V_{2\text{-}27}$ | typ. | 5,1 | V |
| – control voltage without chrominance input (pin 2) | $V_{2\text{-}27}$ | typ. | 2,65 | V |
| – colour-off voltage (pin 2) | $V_{2\text{-}27}$ | typ. | 3,15 | V |
| – colour-on voltage (pin 2) | $V_{2\text{-}27}$ | typ. | 3,4 | V |
| – identification-on voltage (pin 2) | $V_{2\text{-}27}$ | typ. | 1,9 | V |
| – change in burst amplitude with supply voltage (± 10%) | | proportional | | |
| – change in burst amplitude with temperature | | typ. | 0,1 | %/K |
| | | < | 0,25 | %/K |
| – voltage at pin 5 at nominal input signal | $V_{5\text{-}27}$ | typ. | 5 | V |

**Demodulator part**

| | | | | |
|---|---|---|---|---|
| Input burst signal amplitude (peak-to-peak value) between pins 21 and 22; note 6 | $V_{21\text{-}22(p\text{-}p)}$ | typ. | 100 | mV |
| Input impedance between pins 21 and 22 | $\lvert Z_{21\text{-}22}\rvert$ | typ. | 2 | kΩ |
| Ratio of demodulated signals for equal input signals at pins 21 and 22 (B–Y)/(R–Y) | $\frac{V_{16\text{-}27}}{V_{12\text{-}27}}$ | typ. | 1,78 ± 10% | |
| (G–Y)/(R–Y); no (B–Y) signal | $\frac{V_{14\text{-}27}}{V_{12\text{-}27}}$ | typ. | –0,51 ± 10% | |
| (G–Y)/(B–Y); no (R–Y) signal | $\frac{V_{14\text{-}27}}{V_{16\text{-}27}}$ | typ. | –0,19 ± 25% | |
| Frequency response between 0 and 1 MHz | | | –3 | dB |
| Cross talk between colour demodulated signals | | > | 40 | dB |
| Phase difference between (R–Y) signal and (R–Y) reference signal | | < | 5° | |
| Phase difference between (R–Y) and (B–Y) reference signals | | typ. | 90°<br>85 to 95° | |

**R.G.B. matrix and amplifiers**

| | | | | |
|---|---|---|---|---|
| Output voltage (peak-to-peak value) at nominal luminance/contrast (black to white); note 3 | $V_{12,14,16\text{-}27(p\text{-}p)}$ | typ. | 5,4<br>4,5 to 6,3 | V<br>V |
| Output voltage (peak-to-peak value) of the RED channel at nominal contrast/saturation and no luminance signal at the input, (R–Y) signal | $V_{12\text{-}27(p\text{-}p)}$ | typ. | 5,25<br>3,7 to 6,7 | V<br>V |
| Maximum peak white level; note 7 | | typ. | 9,3<br>9,0 to 9,6 | V<br>V |
| Maximum output current | $I_{12,14,16}$ | < | 15 | mA |
| Black level at the output for a brightness control voltage of 2 V | $V_{12,14,16\text{-}27}$ | typ. | 2,6 | V |
| Difference in black level between the three channels at an output level of 3 V; note 8 | ΔV | < | 200 | mV |
| Black level shift with vision contents | | < | 40 | mV |
| Brightness control voltage range | see Fig. 5 | | | |
| Input current brightness control | $I_{11}$ | < | 50 | μA |
| Variation of black level with temperature | ΔV | typ.<br>< | 0,35<br>1,0 | mV/K<br>mV/K |
| Variation of black level with contrast control | ΔV | typ.<br>< | 10<br>200 | mV<br>mV |
| Relative spread between the R, G and B output signals | | < | 10 | % |
| Relative black-level variation between the three channels during variation of contrast and supply voltage | | typ.<br>< | 0<br>20 | mV<br>mV |

**CHARACTERISTICS** (continued)

**RGB matrix and amplifier** (continued)

| | | | |
|---|---|---|---|
| Differential black-level drift over a temperature range of 40 °C | | typ.<br>< | 0 mV<br>20 mV |
| Blanking level at the RGB outputs | | typ. | 2,1 V<br>1,9 to 2,3 V |
| Difference in blanking level of the three channels | | typ. | 0 mV |
| Differential blanking level drift over a temperature range of 40 °C | | typ. | 0 mV |
| Tracking of output black level with supply voltage | $\frac{\Delta V_{bl}}{V_{bl}} \times \frac{V_P}{\Delta V_P}$ | typ. | 1,1 |
| Signal-to-noise ratio of output signals; note 11 | S/N | > | 62 dB |
| Residual 4,4 MHz signal at RGB outputs (peak-to-peak value) | | typ.<br>< | 40 mV<br>150 mV |
| Residual 8,8 MHz signal and higher harmonics at the RGB outputs (peak-to-peak value) | | typ.<br>< | 75 mV<br>150 mV |
| Output impedance of RGB outputs | $\lvert Z_{12,14,16\text{-}27} \rvert$ | typ. | 50 Ω |
| Frequency response of total luminance and RGB amplifier circuits for f = 0 to 5 MHz | | < | −3 dB |

**Signal insertion** (pins 13,15 and 17)

| | | | |
|---|---|---|---|
| Input signals (peak-to-peak value) for an RGB output voltage of 5 V peak-to-peak | $V_{13,15,17\text{-}27(p\text{-}p)}$ | typ. | 1 V<br>0,85 to 1,1 V |
| Difference between the black levels of the RGB signals and the inserted signals at the output; note 9 | ΔV | < | 260 mV |
| Output rise time | $t_r$ | typ.<br>< | 40 ns<br>80 ns |
| Differential delay time for the three channels | $t_d$ | typ.<br>< | 0 ns<br>40 ns |
| Input current | $I_{13,15,17}$ | < | 10 μA |

**Data blanking** (pin 9)

| | | | |
|---|---|---|---|
| Input voltage for no data insertion | $V_{9\text{-}27}$ | < | 0,4 V |
| Input voltage for data insertion | $V_{9\text{-}27}$ | > | 0,9 V |
| Maximum input voltage | $V_{9\text{-}27}$ | < | 3 V |
| Delay of data blanking | $t_d$ | < | 20 ns |
| Input current | $I_9$ | < | 35 μA |
| Input impedance | $\lvert Z_{9\text{-}27} \rvert$ | typ. | 10 kΩ |
| Suppression of the internal RGB signals when $V_{9\text{-}27} > 0{,}9$ V | | > | 46 dB |

**Sandcastle input** (pin 8)

| | | |
|---|---|---|
| Level at which the RGB blanking is activated | $V_{8\text{-}27}$ | typ. 1,5 V<br>1 to 2 V |
| Level at which burst gating and clamping pulse are separated | $V_{8\text{-}27}$ | typ. 7,0 V<br>6,5 to 7,5 V |
| Delay between black level clamping and burst gating pulse | $t_d$ | typ. 0,4 μs |
| Input current for: | | |
| $V_{8\text{-}27}$ = 0 to 1 V | $-I_8$ | < 1 mA |
| $V_{8\text{-}27}$ = 1 to 8,5 V | $I_8$ | typ. 20 μA |
| $V_{8\text{-}27}$ = 8,5 to 12 V | $I_8$ | < 2 mA |

**Notes to the characteristics**

1. Signal with the negative-going sync; amplitude includes sync pulse amplitude.
2. Indicated is a signal for a colour bar with 75% saturation, so chrominance to burst ratio is 2,2 : 1.
3. Nominal contrast is specified as the maximum contrast −3 dB and nominal saturation as the maximum saturation −6 dB.
4. All frequency variations are referred to the 4,4 MHz carrier frequency.
5. For ± 400 Hz deviation of the oscillator frequency.
6. These signal amplitudes are determined by the a.c.c. circuit of the reference part.
7. When this level is exceeded, the amplitude of the output signal is reduced via a discharge of the capacitor at pin 7 (contrast control). The start of the peak white limiting action has a delay of one line period.
8. The variation of the black level depends directly on the gain of each channel during brightness control in the three channels. As a consequence, the black levels at the outputs (for output levels above or below 3 V) can have a difference which exceeds 200 mV. Because the amplitude and the black level change with brightness control have a direct relationship, no discolouring can occur, caused by adjustment of contrast and brightness.
9. This difference occurs when the source impedance of the data signal inputs is 150 Ω and the black level clamp pulse duration is 4 μs (sandcastle pulse). A lower difference is obtained when the impedance is lower.
10. Cross-coupling is measured under the following condition. Input signals nominal, contrast and saturation such that nominal output signals are obtained. The signals at the output at which no signal should be available must be compared with the nominal output signal at that output.
11. The signal-to-noise ratio is specified as peak-to-peak signal with respect to r.m.s. noise.

DEVELOPMENT SAMPLE DATA

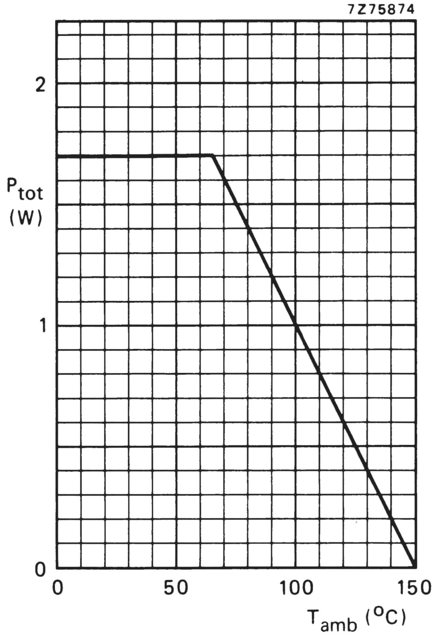


Fig. 2 Power derating curve.

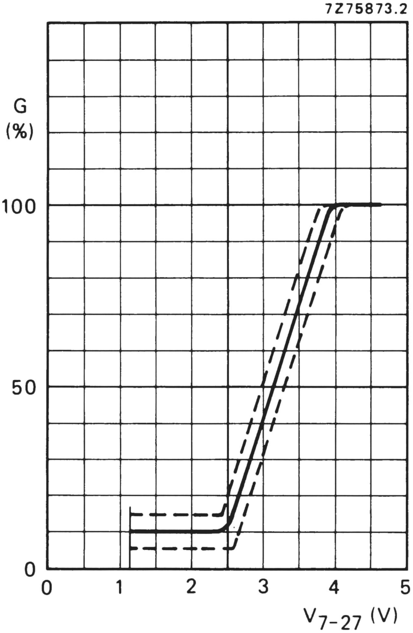


Fig. 3 Contrast control voltage range.

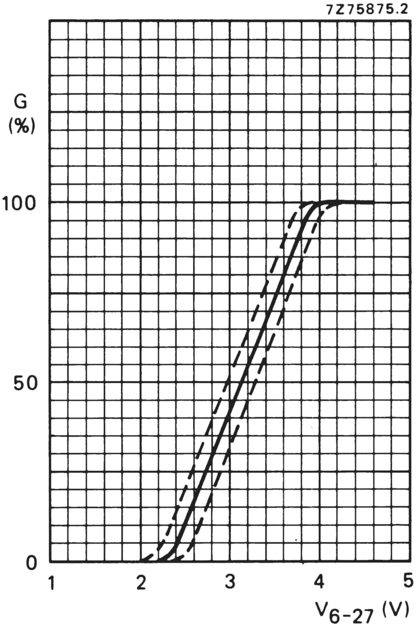


Fig. 4 Saturation control voltage range.

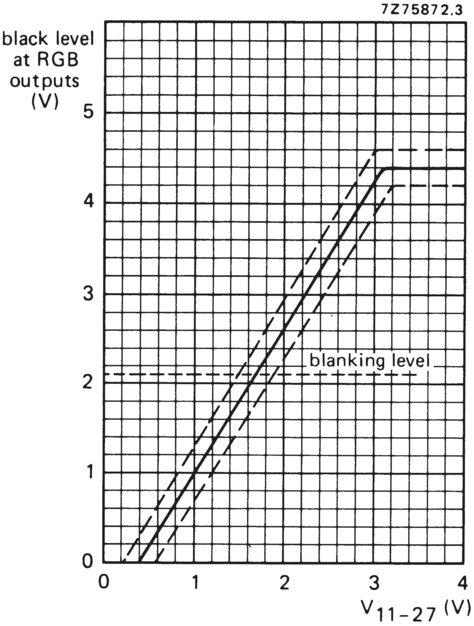


Fig. 5 Brightness control voltage range.

## APPLICATION INFORMATION

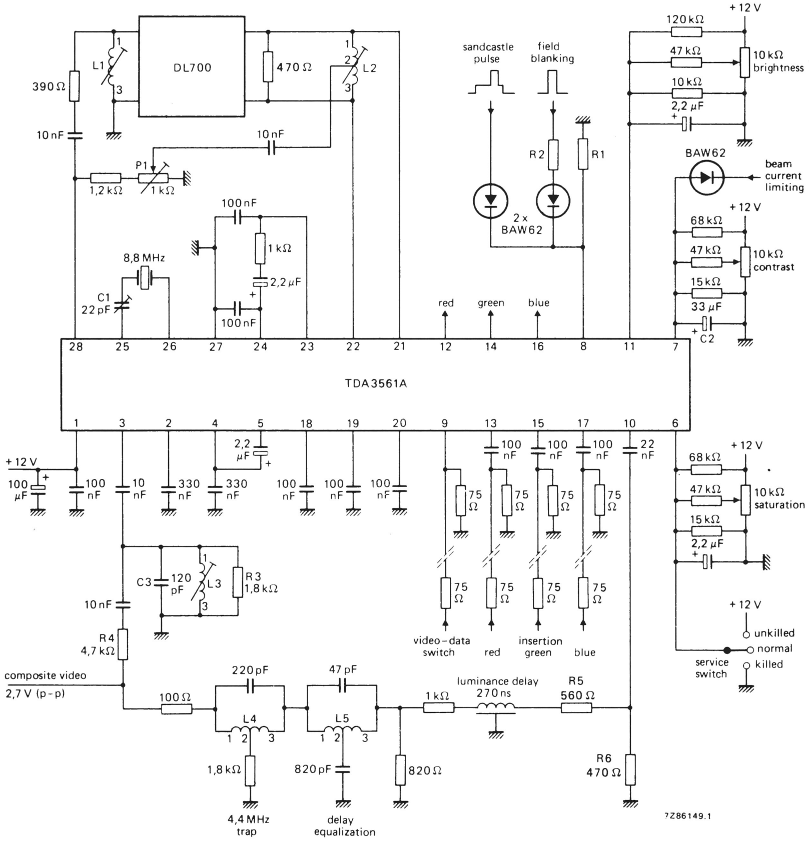

DL700
L1
390 Ω
10 nF
470 Ω
L2
10 nF
P1
1,2 kΩ
1 kΩ
100 nF
1 kΩ
2,2 µF
100 nF
8,8 MHz
C1
22 pF
sandcastle pulse
field blanking
R2
R1
2 x BAW62
red
green
blue
+12 V
120 kΩ
47 kΩ
10 kΩ brightness
10 kΩ
2,2 µF
BAW62
beam current limiting
68 kΩ
47 kΩ
10 kΩ contrast
15 kΩ
33 µF
C2
TDA3561A
28 25 26 27 24 23 22 21 12 14 16 8 11 7
1 3 2 4 5 18 19 20 9 13 15 17 10 6
+12 V
100 µF
100 nF
10 nF
330 nF
330 nF
2,2 µF
100 nF
100 nF
100 nF
100 nF
100 nF
100 nF
22 nF
75 Ω
68 kΩ
47 kΩ
10 kΩ saturation
15 kΩ
2,2 µF
C3
120 pF
L3
R3 1,8 kΩ
10 nF
R4 4,7 kΩ
video-data switch
red
insertion green
blue
+12 V
unkilled
normal
killed
service switch
composite video 2,7 V (p-p)
100 Ω
220 pF
L4
47 pF
L5
1 kΩ
luminance delay 270 ns
R5 560 Ω
1,8 kΩ
4,4 MHz trap
820 pF
delay equalization
820 Ω
R6 470 Ω
7Z86149.1

Fig. 6 Application circuit.

DEVELOPMENT SAMPLE DATA

Adjustments (see Fig. 6)

| | | |
|---|---|---|
| C1 | 8,8 MHz oscillator | |
| L1 | phase delay line | = 10,7 µH |
| L2 | nominal value | = 10,7 µH |
| L3 | 4,4 MHz chrominance input filter | = 10,7 µH = L1 |
| L4 | 4,4 MHz trap in luminance signal line | = 5,6 µH |
| L5 | delay equalization | = 66,1 µH |
| P1 | amplitude of direct chroma singal | |
| R1<br>R2 | field blanking $\frac{R1}{R1 + R2}$ x field blanking amplitude 2,0 V to 6,5 V. | |

For a video input voltage of 1 V peak-to-peak: R3 can be omitted; R4 = 1 kΩ; R5 must be short-circuited; R6 = 1 kΩ.

## APPLICATION INFORMATION

The function is described against the corresponding pin number.

### 1. + 12 V power supply

The circuit gives good operation in a supply voltage range between 8 and 13,2 V provided that the supply voltage for the controls is equal to the supply voltage for the TDA3561A. All signal and control levels have a linear dependency on the supply voltage. The current taken by the device at 12 V is typically 85 mA. It is linearly dependent on the supply voltage.

### 2. Control voltage for identification

This pin requires a detection capacitor of about 330 nF for correct operation. The voltages available under various signal conditions are given in the specification.

### 3. Chrominance input

The chroma signal must be a.c.-coupled to the input. Its amplitude must be between 55 mV and 1100 mV peak-to-peak (25 mV to 500 mV peak-to-peak burst signal). All figures for the chroma signals are based on a colour bar signal with 75% saturation, that is the burst-to-chroma ratio of the input signal is 1 : 2,25.

### 4. Reference voltage A.C.C. detector

This pin must be decoupled by a capacitor of about 330 nF. The voltage at this pin is 4,9 V.

### 5. Control voltage A.C.C.

The A.C.C. is obtained by synchronous detection of the burst signal followed by a peak detector. A good noise immunity is obtained in this way and an increase of the colour for weak input signals is prevented. The recommended capacitor value at this pin is 2,2 μF.

### 6. Saturation control

The saturation control range is in excess of 50 dB. The control voltage range is 2 to 4 V. Saturation control is a linear function of the control voltage.

When the colour killer is active, the saturation control voltage is reduced to a low level if the resistance of the external saturation control network is sufficiently high. Then the chroma amplifier supplies no signal to the demodulator. Colour switch-on can be delayed by proper choice of the time constant for the saturation control setting circuit.

When the saturation control pin is connected to the power supply the colour killer circuit is overruled so that the colour signal is visible on the screen. In this way it is possible to adjust the oscillator frequency without using a frequency counter (see also pins 25 and 26).

### 7. Contrast control

The contrast control range is 20 dB for a control voltage change from + 2 to + 4 V. Contrast control is a linear function of the control voltage. The output signal is suppressed when the control voltage is 1 V or less. If one or more output signals surpasses the level of 9 V the peak white limiter circuit becomes active and reduces the output signals via the contrast control by discharging C2 via an internal current sink.

### 8. Sandcastle and field blanking input

The output signals are blanked if the amplitude of the input pulse is between 2 and 6,5 V. The burst gate and clamping circuits are activated if the input pulse exceeds a level of 7,5 V.
The higher part of the sandcastle pulse should start just after the sync pulse to prevent clamping of video signal on the sync pulse. The width should be about 4 μs for proper A.C.C. operation.

### 9. Video-data switching

The insertion circuit is activated by means of this input by an input pulse between 1 V and 2 V. In that condition, the internal RGB signals are switched off and the inserted signals are supplied to the output amplifiers. If only normal operation is wanted this pin should be connected to the negative supply. The switching times are very short (< 20 ns) to avoid coloured edges of the inserted signals on the screen.

### 10. Luminance signal input

The input signal should have a peak-to-peak amplitude of 0,45 V (peak white to sync) to obtain a black-white output signal of 5 V at nominal contrast. It must be a.c.-coupled to the input by a capacitor of about 22 nF. The signal is clamped at the input to an internal reference voltage.
A 1 kΩ luminance delay line can be applied because the luminance input impedance is made very high. Consequently the charging and discharging currents of the coupling capacitor are very small and do not influence the signal level at the input noticeably. Additionally the coupling capacitor value may be small.

### 11. Brightness control

The black level of the RGB outputs can be set by the voltage on this pin (see Fig. 5). The black level can be set higher than 4 V however the available output signal amplitude is reduced (see pin 7). Brightness control also operates on the black level of the inserted signals.

### 12, 14, 16. RGB outputs

The output circuits for red, green and blue are identical. Output signals are 5,25 V (R, G and B) at nominal input signals and control settings. The black levels of the three outputs have the same value. The blanking level at the outputs is 2,1 V. The peak white level is limited to 9,3 V. When this level exceeded the output signal amplitude is reduced via the contrast control (see pin 7).

### 13, 15, 17. Inputs for external RGB signals

The external signals must be a.c.-coupled to the inputs via a coupling capacitor of about 100 nF. Source impedance should not exceed 150 Ω. The input signal required for a 5 V peak-to-peak output signal is 1 V peak -to-peak. At the RGB outputs the black level of the inserted signal is identical to that of normal RGB signals. When these inputs are not used the coupling capacitors have to be connected to the negative supply.

### 18, 19, 20. Black level clamp capacitors

The black level clamp capacitors for the three channels are connected to these pins. The value of each capacitor should be about 100 nF.

### 21, 22. Inputs (B-Y) and (R-Y) demodulators

The input signal is automatically fixed to the required level by means of the burst phase detector and A.C.C. generator which are connected to pin 21 and pin 22. As the burst (applied differentially to those pins) is kept constant by the A.C.C., the colour difference signals automatically have the correct value.

## APPLICATION INFORMATION (continued)

### 23, 24. Burst phase detector outputs

At these pins the output of the burst phase detector is filtered and controls the reference oscillator. An adequate catching range is obtained with the time constants given in the application circuit (see Fig. 6).

### 25, 26. Reference oscillator

The frequency of the oscillator is adjusted by the variable capacitor C1. For frequency adjustment interconnect pin 21 and pin 22. The frequency can be measured by connecting a suitable frequency counter to pin 25.

### 28. Output of the chroma amplifier

Both burst and chroma signals are available at the output. The burst-to-chroma ratio at the output is identical to that at the input for nominal control settings. The burst signal is not affected by the controls. The amplitude of the input signal to the demodulator is kept constant by the A.C.C. Therefore the output signal at pin 28 will depend on the signal loss in the delay line.

# PAL/NTSC DECODER

## GENERAL DESCRIPTION

The TDA3562A is a monolithic integrated decoder for the PAL and/or NTSC colour television standards. It combines all functions required for the identification and demodulation of PAL/NTSC signals. Furthermore it contains a luminance amplifier, an RGB-matrix and amplifier. These amplifiers supply output signals up to 4 V peak-to-peak (picture information) enabling direct drive of the discrete output stages. The circuit also contains separate inputs for data insertion, analogue as well as digital, which can be used for text display systems (e.g. Teletext/broadcast Antiope), channel number display, etc.

### Features

- A black-current stabilizer which controls the black-currents of the three electron-guns to a level low enough to omit the black-level adjustment
- Contrast control of inserted RGB signals
- No black-level disturbance when non-synchronized external RGB signals are available on the inputs
- NTSC capability with hue control

## QUICK REFERENCE DATA

| | | | | |
|---|---|---|---|---|
| Supply voltage (pin 1) | $V_P = V_{1\text{-}27}$ | typ. | 12 | V |
| Supply current (pin 1) | $I_P = I_1$ | typ. | 80 | mA |
| **Luminance amplifier** (pin 8) | | | | |
| Input voltage (peak-to-peak value) | $V_{8\text{-}27(p\text{-}p)}$ | typ. | 450 | mV |
| Contrast control range | | typ. | 20 | dB |
| **Chrominance amplifier** (pin 4) | | | | |
| Input voltage range (peak-to-peak value) | $V_{4\text{-}27(p\text{-}p)}$ | | 40 to 1100 | mV |
| Saturation control range | | min. | 50 | dB |
| **RGB matrix and amplifiers** | | | | |
| Output voltage at nominal luminance and contrast (peak-to-peak value) | $V_{13,15,17\text{-}27(p\text{-}p)}$ | typ. | 4 | V |
| **Data insertion** | | | | |
| Input signals (peak-to-peak value) | $V_{12,14,16\text{-}27(p\text{-}p)}$ | typ. | 1 | V |
| **Data blanking** (pin 9) | | | | |
| Input voltage for data insertion | $V_{9\text{-}27}$ | min. | 0,9 | V |
| **Sandcastle input** (pin 7) | | | | |
| Blanking input voltage | $V_{7\text{-}27}$ | typ. | 1,5 | V |
| Burst gating and clamping input voltage | $V_{7\text{-}27}$ | typ. | 7 | V |

## PACKAGE OUTLINE

28-lead DIL; plastic, with internal heat spreader (SOT-117).

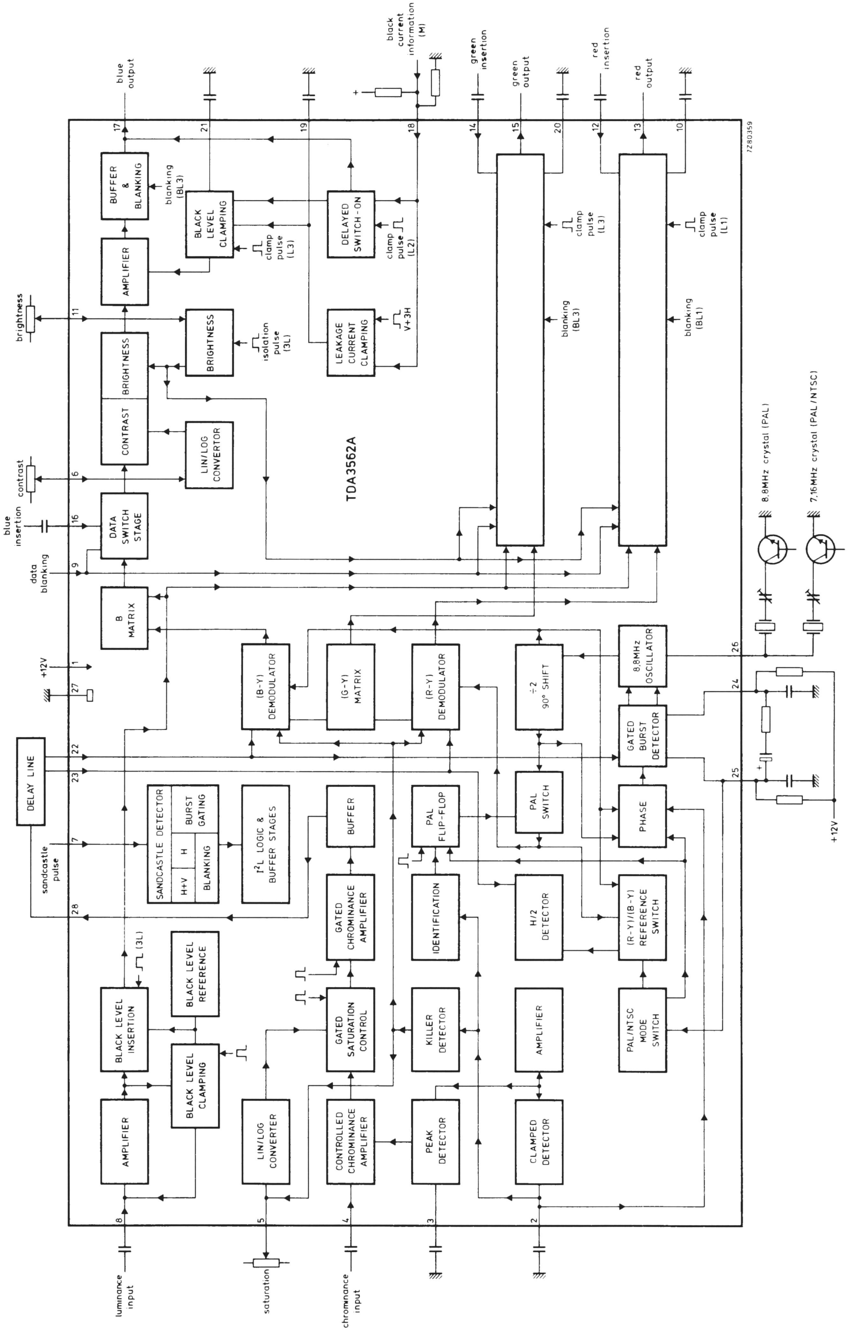

TDA3562A
7Z80359
luminance input
saturation
chrominance input
sandcastle pulse
DELAY LINE
+12V
data blanking
blue insertion
contrast
brightness
blue output
black current information (M)
green insertion
green output
red insertion
red output
AMPLIFIER
BLACK LEVEL CLAMPING
BLACK LEVEL INSERTION
BLACK LEVEL REFERENCE
(3L)
LIN/LOG CONVERTER
CONTROLLED CHROMINANCE AMPLIFIER
GATED SATURATION CONTROL
GATED CHROMINANCE AMPLIFIER
BUFFER
PEAK DETECTOR
KILLER DETECTOR
IDENTIFICATION
PAL FLIP-FLOP
CLAMPED DETECTOR
AMPLIFIER
H/2 DETECTOR
PAL SWITCH
÷2 90° SHIFT
PAL/NTSC MODE SWITCH
(R-Y)/(B-Y) REFERENCE SWITCH
PHASE
GATED BURST DETECTOR
8,8MHz OSCILLATOR
SANDCASTLE DETECTOR
H+V
H
BLANKING
BURST GATING
I²L LOGIC & BUFFER STAGES
(B-Y) DEMODULATOR
(G-Y) MATRIX
(R-Y) DEMODULATOR
B MATRIX
DATA SWITCH STAGE
CONTRAST
BRIGHTNESS
LIN/LOG CONVERTOR
BRIGHTNESS
isolation pulse (3L)
AMPLIFIER
BUFFER & BLANKING
blanking (BL3)
BLACK LEVEL CLAMPING
clamp pulse (L3)
DELAYED SWITCH-ON
clamp pulse (L2)
LEAKAGE CURRENT CLAMPING
V+3H
clamp pulse (L3)
blanking (BL3)
clamp pulse (L1)
blanking (BL1)
8,8MHz crystal (PAL)
7,16MHz crystal (PAL/NTSC)
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28

Fig. 1 Block diagram; for explanation of pulse mnemonics see Fig. 6.

## FUNCTIONAL DESCRIPTION

### Luminance amplifier

The luminance amplifier is voltage driven and requires an input signal of 450 mV peak-to-peak (positive video). The luminance delay line must be connected between the i.f. amplifier and the decoder. The input signal is a.c. coupled to the input (pin 8). After amplification, the black level at the output of the preamplifier is clamped to a fixed d.c. level by the black level clamping circuit.

During three line periods after vertical blanking, the luminance signal is blanked out and the black level reference voltage is inserted by a switching circuit. This black level reference voltage is controlled via pin 11 (brightness). At the same time the RGB signals are clamped. Noise and residual signals have no influence during clamping thus simple internal clamping circuitry is used.

### Chrominance amplifiers

The chrominance amplifier has an asymmetrical input. The input signal must be a.c. coupled (pin 4) and have a minimum amplitude of 40 mV peak-to-peak. The gain control stage has a control range in excess of 30 dB, the maximum input signal must not exceed 1,1 V peak-to-peak, otherwise clipping of the input signal will occur. From the gain control stage the chrominance signal is fed to the saturation control stage. Saturation is linear controlled via pin 5. The control voltage range is 2 to 4 V, the input impedance is high and the saturation control range is in excess of 50 dB. The burst signal is not affected by saturation control. The signal is then fed to a gated amplifier which has a 12 dB higher gain during the chrominance signal. As a result the signal at the output (pin 28) has a burst to chrominance ratio which is 6 dB lower than that of the input signal when the saturation control is set at –6 dB. The chrominance output signal is fed to the delay line and, after matrixing, is applied to the demodulator input pins (pins 22 and 23). These signals are fed to the burst phase detector.

### Oscillator and identification circuit

The burst phase detector is gated with the narrow part of the sandcastle pulse (pin 7). In the detector the (R-Y) and (B-Y) signals are added to provide the composite burst signal again. This composite signal is compared with the oscillator signal divided-by-2 (R-Y) reference signal. The control voltage is available at pins 24 and 25, and is also applied to the 8,8 MHz oscillator. The 4,4 MHz signal is obtained via the divide-by-2 circuit, which generates both the (B-Y) and (R-Y) reference signals and provides a 90° phase shift between them.

The flip-flop is driven by pulses obtained from the sandcastle detector. For the identification of the phase at PAL mode, the (R-Y) reference signal coming from the PAL switch, is compared to the vertical signal (R-Y) of the PAL delay line. This is carried out in the H/2 detector, which is gated during burst. When the phase is incorrect, the flip-flop gets a reset from the identification circuit. When the phase is correct, the output voltage of the H/2 detector is directly related to the burst amplitude so that this voltage can be used for the a.c.c. To avoid 'blooming-up' of the picture under weak input signal conditions the a.c.c. voltage is generated by peak detection of the H/2 detector output signal.

The killer and identification circuits get their information from a gated output signal of the H/2 detector. Killing is obtained via the saturation control stage and the demodulators to obtain good suppression. The time constant of the saturation control (pin 5) provides a delayed switch-on after killing.

Adjustment of the oscillator is achieved by variation of the burst phase detector load resistance between pins 24 and 25 (see Fig. 7). With this application the trimmer capacitor in series with the 8,8 MHz crystal (pin 26) can be replaced by a fixed value capacitor to compensate for unbalance of the phase detector.

## FUNCTIONAL DESCRIPTION (continued)

### Demodulator

The (R-Y) and (B-Y) demodulators are driven by the colour difference signals from the delay-line matrix circuit and the reference signals from the 8,8 MHz divider circuit. The (R-Y) reference signal is fed via the PAL-switch. The output signals are fed to the R and B matrix circuits and to the (G-Y) matrix to provide the (G-Y) signal which is applied to the G-matrix. The demodulation circuits are killed and blanked by by-passing the input signals.

### NTSC mode

The NTSC mode is switched on when the voltage at the burst phase detector outputs (pins 24 and 25) is adjusted below 9 V. To ensure reliable application the phase detector load resistors are external. When the TDA3562A is used only for PAL these two 33 kΩ resistors must be connected to + 12 V (see Fig. 7). For PAL/NTSC application the value of each resistor must be reduced to 10 kΩ and connected to the slider of a potentiometer (see Fig. 8). The switching transistor brings the voltage at pins 24 and 25 below 9 V which switches the circuit to the NTSC mode. The position of the PAL flip-flop ensures that the correct phase of the (R-Y) reference signal is supplied to the (R-Y) demodulator. The drive to the H/2 detector is now provided by the (B-Y) reference signal. In the PAL mode it is driven by the (R-Y) reference signal.

Hue control is realized by changing the phase of the reference drive to the burst phase detector. This is achieved by varying the voltage at pins 24 and 25 between 7,5 and 8,5 V, nominal position 8,0 V. The hue control characteristic is shown in Fig. 5.

### RGB matrix and amplifiers

The three matrix and amplifier circuits are identical and only one circuit will be described.

The luminance and the colour difference signals are added in the matrix circuit to obtain the colour signal, which is then fed to the contrast control stage. The contrast control voltage is supplied to pin 6 (high-input impedance). The control range is +5 dB to −15 dB nominal. The relationship between the control voltage and the gain is linear (see Fig. 2).

During the 3-line period after blanking a pulse is inserted at the output of the contrast control stage. The amplitude of this pulse is varied by a control voltage at pin 11. This applies a variable offset to the normal black level, thus providing brightness control. The brightness control range is 1 V to 3 V.

While this offset level is present, the 'black-current' input impedance (pin 18) is high and the internal clamp circuit is activated. The clamp circuit then compares the reference voltage at pin 19 with the voltage developed across the external resistor network $R_A$ and $R_B$ (pin 18) which is provided by picture tube beam current. The output of the comparator is stored in capacitors connected from pins 10, 20 and 21 to ground which controls the black level at the output. The reference voltage is composed by the resistor divider network and the leakage current of the picture tube into this bleeder. During vertical blanking, this voltage is stored in the capacitor connected to pin 19, which ensures that the leakage current of the CRT does not influence the black current measurement.

The RGB output signals can never exceed a level of 10 V. When the signal tends to exceed this level the output signal is clipped. The black level at the outputs (pins 13, 15 and 17) will be about 3 V. This level depends on the spread of the guns of the picture tube. If a beam current stabilizer is not used it is possible to stabilize the black levels at the outputs, which in this application must be connected to the black current measuring input (pin 18) via a resistor network.

### Data insertion

Each colour amplifier has a separate input for data insertion. A 1 V peak-to-peak input signal provides a 4 V peak-to-peak output signal. To avoid the 'black-level' of the inserted signal differing from the black level of the normal video signal, the data is clamped to the black level of the luminance signal. Therefore a.c. coupling is required for the data inputs. To avoid a disturbance of the blanking level due to the clamping circuit, the source impedance of the driver circuit must not exceed 150 Ω.

The data insertion circuit is activated by the data blanking input (pin 9). When the voltage at this pin exceeds a level of 0,9 V, the RGB matrix circuits are switched off and the data amplifiers are switched on. To avoid coloured edges, the data blanking switching time is short.

The amplitude of the data output signals is controlled by the contrast control at pin 6. The black level is equal to the video black level and can be varied between 2 and 4 V (nominal condition) by the brightness control voltage at pin 11.

Non-synchronized data signals do not disturb the black level of the internal signals.

### Blanking of RGB and data signals

Both the RGB and data signals can be blanked via the sandcastle input (pin 7). A slicing level of 1,5 V is used for this blanking function, so that the wide part of the sandcastle pulse is separated from the remainder of the pulse. During blanking a level of + 1 V is available at the output.

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | | |
|---|---|---|---|---|
| Supply voltage (pin 1) | $V_P = V_{1\text{-}27}$ | max. | 13,2 | V |
| Total power dissipation | $P_{tot}$ | max. | 1,7 | W |
| Storage temperature range | $T_{stg}$ | | −25 to + 150 | °C |
| Operating ambient temperature range | $T_{amb}$ | | −25 to + 70 | °C |

## THERMAL RESISTANCE

| | | | | |
|---|---|---|---|---|
| From junction to ambient (in free air) | $R_{th\ j\text{-}a}$ | = | 40 | K/W |

## CHARACTERISTICS

$V_P = V_{1-27} = 12$ V; $T_{amb} = 25$ V; unless otherwise specified

| parameter | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| **Supply** (pin 1) | | | | | |
| Supply voltage | $V_P = V_{1-27}$ | 10,8 | 12 | 13,2 | V |
| Supply current | $I_P = I_1$ | – | 80 | 110 | mA |
| Total power dissipation | $P_{tot}$ | – | 0,95 | 1,3 | W |
| **Luminance amplifier** (pin 8) | | | | | |
| Input voltage (note 1) (peak-to-peak value) | $V_{8-27(p-p)}$ | – | 0,45 | – | V |
| Input level before clipping | $V_{8-27}$ | – | – | 1 | V |
| Input current | $I_8$ | – | 0,1 | 1 | μA |
| Contrast control range (see Fig. 2) | | –15 | – | +5 | dB |
| Input current contrast control | $I_7$ | – | – | 15 | μA |
| **Chrominance amplifier** (pin 4) | | | | | |
| Input voltage (note 2) (peak-to-peak value) | $V_{4-27(p-p)}$ | 40 | 390 | 1100 | mV |
| Input impedance | $\|Z_{4-27}\|$ | – | 10 | – | kΩ |
| Input capacitance | $C_{4-27}$ | – | – | 6,5 | pF |
| A.C.C. control range | | 30 | – | – | dB |
| Change of the burst signal at the output over the whole control range | | – | – | 1 | dB |
| Gain at nominal contrast/saturation pin 4 to pin 28 (note 3) | | 34 | – | – | dB |
| Chrominance to burst ratio at nominal saturation (notes 2 and 3) at pin 28 | | – | 12 | – | dB |
| Maximum output voltage (peak-to-peak value); $R_L = 2$ kΩ | $V_{28-27(p-p)}$ | 4 | 5 | – | V |
| Distortion of chrominance amplifier at $V_{28-27(p-p)} = 2$ V (output) up to $V_{4-27(p-p)} = 1$ V (input) | d | – | – | 5 | % |
| Frequency response between 0 and 5 MHz | $\alpha_{28-4}$ | – | – | –2 | dB |
| Saturation control range (see Fig. 3) | | 50 | – | – | dB |
| Input current saturation control (pin 5) | $I_5$ | – | – | 20 | μA |
| Cross-coupling between luminance and chrominance amplifier (note 4) | | – | – | –46 | dB |
| Signal-to-noise ratio at nominal input signal (note 5) | S/N | 56 | – | – | dB |
| Phase shift between burst and chrominance at nominal contrast/saturation | $\Delta\varphi$ | – | – | ± 5 | deg |
| Output impedance of chrominance amplifier | $\|Z_{28-27}\|$ | – | 10 | – | Ω |
| Output current | $I_{28}$ | – | – | 15 | mA |

DEVELOPMENT SAMPLE DATA

| parameter | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| **Reference part** | | | | | |
| Phase-locked-loop<br>catching range (note 6) | Δf | 500 | 700 | – | Hz |
| phase shift for ± 400 Hz deviation of $f_{osc}$ (note 6) | Δφ | – | – | 5 | deg |
| Oscillator<br>temperature coefficient of oscillator frequency (note 6) | $TC_{osc}$ | – | –2 | – | Hz/K |
| frequency variation when supply voltage increases from 10 V to 13,2 V (note 6) | $\Delta f_{osc}$ | – | 40 | – | Hz |
| input resistance (pin 26) | $R_{26-27}$ | – | 400 | – | Ω |
| input capacitance (pin 26) | $C_{26-27}$ | – | – | 10 | pF |
| A.C.C. generation (pin 2)<br>control voltage at nominal input signal | $V_{2-27}$ | – | 4,5 | – | V |
| control voltage without chrominance input | $V_{2-27}$ | – | 2,0 | – | V |
| colour-off voltage | $V_{2-27}$ | – | 2,8 | – | V |
| colour-on voltage | $V_{2-27}$ | – | 3,0 | – | V |
| identification-on voltage | $V_{2-27}$ | – | 1,7 | – | V |
| change in burst amplitude with temperature | | – | 0,1 | 0,25 | %/K |
| voltage at pin 3 at nominal input signal | $V_{3-27}$ | – | 5,1 | – | V |
| **Demodulator part** | | | | | |
| Input burst signal amplitude (peak-to-peak value) between pins 23 and 27 (note 7) | $V_{23-27(p-p)}$ | – | 80 | – | mV |
| Input impedance between pins 22 or 23 and 27 | $\|Z_{22-27/23-27}\|$ | – | 1 | – | kΩ |
| Ratio of demodulated signals (note 8)<br>(B-Y)/(R-Y) | $\frac{V_{17-27}}{V_{13-27}}$ | – | 1,78 ± 10% | – | |
| (G-Y)/(R-Y); no (B-Y) signal | $\frac{V_{15-27}}{V_{13-27}}$ | – | –0,51 ± 10% | – | |
| (G-Y)/(B-Y); no (R-Y) signal | $\frac{V_{15-27}}{V_{17-27}}$ | – | –0,19 ± 25% | – | |
| Frequency response between 0 and 1 MHz | | – | – | –3 | dB |
| Cross-talk between colour difference signals | | 40 | – | – | dB |
| Phase difference between (R-Y) signal and (R-Y) reference signal | Δφ | – | – | 5 | deg |
| Phase difference between (R-Y) and (B-Y) reference signals | Δφ | 85 | 90 | 95 | deg |

CHARACTERISTICS (continued)

| parameter | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| **RGB matrix and amplifiers** | | | | | |
| Output voltage (peak-to-peak value) at nominal luminance/contrast (black-to-white) (note 3) | $V_{13,15,17\text{-}27(p\text{-}p)}$ | 3,5 | 4 | 4,5 | V |
| Output voltage at pin 13 (peak-to-peak value) at nominal contrast/saturation and no luminance signal to (R-Y) | $V_{13\text{-}27(p\text{-}p)}$ | – | 4,2 | – | V |
| Maximum peak-white level | $V_{13,15,17(m)}$ | 9,7 | 10 | 10,3 | V |
| Available output current (pins 13,15,17) | $I_{13,15,17}$ | 10 | – | – | mA |
| Difference between black level and measuring level at the output for a brightness control voltage at pin 11 of 2 V (note 9) | $\Delta V_{13,15,17\text{-}27}$ | – | 0 | – | V |
| Difference in black level between the three channels without black current stabilization (note 10) | | – | – | 100 | mV |
| Control range of black-current stabilization at $V_{b1} = 3$ V; $V_{11\text{-}27} = 2$ V | | – | – | ± 2 | V |
| Black level shift with vision contents | | – | – | 40 | mV |
| Brightness control voltage range | | | see Fig. 4 | | |
| Brightness control input current | $I_{11}$ | – | – | 5 | µA |
| Variation of black level with temperature | $\Delta V/\Delta T$ | – | 0 | – | mV/K |
| Variation of black level with contrast* | $\Delta V$ | – | – | 100 | mV |
| Relative spread between the R, G and B output signals | | – | – | 10 | % |
| Relative black-level variation between the three channels during variation of contrast, brightness and supply voltage (± 10%) | | – | 0 | 20 | mV |
| Differential black-level drift over a temperature range of 40 °C* | | – | 0 | 20 | mV |
| Blanking level at the RGB outputs | | – | 0,95 | 1,1 | V |
| Difference in blanking level of the three channels | | – | 0 | – | mV |
| Differential drift of the blanking levels over a temperature range of 40 °C | | – | 0 | – | mV |
| Tracking of output black level with supply voltage | $\frac{\Delta V_{bl}}{V_{bl}} \times \frac{V_P}{\Delta V_P}$ | – | 1 | – | |
| Tracking of contrast control between the three channels over a control range at 10 dB | | – | – | 0,5 | dB |

* With respect to the measuring pulses.

| parameter | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| Output signal during the clamp pulse (3L) after switch-on | | 7,5 | – | – | V |
| Signal-to-noise ratio of output signals (note 5) | S/N | 62 | – | – | dB |
| Residual 4,4 MHz signal at RGB outputs (peak-to-peak value) | | – | – | 50 | mV |
| Residual 8,8 MHz signal and higher harmonics at the RGB outputs (peak-to-peak value) | | – | – | 150 | mV |
| Output impedance of RGB outputs | $\lvert Z_{13,15,17\text{-}27} \rvert$ | – | 50 | – | Ω |
| Frequency response of total luminance and RGB amplifier circuits for f = 0 to 5 MHz | | – | –1 | –3 | dB |
| Current source of output stage | | 2 | 3 | – | mA |
| Difference of black level at the three outputs at nominal brightness* | | – | – | 10 | mV |
| Tracking of brightness control | | – | – | 2 | % |
| **Data insertion** (pins 12, 14 and 16) | | | | | |
| Input signals (peak-to-peak value) for an RGB output voltage of 4 V (peak-to-peak) at nominal contrast | $V_{12,14,16\text{-}27(p\text{-}p)}$ | 0,9 | 1 | 1,1 | V |
| Difference between the black levels of the RGB signals and the inserted signals at the output (note 11) | ΔV | – | – | 100 | mV |
| Output rise time | $t_r$ | – | – | 80 | ns |
| Differential delay time for the three channels | $t_d$ | – | 0 | 40 | ns |
| Input current | $I_{12,14,16}$ | – | – | 10 | μA |
| **Data blanking** (pin 9) | | | | | |
| Input voltage for no data insertion | $V_{9\text{-}27}$ | – | – | 0,4 | V |
| Input voltage for data insertion | $V_{9\text{-}27}$ | 0,9 | – | – | V |
| Maximum input voltage | $V_{9\text{-}27(m)}$ | – | – | 3 | V |
| Delay of data blanking | $t_d$ | – | – | 20 | ns |
| Input resistance | $R_{9\text{-}27}$ | 7 | 10 | 13 | kΩ |
| Suppression of the internal RGB signals when $V_{9\text{-}27} > 0{,}9$ V | | 46 | – | – | dB |

DEVELOPMENT SAMPLE DATA

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* With respect to the measuring pulses.

**CHARACTERISTICS** (continued)

| parameter | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| **Sandcastle input** (pin 7) | | | | | |
| Level at which the RGB blanking is activated | $V_{7\text{-}27}$ | 1 | 1,5 | 2 | V |
| Level at which the horizontal pulses are separated | $V_{7\text{-}27}$ | 3 | 3,5 | 4 | V |
| Level at which burst gating and clamping pulse are separated | $V_{7\text{-}27}$ | 6,5 | 7,0 | 7,5 | V |
| Delay between black level clamping and burst gating pulse | $t_d$ | – | 0,6 | – | μs |
| Input current | | | | | |
| at $V_{7\text{-}27}$ = 0 to 1 V | $-I_7$ | – | – | 1 | mA |
| at $V_{7\text{-}27}$ = 1 to 8,5 V | $I_7$ | – | 50 | – | μA |
| at $V_{7\text{-}27}$ = 8,5 to 12 V | $I_7$ | – | – | 2 | mA |
| **Black current stabilization** (pin 18) | | | | | |
| D.C. bias voltage | $V_{18\text{-}27}$ | 3,5 | 5 | 7,0 | V |
| Difference between input voltage for 'black' current and leakage current | $\Delta V$ | – | 0,5 | – | V |
| Input current during 'black' current | $I_{18}$ | – | – | 1 | μA |
| Input current during scan | $I_{18}$ | – | – | 10 | mA |
| Internal limiting at pin 10 | $V_{10\text{-}27}$ | – | 9 | – | V |
| Switching threshold for 'black' current control ON | $V_{1\text{-}27}$ | – | 8 | – | V |
| Input resistance during scan | $R_{1\text{-}27}$ | – | 1,5 | – | kΩ |
| D.C. input current during scan at pins 10, 20 and 21 | $I_{10,20,21}$ | – | – | 50 | nA |
| Maximum charge/discharge current during measuring time at pins 10,19,20 and 21 | $I_{c/d}$ | – | 10 | – | mA |
| **NTSC** | | | | | |
| Level at which the PAL/NTSC switch is activated (pins 24 and 25) | $V_{24\text{-}25}$ | – | 9 | – | V |
| Average output current (note 12) | $I_{24+25}$ | 75 | 90 | 105 | μA |
| Hue control | | | see Fig. 5 | | |

**Notes to the characteristics**

1. Signal with the negative-going sync; amplitude includes sync amplitude.
2. Indicated is a signal for a colour bar with 75% saturation; chrominance to burst ratio is 2,2 : 1.
3. Nominal contrast is specified as the maximum contrast −5 dB and nominal saturation as the maximum saturation −6 dB.
4. Cross coupling is measured under the following condition: input signal nominal, contrast and saturation such that nominal output signals are obtained. The signals at the output at which no signal should be available must be compared with the nominal output signal at that output.
5. The signal-to-noise ratio is defined as peak-to-peak signal with respect to r.m.s. noise.
6. All frequency variations are referred to 4,4 MHz carrier frequency.
7. These signal amplitudes are determined by the a.c.c. circuit of the reference part.
8. The demodulators are driven by a chrominance signal of equal amplitude for the (R-Y) and the (B-Y) components. The phase of the (R-Y) chrominance signal equals the phase of the (R-Y) reference signal. This also applies to the (B-Y) signals.
9. This value depends on the gain setting of the RGB output amplifiers and the drift of the picture tube guns. Higher black level values are possible (up to 5 V) but in that application the amplitude of the output signal is reduced.
10. The variation of the black-level during brightness control in the three different channels is directly dependent on the gain of each channel. Discolouration during adjustments of contrast and brightness does not occur because amplitude and the black-level change with brightness control are directly related.
11. This difference occurs when the source impedance of the data signals is 150 Ω and the black level clamp pulse width is 4 μs (sandcastle pulse). For a lower impedance the difference will be lower.
12. The voltage at pins 24 and 25 can be changed by connecting the load resistors (10 kΩ in this application) to the slider bar of the hue control potentiometer (see Fig. 8). When the transistor is switched on, the voltage at pins 24 and 25 is reduced below 9 V, and the circuit is switched to NTSC mode.

DEVELOPMENT SAMPLE DATA

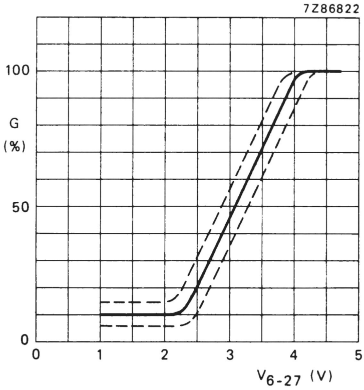


Fig. 2 Contrast control voltage range.

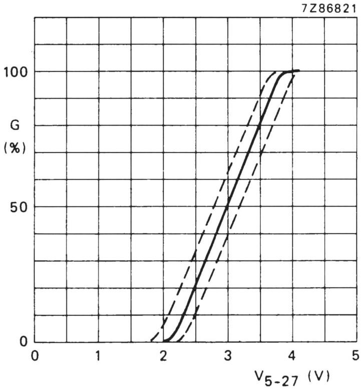


Fig. 3 Saturation control voltage range.

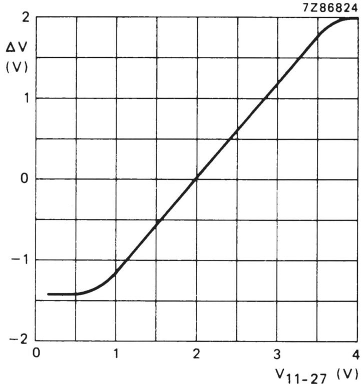


Fig. 4 Difference between black level and measuring level at the RGB outputs (ΔV) as a function of the brightness control input voltage ($V_{11-27}$).

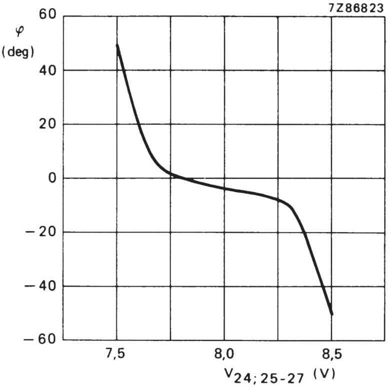


Fig. 5 Hue control voltage range.

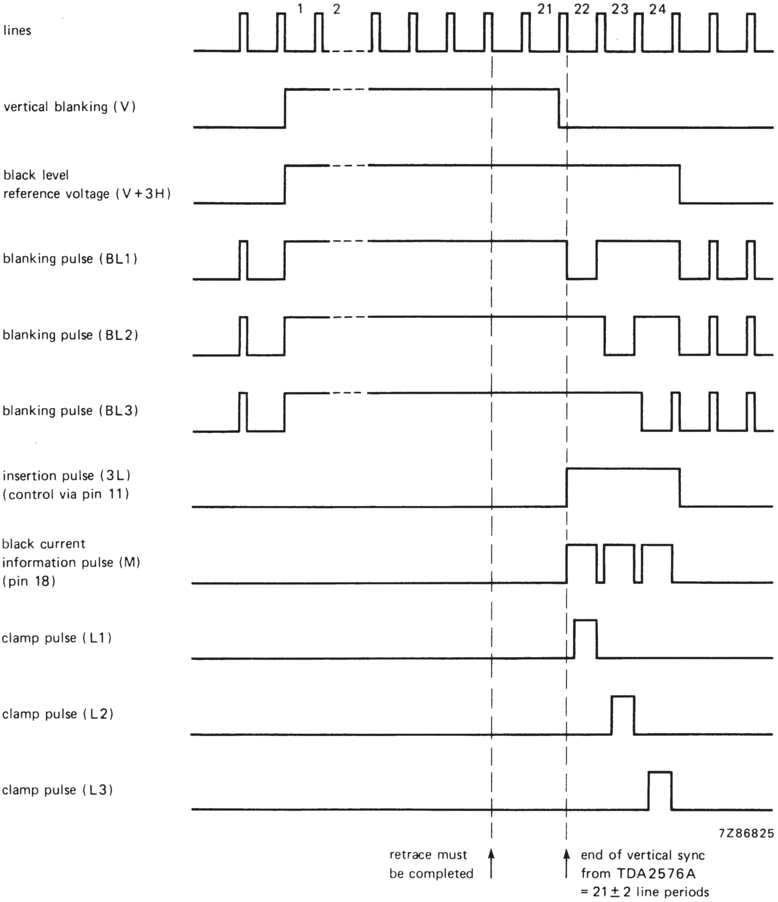

lines
1
2
21
22
23
24
vertical blanking (V)
black level
reference voltage (V + 3H)
blanking pulse (BL1)
blanking pulse (BL2)
blanking pulse (BL3)
insertion pulse (3L)
(control via pin 11)
black current
information pulse (M)
(pin 18)
clamp pulse (L1)
clamp pulse (L2)
clamp pulse (L3)
7Z86825
retrace must
be completed
end of vertical sync
from TDA2576A
= 21 ± 2 line periods

Fig. 6 Timing diagram for black-current stabilizing.

## APPLICATION INFORMATION

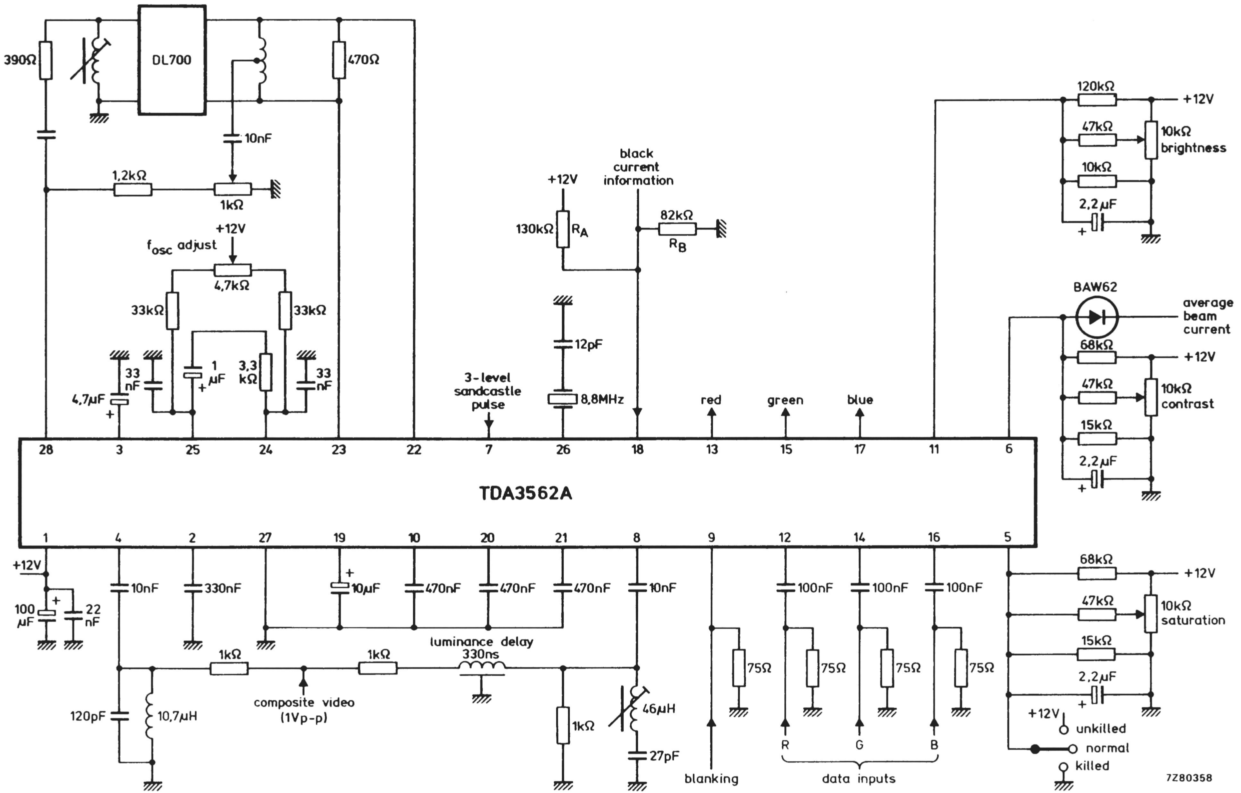

390Ω
DL700
470Ω
10nF
1,2kΩ
1kΩ
+12V
f_osc adjust
4,7kΩ
33kΩ
33kΩ
33 nF
4,7µF
1 µF
3,3 kΩ
33 nF
3-level sandcastle pulse
12pF
8,8MHz
+12V
130kΩ
R_A
black current information
82kΩ
R_B
red
green
blue
120kΩ
+12V
47kΩ
10kΩ brightness
10kΩ
2,2µF
BAW62
average beam current
68kΩ
+12V
47kΩ
10kΩ contrast
15kΩ
2,2µF
TDA3562A
28
3
25
24
23
22
7
26
18
13
15
17
11
6
1
4
2
27
19
10
20
21
8
9
12
14
16
5
+12V
100 µF
22 nF
10nF
330nF
10µF
470nF
470nF
470nF
10nF
100nF
100nF
100nF
68kΩ
+12V
47kΩ
10kΩ saturation
15kΩ
2,2µF
1kΩ
1kΩ
luminance delay 330ns
120pF
10,7µH
composite video (1Vp-p)
1kΩ
46µH
27pF
75Ω
75Ω
75Ω
75Ω
blanking
R
G
B
data inputs
+12V
unkilled
normal
killed
7Z80358

Fig. 7 Application diagram showing the TDA3562A for a PAL decoder.

DEVELOPMENT SAMPLE DATA

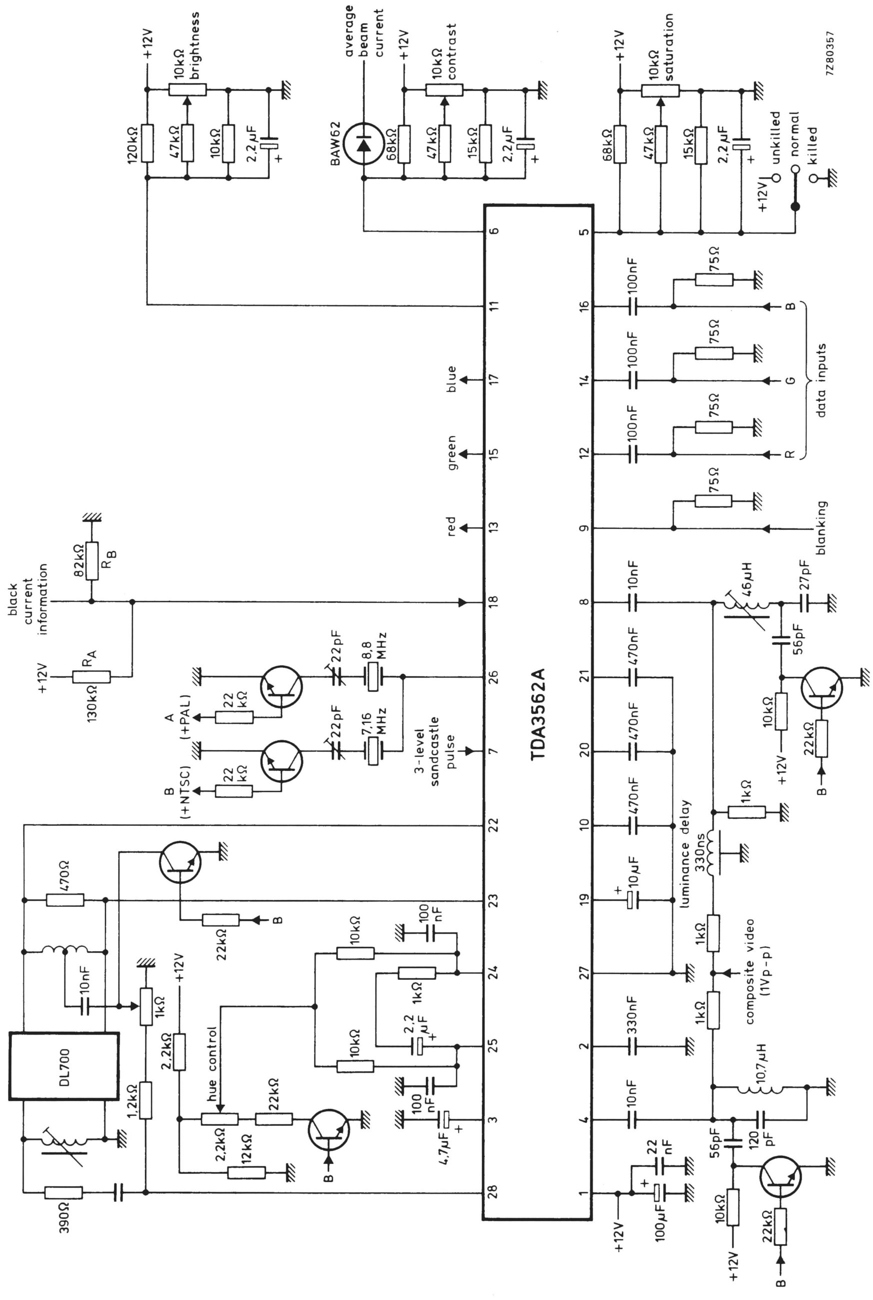

+12V
120kΩ
10kΩ brightness
47kΩ
10kΩ
2,2μF
average beam current
BAW62
+12V
68kΩ
10kΩ contrast
47kΩ
15kΩ
2,2μF
+12V
68kΩ
10kΩ saturation
47kΩ
15kΩ
2,2μF
+12V
unkilled
normal
killed
7Z80357
black current information
82kΩ
$R_B$
+12V
$R_A$
130kΩ
A (+PAL)
22 kΩ
22pF
8,8 MHz
B (+NTSC)
22 kΩ
22pF
7,16 MHz
3-level sandcastle pulse
red
green
blue
TDA3562A
6
11
17
15
13
18
26
7
22
23
24
25
3
28
5
16
14
12
9
8
21
20
10
19
27
2
4
1
100nF
75Ω
B
G
R
data inputs
blanking
10nF
46μH
27pF
56pF
470nF
10kΩ
+12V
22kΩ
B
1kΩ
luminance delay 330ns
10μF
1kΩ
composite video (1Vp-p)
1kΩ
330nF
10,7μH
10nF
56pF
120 pF
22 nF
100μF
+12V
10kΩ
+12V
22kΩ
B
470Ω
22kΩ
B
10nF
1kΩ
+12V
2,2kΩ
1,2kΩ
DL700
hue control
2,2kΩ
22kΩ
12kΩ
B
10kΩ
100 nF
1kΩ
2,2 μF
10kΩ
100 nF
4,7μF
390Ω

Fig. 8 Application diagram showing the TDA3562A for a PAL/NTSC decoder.

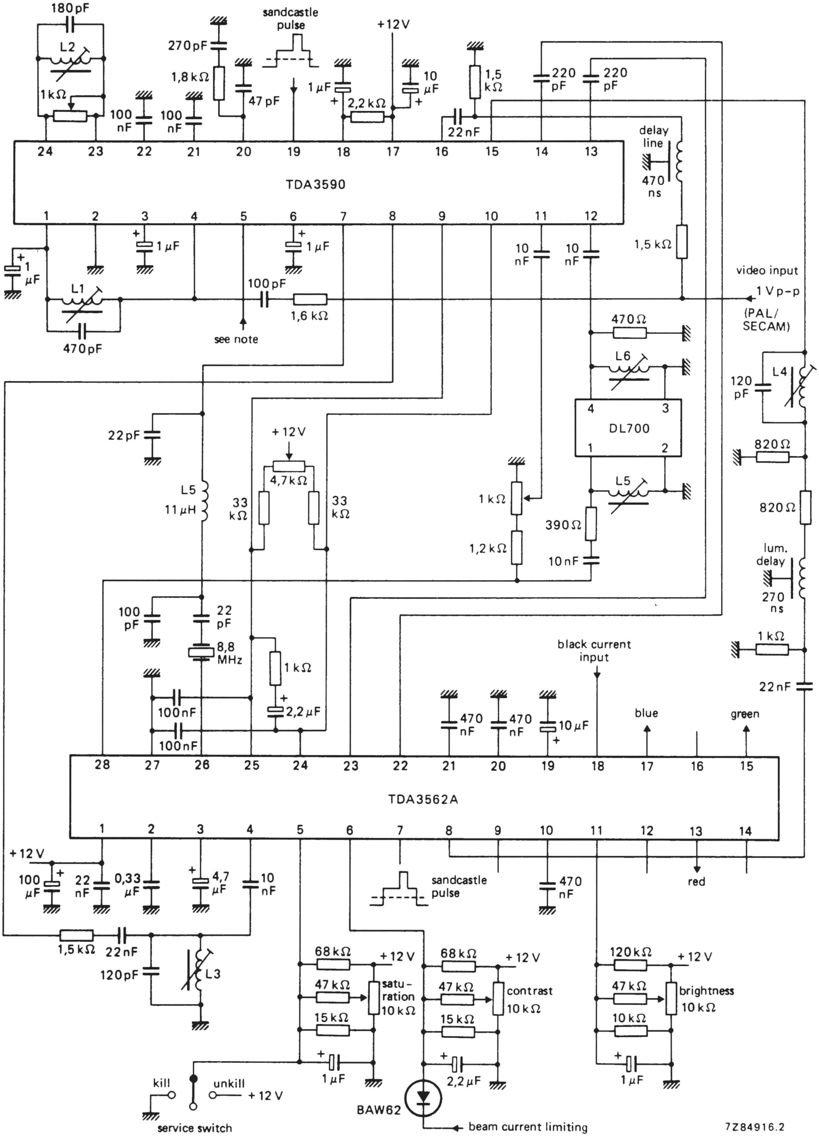

180 pF
L2
1 kΩ
100 nF
100 nF
270 pF
1,8 kΩ
47 pF
sandcastle pulse
1 μF
2,2 kΩ
+12 V
10 μF
1,5 kΩ
22 nF
220 pF
220 pF
delay line
470 ns
TDA3590
24
23
22
21
20
19
18
17
16
15
14
13
1
2
3
4
5
6
7
8
9
10
11
12
1 μF
1 μF
1 μF
L1
470 pF
100 pF
1,6 kΩ
see note
10 nF
10 nF
1,5 kΩ
video input
1 V p-p
(PAL/ SECAM)
470 Ω
L6
DL700
4
3
1
2
L5
120 pF
L4
820 Ω
820 Ω
lum. delay
270 ns
1 kΩ
22 nF
22 pF
L5
11 μH
+12 V
4,7 kΩ
33 kΩ
33 kΩ
1 kΩ
1,2 kΩ
390 Ω
10 nF
100 pF
22 pF
8,8 MHz
1 kΩ
2,2 μF
100 nF
100 nF
black current input
470 nF
470 nF
10 μF
blue
green
28
27
26
25
24
23
22
21
20
19
18
17
16
15
TDA3562A
1
2
3
4
5
6
7
8
9
10
11
12
13
14
+12 V
100 μF
22 nF
0,33 μF
4,7 μF
10 nF
sandcastle pulse
470 nF
red
1,5 kΩ
22 nF
120 pF
L3
68 kΩ
+12 V
47 kΩ
saturation 10 kΩ
15 kΩ
1 μF
68 kΩ
+12 V
47 kΩ
contrast 10 kΩ
15 kΩ
2,2 μF
120 kΩ
+12 V
47 kΩ
brightness 10 kΩ
10 kΩ
1 μF
kill
unkill
+12 V
service switch
BAW62
beam current limiting
7Z84916.2

Fig. 9 PAL/SECAM application circuit diagram using the TDA3590 and TDA3562A.

Note to pin 5 TDA3590:

$V_{5\text{-}2} < 1$ V; horizontal identification and black level clamping.
$V_{5\text{-}2} > 11$ V; vertical identification and artificial black level.
$V_{5\text{-}2} =$ 5 to 7 V; horizontal identification and artificial black level.

# NTSC DECODER

## GENERAL DESCRIPTION

The TDA3563 is a monolithic integrated colour decoder for the NTSC standard. It combines all functions required for the identification and demodulation of NTSC signals. Furthermore it contains a luminance amplifier, an RGB-matrix and amplifier. These amplifiers supply signals up to 5,3 V peak-to-peak (picture information) enabling direct drive of the output stages. The circuit also contains inputs for data insertion, analogue as well as digital, which can be used for Teletext information, channel number display, etc.

## QUICK REFERENCE DATA

| | | | | |
|---|---|---|---|---|
| Supply voltage (pin 1) | $V_P = V_{1\text{-}27}$ | typ. | 12 | V |
| Supply current (pin 1) | $I_P = I_1$ | typ. | 85 | mA |
| Luminance input signal (peak-to-peak value) | $V_{10\text{-}27(p\text{-}p)}$ | typ. | 0,45 | V |
| Chrominance input signal (peak-to-peak value) | $V_{3\text{-}27(p\text{-}p)}$ | | 55 to 1100 | mV |
| Data input signals (peak-to-peak value) | $V_{13;15;17\text{-}27(p\text{-}p)}$ | typ. | 1 | V |
| RGB output signals at nominal contrast and saturation (peak-to-peak value) | $V_{12;14;16\text{-}27(p\text{-}p)}$ | typ. | 5,3 | V |
| Contrast control range | | typ. | 20 | dB |
| Saturation control range | | min. | 50 | dB |
| Input voltage for fast video-data signal switching | $V_{9\text{-}27}$ | min. | 0,9 | V |
| Blanking input voltage | $V_{8\text{-}27}$ | typ. | 1,5 | V |
| Burst gating and black-level gating input voltage | $V_{8\text{-}27}$ | typ. | 7 | V |

## PACKAGE OUTLINE

28-lead DIL; plastic, with internal heat spreader (SOT-117).

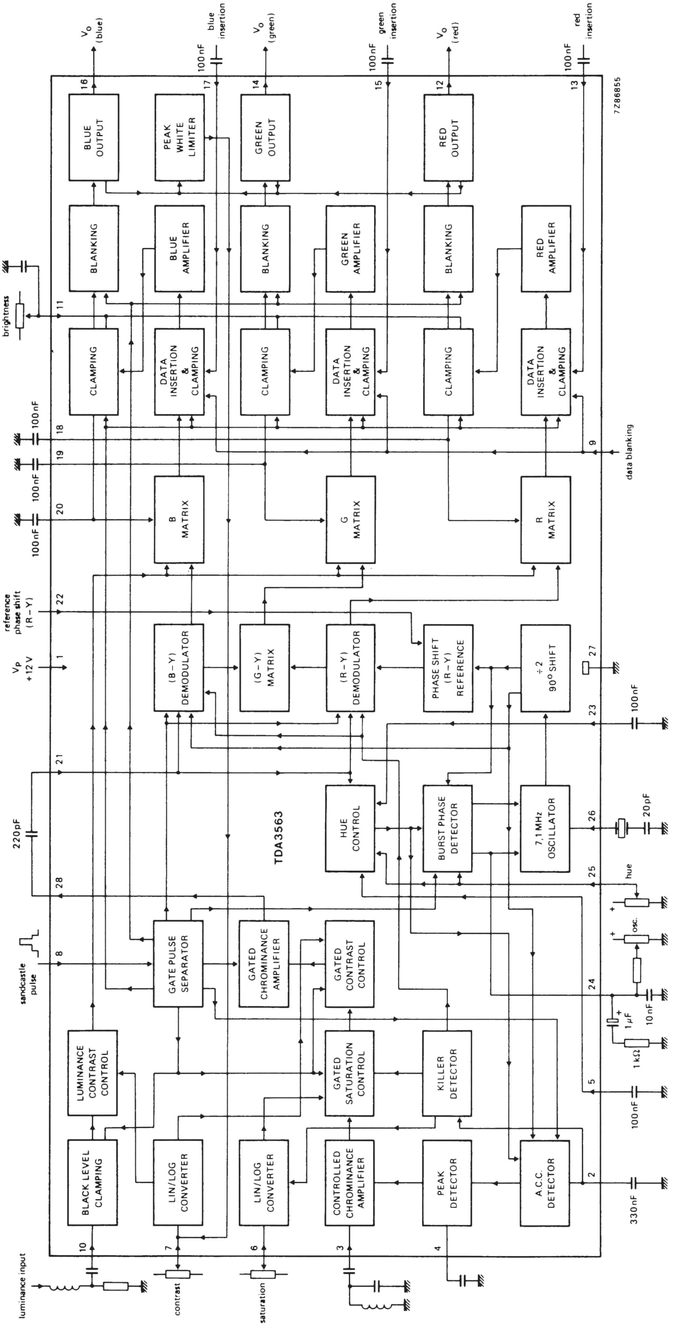

TDA3563
7Z86855
BLUE OUTPUT
PEAK WHITE LIMITER
GREEN OUTPUT
RED OUTPUT
BLANKING
BLUE AMPLIFIER
BLANKING
GREEN AMPLIFIER
BLANKING
RED AMPLIFIER
CLAMPING
DATA INSERTION & CLAMPING
CLAMPING
DATA INSERTION & CLAMPING
CLAMPING
DATA INSERTION & CLAMPING
B MATRIX
G MATRIX
R MATRIX
(B – Y) DEMODULATOR
(G – Y) MATRIX
(R – Y) DEMODULATOR
PHASE SHIFT (R – Y) REFERENCE
÷ 2 90° SHIFT
HUE CONTROL
BURST PHASE DETECTOR
7,1 MHz OSCILLATOR
GATE PULSE SEPARATOR
GATED CHROMINANCE AMPLIFIER
GATED CONTRAST CONTROL
LUMINANCE CONTRAST CONTROL
GATED SATURATION CONTROL
KILLER DETECTOR
BLACK LEVEL CLAMPING
LIN/LOG CONVERTER
LIN/LOG CONVERTER
CONTROLLED CHROMINANCE AMPLIFIER
PEAK DETECTOR
A.C.C. DETECTOR
$V_o$ (blue)
blue insertion
$V_o$ (green)
green insertion
$V_o$ (red)
red insertion
100 nF
16
17
14
15
12
13
brightness
11
18
19
20
reference phase shift (R – Y)
22
$V_P$ +12 V
1
21
220 pF
28
sandcastle pulse
8
10
7
6
3
4
luminance input
contrast
saturation
data blanking
9
27
23
26
20 pF
25
hue
osc.
24
10 nF
1 µF
1 kΩ
5
2
330 nF

Fig. 1 Block diagram.

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | |
|---|---|---|---|
| Supply voltage (pin 1) | $V_P = V_{1\text{-}27}$ | max. | 13,2 V |
| Total power dissipation | $P_{tot}$ | max. | 1,7 W |
| Storage temperature range | $T_{stg}$ | | −25 to + 150 °C |
| Operating ambient temperature range | $T_{amb}$ | | −25 to + 65 °C |

## THERMAL RESISTANCE

| | | | |
|---|---|---|---|
| From junction to ambient (in free air) | $R_{th\ j\text{-}a}$ | = | 50 K/W |

## CHARACTERISTICS

$V_P = V_{1\text{-}27} = 12$ V; $T_{amb} = 25\ ^oC$; unless otherwise specified

| parameter | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| **Supply** (pin 1) | | | | | |
| Supply voltage | $V_P = V_{1\text{-}27}$ | 10 | 12 | 13,2 | V |
| Supply current | $I_P = I_1$ | – | 85 | 115 | mA |
| Total power dissipation | $P_{tot}$ | – | 1 | 1,4 | W |
| **Luminance amplifier** | | | | | |
| Input voltage (note 1) (peak-to-peak value) | $V_{10\text{-}27(p\text{-}p)}$ | – | 0,45 | – | V |
| Contrast control range (see Fig. 2) | | −17 | – | +3 | dB |
| Control voltage for an attenuation of 40 dB | | – | 1,2 | – | V |
| Contrast control input current | $I_7$ | – | – | 15 | μA |
| **Chrominance amplifier** | | | | | |
| Input voltage (note 2) (peak-to-peak value) | $V_{3\text{-}27(p\text{-}p)}$ | 55 | 550 | 1100 | mV |
| A.C.C. control range | | 30 | – | – | dB |
| Change of the burst signal at the output over the whole control range | | – | – | 1 | dB |
| Output voltage (note 3) (peak-to-peak value) at a burst signal of 0,3 V peak to peak | $V_{28\text{-}27}$ | – | 0,15 | – | V |
| Maximum output voltage range (peak-to-peak value); $R_L = 2\ k\Omega$ | $V_{28\text{-}27}$ | – | 4 | – | V |
| Frequency response between 0 and 5 MHz | $\alpha_{28\text{-}3}$ | – | – | −2 | dB |
| Saturation control range (see Fig. 3) | | 50 | – | – | dB |
| Saturation control input current | $I_6$ | – | – | 20 | μA |
| Output impedance of chrominance amplifier | $\lvert Z_{28\text{-}27}\rvert$ | – | 25 | – | Ω |
| Output current | $I_{28}$ | – | – | 10 | mA |
| **Reference part** | | | | | |
| *Phase-locked loop* | | | | | |
| Catching range (note 4) | $\Delta f$ | 500 | 700 | – | Hz |
| Phase shift (notes 4 and 5) | $\Delta\varphi$ | – | – | 5 | deg |
| *Oscillator* | | | | | |
| Temperature coefficient of oscillator frequency (note 4) | $TC_{osc}$ | – | −1,5 | – | Hz/K |
| Frequency variation when supply voltage increases from 10 V to 13,2 V (note 4) | $\Delta f_{osc}$ | – | 40 | – | Hz |

| parameter | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| **Reference part** (continued) | | | | | |
| *Oscillator* (continued) | | | | | |
| Input resistance (pin 26) | $R_{26\text{-}27}$ | – | 400 | – | Ω |
| Input capacitance (pin 26) | $C_{26\text{-}27}$ | – | – | 10 | pF |
| *A.C.C. generation* (pin 2) | | | | | |
| Control voltage at nominal input signal | $V_{2\text{-}27}$ | – | 5,0 | – | V |
| Control voltage without chrominance input | $V_{2\text{-}27}$ | – | 2,7 | – | V |
| Colour-off voltage | $V_{2\text{-}27}$ | – | 3,0 | – | V |
| Colour-on voltage | $V_{2\text{-}27}$ | – | 3,3 | – | V |
| *Hue control* | | | | | |
| Control range | | ±50 | – | – | deg |
| **Demodulator part** | | | | | |
| Input burst signal amplitude (peak-to-peak value) | $V_{21\text{-}27(p\text{-}p)}$ | – | 300 | – | mV |
| Ratio for demodulated signals for equal input signal amplitudes | | | | | |
| (B-Y)/(R-Y) | $\frac{V_{16\text{-}27}}{V_{12\text{-}27}}$ | – | 1,06 ± 10% | – | |
| (G-Y)/(R-Y); no (B-Y) signal | $\frac{V_{14\text{-}27}}{V_{12\text{-}27}}$ | – | –0,27 ± 20% | – | |
| (G-Y)/(B-Y); no (R-Y) signal | $\frac{V_{14\text{-}27}}{V_{16\text{-}27}}$ | – | –0,2 ± 20% | – | |
| Frequency response between 0 and 1 MHz | | – | – | –3 | dB |
| **RGB matrix and amplifiers** | | | | | |
| Output voltage (note 3) (peak-to-peak value) at nominal luminance/contrast (black-to-white) | $V_{12;14;16\text{-}27}$ | 4,5 | 5,3 | 6,3 | V |
| Maximum peak-white level (note 6) | $V_{12;14;16\text{-}27}$ | 9,0 | 9,3 | 9,6 | V |
| Maximum output current | $I_{12;14;16}$ | – | – | 10 | mA |
| Output black level voltage for brightness control of 2 V | | – | 2,7 | – | V |
| Brightness control voltage range | | | see Fig. 4 | | |
| Brightness control input current | $I_{11}$ | – | – | 50 | μA |
| Relative spread between R, G and B output signals | | – | – | 10 | % |
| Blanking level at RGB outputs | | 1,9 | 2,1 | 2,3 | V |
| Tracking of output black level with supply voltage | $\frac{\Delta V_{bl}}{V_{bl}} \times \frac{V_P}{\Delta V_P}$ | – | 1,1 | – | |

**CHARACTERISTICS** (continued)

| parameter | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| **RGB matrix and amplifiers** (continued) | | | | | |
| Output impedance of RGB outputs | $\|Z_{12;14;16\text{-}27}\|$ | – | 50 | – | Ω |
| Frequency response of total luminance and RGB amplifier circuits for f = 0 to 5 MHz | | – | – | –3 | dB |
| **Data insertion** | | | | | |
| Input signals (peak-to-peak value) for an RGB output voltage of 5 V (peak-to-peak) | $V_{13;15;17\text{-}27(p\text{-}p)}$ | 0,9 | 1 | 1,1 | V |
| **Data blanking** (pin 9) | | | | | |
| Input voltage for no data insertion | $V_{9\text{-}27}$ | – | – | 0,3 | V |
| Input voltage for data insertion | $V_{9\text{-}27}$ | 0,9 | – | – | V |
| Maximum input voltage | $V_{9\text{-}27(m)}$ | – | – | 2 | V |
| Delay of data blanking | $t_d$ | – | – | 20 | ns |
| Input current | $I_9$ | – | – | 35 | μA |
| **Sandcastle input** (pin 8) | | | | | |
| Level at which RGB blanking is activated | $V_{8\text{-}27}$ | 1 | 1,5 | 2 | V |
| Level at which burst gating and clamping pulse are separated | $V_{8\text{-}27}$ | 6,5 | 7,0 | 7,5 | V |
| Delay between black level clamping and burst gating pulse | $t_d$ | – | 0,4 | – | μs |
| Input current | | | | | |
| at $V_{8\text{-}27}$ = 0 to 1 V | $-I_8$ | – | – | 1 | mA |
| at $V_{8\text{-}27}$ = 1 to 8,5 V | $I_8$ | – | 20 | – | μA |
| at $V_{8\text{-}27}$ = 8,5 to 12 V | $I_8$ | – | – | 2 | mA |

**Notes to the characteristics**

1. Signal with negative-going sync; amplitude includes sync amplitude.
2. Indicated is a signal for a colour bar with 75% saturation; chrominance to burst ratio is 2,2 : 1.
3. At nominal contrast and saturation. Nominal contrast is specified as the maximum contrast –3 dB and nominal saturation as the maximum saturation –6 dB.
4. All frequency variations are referred to 3,58 MHz carrier frequency.
5. For ± 400 Hz deviation of the oscillator frequency.
6. If the typical voltage for this white level is exceeded, the output voltage is reduced by discharging the capacitor at pin 7 (contrast control); discharge current is 1,5 mA.

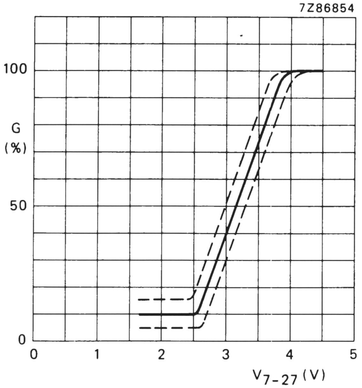


Fig. 2 Contrast control voltage range.

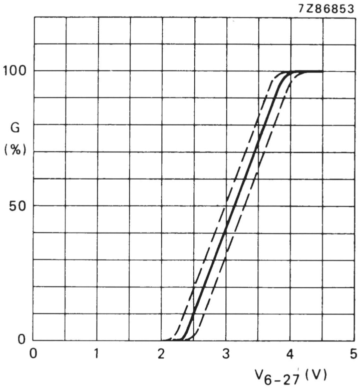


Fig. 3 Saturation control voltage range.

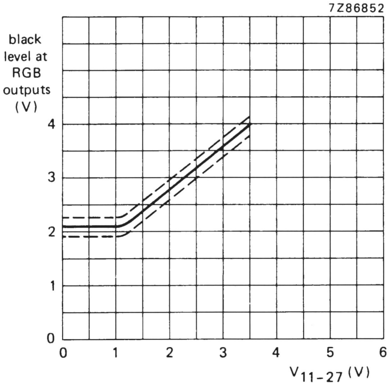


Fig. 4 Brightness control voltage range.

## APPLICATION INFORMATION

The function is described against the corresponding pin number.

### 1. + 12 V power supply

The circuit gives good operation in a supply voltage range between 8 and 13,2 V provided that the supply voltage for the controls is equal to the supply voltage of the TDA3563. All signal and control levels have a linear dependency on the supply voltage. The current consumed by the IC at + 12 V is typically 85 mA. It is linearly dependent on the supply voltage.

### 2. Control voltage for identification

The output pulses of the a.c.c. detector are detected with a sample-and-hold circuit to obtain information for the colour killer. The output is available at pin 2.

### 3. Chrominance input

The chrominance signal must be a.c.-coupled to the input. Its amplitude must be between 55 and 1100 mV peak-to-peak (25 to 500 mV peak-to-peak burst signal). All figures for the chrominance signals are based on a colour bar signal with 75% saturation, that is if the burst-to-chrominance ratio of the input is 1 : 2,2.

### 4. Control voltage a.c.c. detector

The shifted burst signal is synchronously demodulated in a separate a.c.c. detector to generate the a.c.c. voltage. The output pulses of this detector are peak detected to control the gain of the chrominance amplifier, thus preventing blooming-up of the colour during weak signal reception.

### 5. Decoupling of the 90° phase shift circuit

A control circuit is required in the 90° phase shift circuit to make the chrominance voltage independent of the hue setting. The control circuit is decoupled by a capacitor at this pin.

### 6. Saturation control

The saturation control range is in excess of 50 dB. The control voltage range is 2 to 4 V. Saturation control is a linear function of the control voltage.

When the colour killer is active, the saturation control voltage is reduced to a low level if the resistance of the external control network is sufficiently high. Then the chrominance amplifier supplies no signal to the demodulator. Colour switch-on can be delayed by proper choice of the time constant for the saturation control setting circuit.

When the saturation control pin is connected to the power supply the colour killer circuit is overruled so that the colour signal is visible on the screen. In this way it is possible to adjust the oscillator frequency without using a frequency counter (see also pins 24 and 26).

### 7. Contrast control

The contrast control range is 20 dB for a control voltage change from +2 V to +4 V. Contrast control is a linear function of the control voltage. The output signal is suppressed when the control voltage is 1 V or less. If one or more output signals surpasses the level of 9 V the peak-white limiter circuit becomes active and reduces the output signals via the contrast control by discharging a 10 μF capacitor via an internal current sink.

### 8. Sandcastle and vertical blanking input

The output signals are blanked if the amplitude of the pulse is between 2 V and 6,5 V. The burst gate and clamping circuits are activated if the input pulse exceeds a level of 7,5 V. The higher part of the sandcastle pulse should start just after the sync pulse to prevent clamping of the video signal on the sync pulse. The duration should be about 4 μs for proper a.c.c. operation.

### 9. Video-data switching

The insertion circuit is activated by means of this input by an input pulse between 1 and 2 V. In that condition, the internal RGB signals are switched off and the inserted signals are supplied to the output amplifiers. If only normal operation is wanted this pin should be connected to ground (pin 27).

The switching times are very short (< 20 ns) to avoid coloured edges of the inserted signals on the screen.

### 10. Luminance signal input

The input signal should have a peak-to-peak amplitude of 0,45 V (peak-white to sync) to obtain a black-white output signal of 5,3 V at nominal contrast. It must be a.c.-coupled to the input by a capacitor of about 22 nF. The signal is clamped at the input to an internal reference voltage. The 1 kΩ luminance delay line can be applied because the luminance impedance is very high. Consequently the charging and discharging currents of the coupling capacitor are very small and do not influence the signal level at the input noticeably. Additionally the coupling capacitor value may be small.

### 11. Brightness control

The black level of the RGB outputs can be set by the voltage on this pin (see Fig. 4). The minimum black level is identical to the blanking level. The black level can be set higher than 4 V, however, the available output signal amplitude is reduced (see also pin 7). Brightness control also operates on the black level of the inserted signals.

### 12, 14, 16. RGB outputs

The output circuits for red, green and blue are identical. Output signals are 5,3 V (black-white) for nominal input signals and control settings. The black levels of the three outputs have the same value. The blanking level at the outputs is 2,1 V. The peak-white level is limited to 9 V. When this level is exceeded the output signal amplitude is reduced via the contrast control (see also pin 7).

### 13, 15, 17. Inputs for external RGB signals

The external signals must be a.c.-coupled to the inputs via a coupling capacitor of about 100 nF. Source impedance should not exceed 150 Ω. The input signal required for a 5 V peak-to-peak output signal is 1 V peak to peak. At the RGB outputs the black level of the inserted signal is identical to that of normal RGB signals. When these inputs are not used the coupling capacitors have to be connected to ground (pin 27).

### 18, 19, 20. Black level clamp capacitors

The black level clamp capacitors for the three channels are connected to these pins. The value of each capacitor should be about 100 nF.

### 21, 22. Demodulator input and reference signal phase adjustment

The (R-Y) and (B-Y) demodulator inputs are internally connected (pin 21). The phase angle between the two reference carriers is 115°. At the nominal hue adjustment the (B-Y) signal is demodulated with a difference of 0°. The phase shift of 115° can be changing the voltage at pin 22. The gain at the two demodulators is identical. The (G-Y) is composed of –0,27(R-Y) –0,22(B-Y).

### 23, 25. Hue control

The hue control is obtained by changing the phase of the input signal of the burst phase detector with respect to the demodulator input signal. This phase shift is obtained by generating a 90° shifted sine-wave via a Miller integrator (biased via pin 23) which is mixed with the original burst signal.

## APPLICATION INFORMATION (continued)

### 24, 26. Reference oscillator

As the burst phase detector has an asymmetrical output the oscillator can be adjusted by changing the voltage of the output (pin 24) via a high-ohmic resistor. The capacitor in series with the oscillator crystal must then have a fixed value. When pin 6 (saturation control) is connected to the positive supply line the burst phase detector is based in its nominal position and the colour killer is overruled. This position can therefore be used for the adjustment of the oscillator.

### 27. Ground

### 28. Output of the chrominance amplifier

The (R-Y) and (B-Y) demodulator input (pin 21) is a.c.-coupled to this output.

# NTSC DECODER

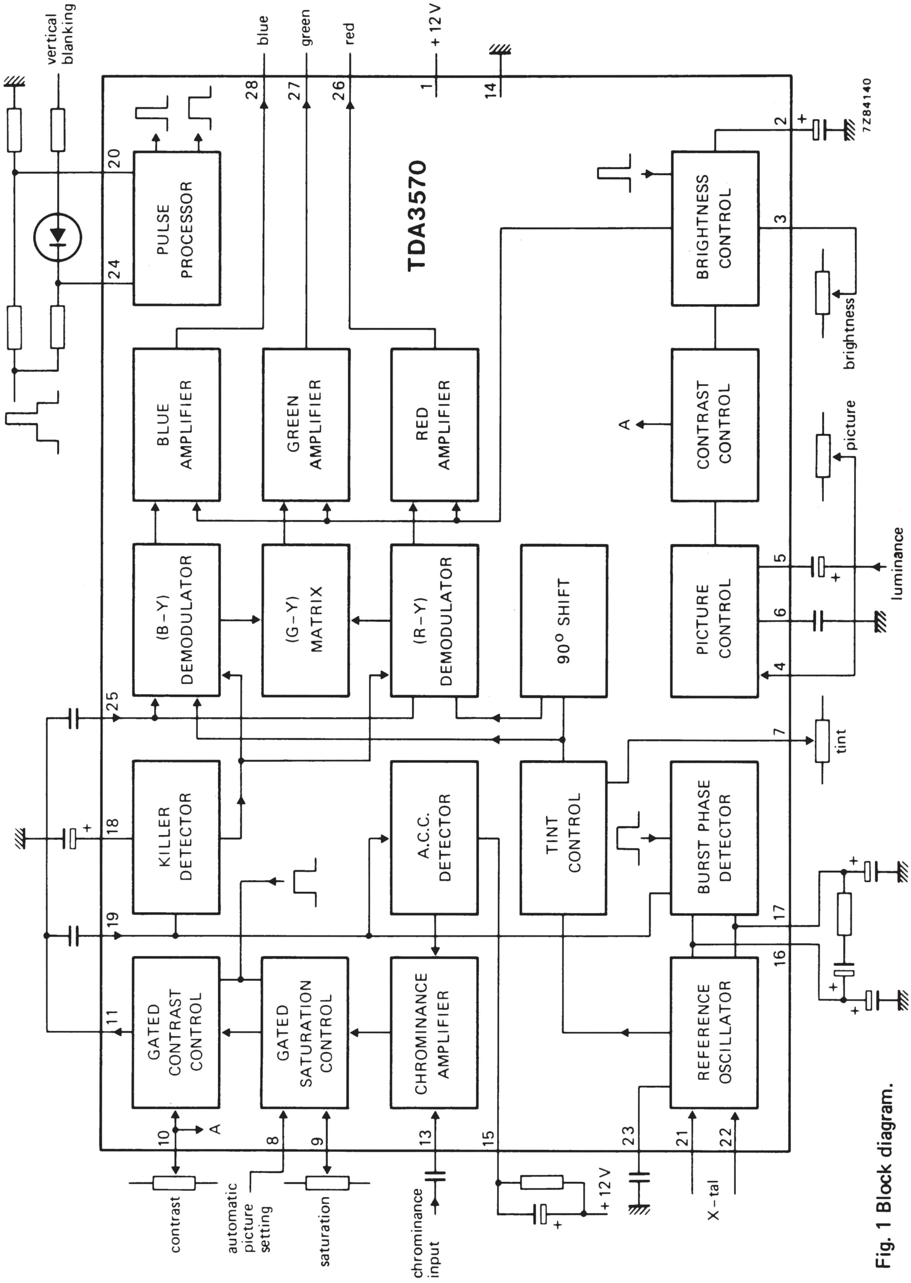
The TDA3570 is a monolithic integrated colour decoder for the NTSC standard. It combines all functions required for the identification and demodulation of NTSC signals. Furthermore it contains a luminance amplifier, an RGB-matrix and amplifier. The amplifier supplies output signals up to 3,5 V peak-to-peak (picture information) enabling direct drive of the output stages. The circuit also contains an automatic picture setting switch to preset positions of both saturation and tint controls.

## QUICK REFERENCE DATA

| | | | | |
|---|---|---|---|---|
| Supply voltage | $V_{1-14}$ | typ. | 12 | V |
| Supply current | $I_1$ | typ. | 43 | mA |
| Luminance input signal (peak-to-peak value) | $V_{5-14(p-p)}$ | typ. | 1 | V |
| RGB output signals (peak-to-peak value) | $V_{26,27,28-14(p-p)}$ | typ. | 3,5 | V |
| Contrast control range | | typ. | 13 | dB |
| Blanking pulse and black level gating input voltage | $V_{24,20-14}$ | $\geqslant$ | 2 | V |
| Chrominance input voltage (peak-to-peak value) | $V_{13-14(p-p)}$ | | 10 to 300 | mV |
| Saturation control range | | $\geqslant$ | 40 | dB |
| Tint control range | | typ. | ± 45° | |

## PACKAGE OUTLINE

28-lead DIL; plastic


TDA3570
PULSE PROCESSOR
BLUE AMPLIFIER
GREEN AMPLIFIER
RED AMPLIFIER
(B−Y) DEMODULATOR
(G−Y) MATRIX
(R−Y) DEMODULATOR
90° SHIFT
KILLER DETECTOR
A.C.C. DETECTOR
TINT CONTROL
BURST PHASE DETECTOR
GATED CONTRAST CONTROL
GATED SATURATION CONTROL
CHROMINANCE AMPLIFIER
REFERENCE OSCILLATOR
BRIGHTNESS CONTROL
CONTRAST CONTROL
PICTURE CONTROL
vertical blanking
blue
green
red
+ 12 V
28
27
26
1
14
20
24
25
18
19
11
10
8
9
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15
23
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16
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4
6
5
3
2
A
A
+
contrast
automatic picture setting
saturation
chrominance input
+ 12 V
X − tal
tint
luminance
picture
brightness
7Z84140

Fig. 1 Block diagram.

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | min. | max. | |
|---|---|---|---|---|
| Supply voltage | $V_P = V_{1\text{-}14}$ | 0 | 14,4 | V |
| Input saturation voltage | $V_{9\text{-}14}$ | 0 | $V_P$ | V |
| Input contrast voltage | $V_{10\text{-}14}$ | 0 | $V_P$ | V |
| Input tint voltage | $V_{7\text{-}14}$ | 0 | $V_P$ | V |
| Input picture voltage | $V_{4\text{-}14}$ | 0 | $V_P$ | V |
| Input brightness voltage | $V_{3\text{-}14}$ | 0 | $V_P$ | V |
| Input sandcastle current | $I_{20}$ | –30 | – | mA |
| Input blanking pulse voltage | $V_{24\text{-}14}$ | –6 | $V_P$ | V |
| Power dissipation at $T_{amb}$ = 70 °C | | | 750 | mW |
| Storage temperature | $T_{stg}$ | –40 to | + 125 | °C |
| Operating ambient temperature | $T_{amb}$ | –20 to | + 70 | °C |

## CHARACTERISTICS

$V_{1\text{-}14} = 12$ V; $V_{5\text{-}14(p\text{-}p)} = 1$ V; $V_{13\text{-}14(p\text{-}p)} = 150$ mV;
$T_{amb} = 25$ °C; measured in Fig. 2

| | | | | |
|---|---|---|---|---|
| Supply voltage | $V_{1\text{-}14}$ | typ. | 12 | V |
| Supply current | $I_1$ | typ. | 43 | mA |

**Luminance**

| | | | | |
|---|---|---|---|---|
| Input voltage (positive-going sync pulse; peak-to-peak value) | $V_{5\text{-}14(p\text{-}p)}$ | typ. | 1 | V |
| Video gain | $G_v$ | typ. | 5 | |
| Contrast control voltage range | $V_{10\text{-}14}$ | | 0 to 12 | V |
| Contrast control range | | typ. | 13 | dB |
| Brightness control voltage range | $V_{3\text{-}14}$ | | 8 to 10 | V |
| Black level range | $V_{26,27,28\text{-}14}$ | | 0 to 7 | V* |
| Max. output voltage | $V_{26,27,28\text{-}14}$ | typ. | 7 | V |
| Blanking and gating pulse | $V_{24\text{-}14}$ | typ. | $\geqslant 2$ | V |
| Input impedance (pin 24) | $\lvert Z_{24\text{-}14} \rvert$ | typ. | 1,5 | kΩ |
| Black level clamp and burst gating pulse | $V_{20\text{-}14}$ | typ. | $\geqslant 2$ | V |
| Input impedance (pin 20) | $\lvert Z_{20\text{-}14} \rvert$ | typ. | 3 | kΩ |

Input circuit: 3 pF in parallel with 9 kΩ

Output circuit: emitter followers with internal $R_E$ = 2,2 kΩ

| | | | | |
|---|---|---|---|---|
| Picture control voltage | $V_{4\text{-}14}$ | | 0 to 12 | V |

---

* Usable range depends on the output signal amplitude.

**Chrominance**

| | | | | |
|---|---|---|---|---|
| Input voltage (peak-to-peak value) | $V_{13\text{-}14(p\text{-}p)}$ | typ. | 150 | mV |
| A.C.C. control range | | typ. | 30 | dB |
| Colour kill level (peak-to-peak value) | $V_{13\text{-}14(p\text{-}p)}$ | typ. | 5 | mV |
| Saturation control voltage range | $V_{9\text{-}14}$ | | 1 to 6 | V |
| Saturation control range | | typ. | 40 | dB |
| Saturation control range in position AUTO* | | typ. | 6 | dB |
| Tint control voltage range | $V_{7\text{-}14}$ | | 1 to 6 | V |
| Tint control range | | typ. | ± 45° | |
| Tint control range in position AUTO* | | typ. | ± 17° | |
| Pull in range of oscillator | | typ. | ± 600 | Hz |
| Phase difference for 100 Hz change of burst | | typ. | ± 1,5° | |

Input circuit: 6 pF in parallel with 3 kΩ

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* Depends on the ratio of R1/R2 in Fig. 2; position AUTO: switch closed.

## APPLICATION INFORMATION

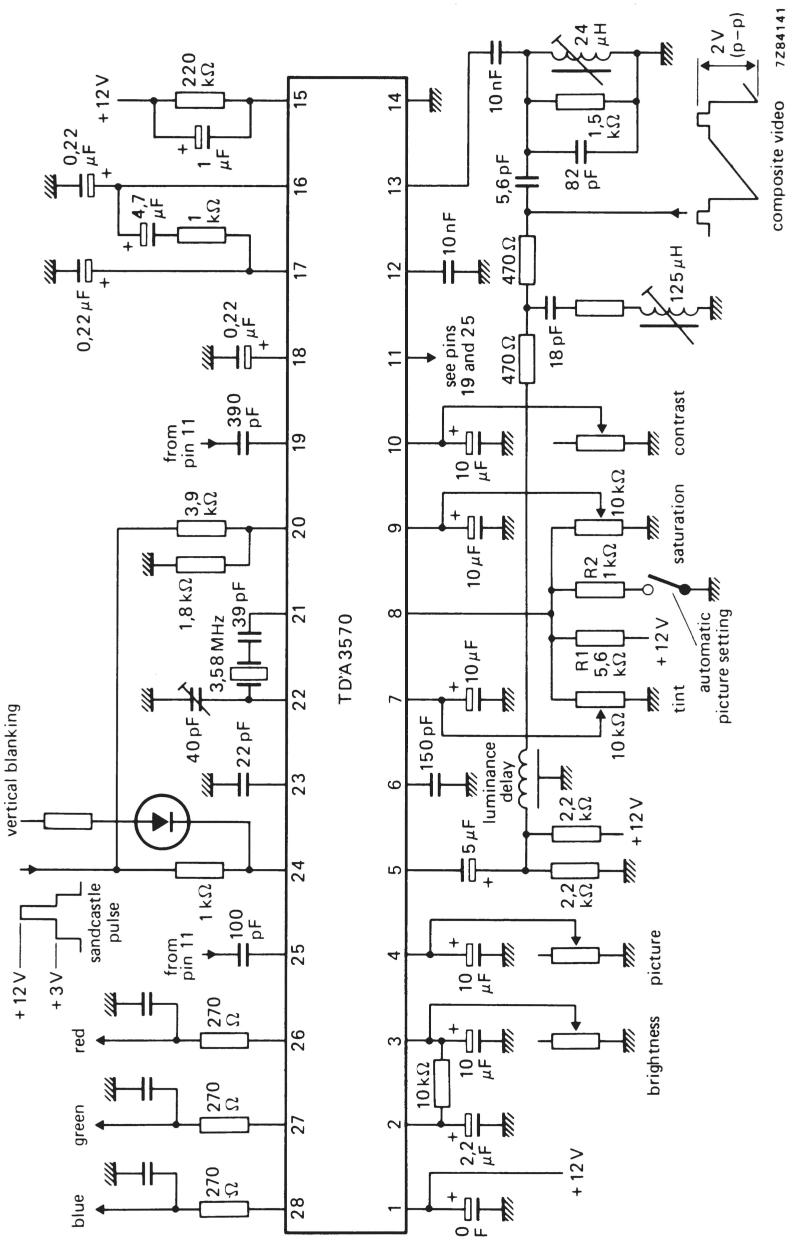
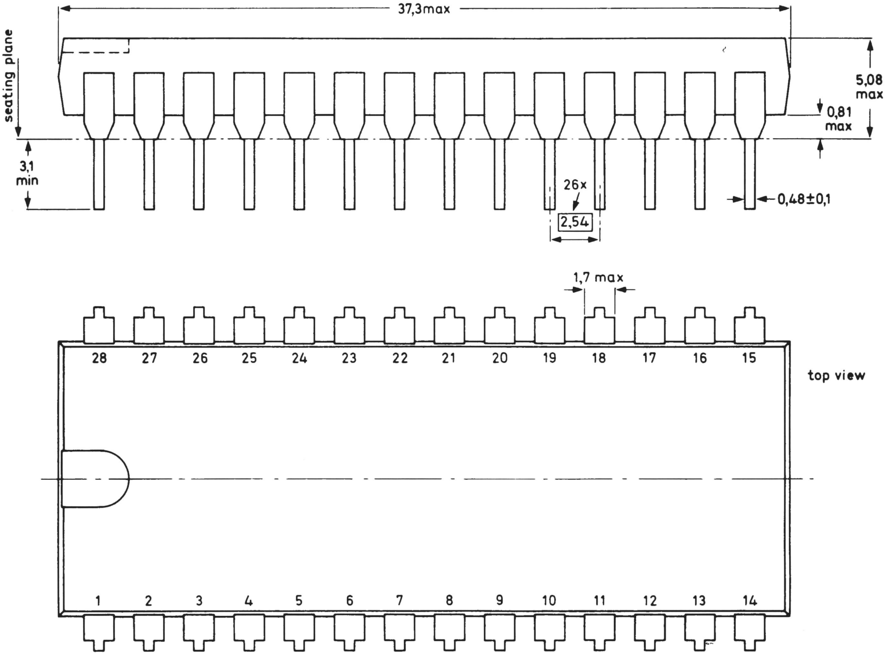
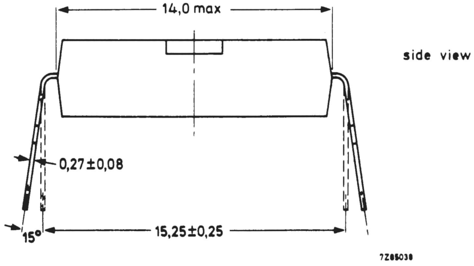

TDA3570
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28
blue
green
red
270 Ω
270 Ω
270 Ω
+12 V
+3 V
sandcastle pulse
from pin 11
100 pF
1 kΩ
vertical blanking
22 pF
40 pF
3,58 MHz
39 pF
1,8 kΩ
3,9 kΩ
from pin 11
390 pF
0,22 µF
0,22 µF
4,7 µF
1 kΩ
0,22 µF
+12 V
220 kΩ
1 µF
+
100 µF
+12 V
2,2 µF
10 kΩ
10 µF
brightness
10 µF
picture
5 µF
2,2 kΩ
2,2 kΩ
+12 V
luminance delay
150 pF
10 µF
10 kΩ
tint
R1 5,6 kΩ
+12 V
R2 1 kΩ
automatic picture setting
10 kΩ
saturation
10 µF
10 µF
contrast
see pins 19 and 25
470 Ω
18 pF
125 µH
470 Ω
10 nF
5,6 pF
82 pF
1,5 kΩ
10 nF
24 µH
composite video
2 V (p–p)
7Z84141

Fig. 2 Application circuit.

## 28-LEAD DUAL IN-LINE; PLASTIC


37,3max
seating plane
5,08
max
0,81
max
3,1
min
26x
2,54
0,48±0,1
1,7 max
28
27
26
25
24
23
22
21
20
19
18
17
16
15
top view
1
2
3
4
5
6
7
8
9
10
11
12
13
14


14,0 max
side view
0,27±0,08
15°
15,25±0,25
7Z85038

DEVELOPMENT SAMPLE DATA
This information is derived from development samples made available for evaluation. It does not necessarily imply that the device will go into regular production.

# SYNC COMBINATION WITH TRANSMITTER IDENTIFICATION AND VERTICAL 625 DIVIDER SYSTEM

## GENERAL DESCRIPTION

The TDA3571B is a monolithic integrated circuit for use in colour television receivers with switched-mode driven or self-regulating horizontal time-base circuits. It is designed in combination with the TDA2581 to operate as a matched pair. When supplied with a composite video signal the TDA3571B delivers drive pulses for the TDA2581 and sync pulses for the vertical deflection. The circuit is optimized for a horizontal and vertical frequency ratio of 625. It incorporates the following features:

### Features

- Horizontal sync separator (including noise inverter)
- Horizontal phase detector
- Horizontal oscillator (31,25 kHz)
- Sandcastle pulse generator
- Vertical sync pulse separator
- Very stable automatic vertical synchronization due to the 625 divider system, without delay after channel change
- Three voltage level sensor on coincidence detector circuit output
- Video transmitter identification circuit for sound muting and search tuning systems
- Inhibit of vertical sync pulse when no video transmitter is detected

## QUICK REFERENCE DATA

| | | | | |
|---|---|---|---|---|
| Supply voltage | | | | |
| horizontal (pin 14) | $V_{14-13}$ | typ. | 12 | V |
| vertical (pin 18) | $V_{18-13}$ | typ. | 12 | V |
| Supply current (pin 14 + pin 18) | $V_{14+18}$ | typ. | 52 | mA |
| Sync separator | | | | |
| input voltage level (peak-to-peak value) | $V_{2-13(p-p)}$ | 0,07 to | 1 | V |
| slicing level | | typ. | 50 | % |
| Output pulse | | | | |
| horizontal (peak-to-peak value) | $V_{8-13(p-p)}$ | min. | 10 | V |
| vertical sync (peak-to-peak value) | $V_{1-13(p-p)}$ | min. | 10 | V |
| burst key (peak-to-peak value) | $V_{15-13(p-p)}$ | min. | 10 | V |
| Video transmitter identification circuit | | | | |
| Output voltage (pin 10) | | | | |
| sync pulse present | $V_{10-13}$ | typ. | 8 | V |
| no sync pulse | $V_{10-13}$ | max. | 1 | V |
| Phase locked loop | | | | |
| control sensitivity | | typ. | 2000 | Hz/µs |
| holding range | Δf | typ. | ± 1000 | Hz |
| catching range | Δf | typ. | ± 900 | Hz |
| Operating ambient temperature range | $T_{amb}$ | −25 to + | 65 | °C |

## PACKAGE OUTLINE

18-lead DIL; plastic (SOT-102A).

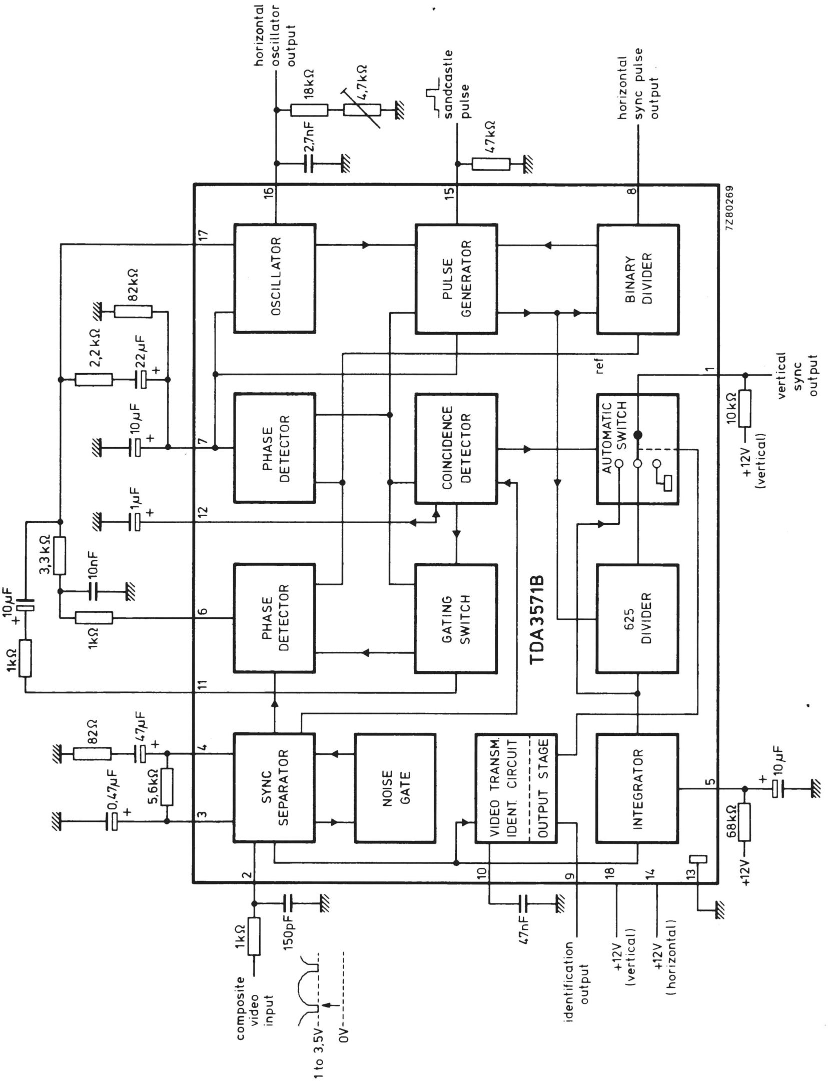

horizontal oscillator output
18kΩ
4,7kΩ
2,7nF
sandcastle pulse
47kΩ
horizontal sync pulse output
7Z80269
82kΩ
2,2kΩ
22μF
10μF
1μF
3,3kΩ
10nF
10μF
1kΩ
1kΩ
82Ω
47μF
0,47μF
5,6kΩ
OSCILLATOR
PULSE GENERATOR
BINARY DIVIDER
PHASE DETECTOR
COINCIDENCE DETECTOR
AUTOMATIC SWITCH
PHASE DETECTOR
GATING SWITCH
625 DIVIDER
SYNC SEPARATOR
NOISE GATE
VIDEO TRANSM. IDENT. CIRCUIT
OUTPUT STAGE
INTEGRATOR
TDA3571B
ref
17
16
15
8
7
12
6
11
4
3
2
10
9
18
14
13
1
5
vertical sync output
10kΩ
+12V (vertical)
10μF
68kΩ
+12V
1kΩ
150pF
47nF
composite video input
1 to 3,5V
0V
identification output
+12V (vertical)
+12V (horizontal)

Fig. 1 Block diagram.

## FUNCTIONAL DESCRIPTION

The video input voltage to drive the sync separator must have negative-going sync, which can be obtained from synchronous demodulators such as TDA2540, TDA2541 and TDA2670.

The slicing level of the sync separator is determined by the value of the resistor between pins 3 and 4. A 5,6 kΩ resistor provides a slicing level midway between the top sync level and the blanking level. Thus the slicing level is independent of the amplitude of the sync pulse input at pin 2.

The nominal top sync level at pin 2 is 1,5 V, and the amplitude selective noise inverter is activated at 0,7 V. The horizontal phase detector has a steepness of 1,2 V/μs and together with the 1800 Hz/V of the horizontal oscillator provides a total control steepness of 2000 Hz/μs.

A second horizontal phase detector provides a 5,5 μs pulse which ensures symmetrical gating of the horizontal synchronization. During catching the gating is automatically switched off. At the same time the flywheel filter is switched to a short time constant. The value of this time constant can be determined externally via pin 11.

When the indirect vertical sync output is generated by the 625 divider system an anti-top flutter pulse switches off the equalizing and vertical sync pulse operation of the phase detector. Thus top flutter distortion of the control voltage due to vertical pulses can be anticipated. When the 625 divider system is in the direct mode the anti-top flutter pulse is inhibited.

The free running output frequency of the horizontal oscillator is 31,25 kHz. The vertical frequency output is obtained by dividing this double horizontal frequency by 625. The double horizontal frequency is fed via a binary divider to provide the normal 15,625 kHz horizontal output at pin 8. The trailing edge of this pulse is positioned 0,9 μs after the end of the video sync pulse input at pin 2 (see Fig. 2).

The automatic vertical sync block contains the following:

- 625 divider
- In/out-sync detector
- Direct/indirect sync switch
- Identification circuit

It is fed by a signal obtained by integration of the composite sync signal and an internally generated, clipped video signal. The vertical sync pulse is sliced out of this integrated signal by an automatically biased clipper. The videopart of the signal helps to build up a vertical sync pulse when heavy negative-going reflections (mountains) distort the video signal. The in/out sync-detector considers a signal out-of-sync when fifteen or more successive incoming vertical sync pulses are not in phase with a reference signal from the 625 divider. Therefore a distorted vertical sync signal needs only one out-of-fifteen pulses to be in phase to keep the system in sync. When the sixteenth successive out-of-sync pulse is detected, the direct/indirect sync switch is activated to feed the vertical sync signal directly out of the block at pin 2 (direct sync vertical output).
At the same time the 625 divider is reset by one of the sync pulses. After the reset pulse, if the 7th sliced vertical sync pulse coincides with a 625 divider window, the sync output pulse is presented again by the divider system and switch-over to indirect mode occurs.
In the direct mode, every 7th non-coinciding sliced vertical sync pulse will reset the counter. Thus a non-standard video signal will result in continuous reset pulses and the direct/indirect switch will remain in the direct position.

To avoid delay in vertical synchronization, caused by waiting time of the divider circuit after channel change or an unsynchronized camera change in the studio, information is fed from the horizontal coincidence detector to the automatic switch for the vertical sync pulse. The loss of horizontal synchronization sets the automatic switch to direct vertical sync. When horizontal coincidence is detected again the setting of the automatic switch depends on whether a standard video signal is received or not. When an external voltage between 2,5 V and 7,25 V is applied via pin 12 to the coincidence detector, the horizontal phase detector is switched to a short time constant and the automatic switch to direct vertical

## FUNCTIONAL DESCRIPTION (continued)

sync. A voltage level on pin 12 > 8,25 V switches the horizontal phase detector to a short time constant, without affecting the indirect/direct vertical sync system which remains operational.

The video transmitter identification circuit detects when a sync pulse occurs during the internal gating pulse. This indicates the presence of a video transmitter and results in the capacitor connected to pin 10 being charged to 8 V. When no sync pulse is present the capacitor discharges to < 1 V. The voltage at pin 10 is compared with an internal d.c. voltage. The identification output at pin 9 is active when pin 10 is < 1,6 V (no video transmitter) and inactive (high impedance) when pin 10 is > 3,5 V. The vertical sync output pulse at pin 1 is inhibited when no video transmitter is identified, which prevents interference or noise affecting the frequency of the vertical output stage. This results in a vertical stable picture, plus vertical stable position information of tuning systems.

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | | |
|---|---|---|---|---|
| Supply voltage | | | | |
| horizontal (pin 14) | $V_{14\text{-}13}$ | max. | 13,2 | V |
| vertical (pin 18) | $V_{18\text{-}13}$ | max. | 13,2 | V |
| Total power dissipation | $P_{tot}$ | max. | 1020 | mW |
| Storage temperature range | $T_{stg}$ | −25 to | +130 | °C |
| Operating ambient temperature range | $T_{amb}$ | −25 to | +65 | °C |

## CHARACTERISTICS

$V_{14\text{-}13}$ = 12 V; $V_{18\text{-}13}$ = 12 V; $T_{amb}$ = 25 °C unless otherwise specified

| parameter | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| **Supply** (pins 14 and 18) | | | | | |
| Supply voltage range | $V_{14;18\text{-}13}$ | 10 | 12 | 13,2 | V |
| Supply current (pin 14 + pin 18) | $I_{14} + I_{18}$ | — | 52 | 77 | mA |
| **Sync separator and noise gate** (pin 2) | | | | | |
| Top sync level (note 1) | $V_{2\text{-}13}$ | 1 | 1,5 | 3,5 | V |
| Sync pulse amplitude (peak-to-peak value) (note 2) | $V_{2\text{-}13(p\text{-}p)}$ | 0,07 | — | 1 | V |
| Noise level | $V_{2\text{-}13}$ | 0,5 | 0,7 | 1,1 | V |
| Slicing level (note 3) | | 35 | 50 | 65 | % |
| Delay between sync input at pin 2 and phase detector output at pin 6* | $t_d$ | — | 0,40 | — | μs |
| **Phase detector** (pin 6) | | | | | |
| Control voltage | $V_{6\text{-}13}$ | 0,5 | 2,8 | 5 | V |
| Control sensitivity | | — | 1,2 | — | V/μs |
| **Phase locked loop** | | | | | |
| Holding range (note 4) | Δf | — | ± 1000 | — | Hz |
| Catching range (note 4) | Δf | ± 600 | ± 900 | — | Hz |
| Control sensitivity | | — | 2000 | — | Hz/μs |
| Phase modulation due to hum on the supply line (note 5) | | — | 2 | — | μs/V |

DEVELOPMENT SAMPLE DATA

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* See waveforms Fig. 2.

CHARACTERISTICS (continued)

| parameter | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| **Horizontal oscillator** | | | | | |
| Output frequency | | | | | |
| free running | $f_o$ | – | 31,250 | – | kHz |
| at pin 8 | $f_8$ | – | 15,625 | – | kHz |
| Temperature coefficient | T | – | $2,5 \times 10^{-4}$ | – | $K^{-1}$ |
| Frequency variation | | | | | |
| without tolerance of external components | $\Delta f_o$ | – | – | 4 | % |
| when voltage at pin 14 drops to 6 V | $\Delta f_o$ | – | – | 10 | % |
| when voltage at pin 14 increases from 10 to 13,2 V | $\Delta f_o$ | – | – | 0,5 | % |
| Output pin 8 | | | | | |
| voltage (no load; peak-to-peak value) | $V_{8-13(p-p)}$ | 10 | – | – | V |
| current (peak-to-peak value) | $I_{8(p-p)}$ | – | 10 | 25 | mA |
| Output resistance | $R_{8-13}$ | – | 433 | – | Ω |
| Output pulse duty factor | $\delta$ | – | 54 | – | % |
| Delay between trailing edge of output pulse and end of sync pulse at pin 2 | $t_d$ | – | 0,9 | – | μs |
| **Sandcastle pulse** (pin 15) | | | | | |
| Output voltage (peak-to-peak value) | $V_{15-13(p-p)}$ | 9 | – | – | V |
| Duration of upper part of output pulse* | $t_p$ | 3 | 3,6 | 4,4 | μs |
| Duration of lower part of output pulse* | $t_p$ | 8,4 | 8,8 | 9,2 | μs |
| Amplitude of lower part of output pulse (peak-to-peak value)* | $V_{15-13(p-p)}$ | 4 | 4,5 | 5 | V |
| Output impedance | $\|Z_o\|$ | – | 200 | – | Ω |
| Delay between trailing edge of sync pulse at pin 2 and leading edge of sandcastle pulse at pin 15* | $t_d$ | – | 0,9 | – | μs |

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* See waveforms Fig. 2.

| parameter | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| **Vertical sync pulse** (pin 1) | | | | | |
| Output voltage (peak-to-peak value) | $V_{1\text{-}13(p\text{-}p)}$ | 10 | – | – | V |
| Load resistor to pin 18 | $R_L$ | 4 | – | – | kΩ |
| Duration of output pulse during indirect synchronization | $t_p$ | – | 170 | – | μs |
| **Video transmitter identification circuit Pin 10** | | | | | |
| Sync pulse present | | | | | |
| charge current | $I_{10}$ | – | + 100 | – | μA |
| output voltage | $V_{10\text{-}13}$ | – | 8 | – | V |
| No sync pulse | | | | | |
| discharge current | $I_{10}$ | – | –100 | – | μA |
| output voltage | $V_{10\text{-}13}$ | – | – | 1 | V |
| Switching level output stage | | | | | |
| pin 9 active when: | $V_{10\text{-}13}$ | 1,6 | 1,9 | 2,5 | V |
| pin 9 inactive when: | $V_{10\text{-}13}$ | 3,0 | 3,5 | 4,0 | V |
| **Pin 9** (note 6) | | | | | |
| Sync pulse present | | | | | |
| output current inactive | $I_9$ | – | – | 1 | μA |
| No sync pulse | | | | | |
| output current active | $I_9$ | 2,5 | 4,0 | 5,0 | mA |
| output voltage active (load ⩽ 0,1 mA) | $V_{9\text{-}13}$ | 10,5 | 11,0 | – | V |
| **Coincidence detector** (pin 12) | | | | | |
| First switching level (note 7) | | | | | |
| voltage | $V_{12\text{-}13}$ | 1,7 | 2,0 | 2,2 | V |
| required input current | $I_{12}$ | 0,8 | – | – | mA |
| maximum allowed input current | $I_{12}$ | – | – | 1,5 | mA |
| Second switching level* (note 8) | | | | | |
| voltage | $V_{12\text{-}13}$ | 7,25 | 7,75 | 8,25 | V |
| required input current | $I_{12}$ | – | 2,2 | 3,0 | mA |
| Voltage | | | | | |
| normal conditions | $V_{12\text{-}13}$ | – | 0,4 | – | V |
| out-of-sync | $V_{12\text{-}13}$ | – | 2,5 | – | V |
| during noise | $V_{12\text{-}13}$ | – | 1,0 | – | V |

* VDR conditions.

**Notes to characteristics**

1. The video signal at pin 2 must have negative-going sync.
2. Up to 1 V peak-to-peak the slicing level is constant; at amplitudes exceeding 1 V peak-to-peak the slicing level will increase.
3. The slicing level is determined by the value of the resistor between pin 3 and pin 4. The 50% figure is obtained with a 5,6 kΩ resistor.
4. Values of external circuitry as shown in Fig. 1.
5. The voltage is a peak-to-peak value; the figure can be reduced to 0,6 μs/V (p-p) by connecting a 330 nF capacitor between pins 7 and 14.
6. The video transmitter identification output stage at pin 9 consists of a p-n-p current source with an n-p-n emitter-follower.
7. A voltage level between 2,5 V and 7,25 V switches the horizontal phase detector to a short time constant and the automatic switch to direct vertical sync.
8. A voltage level > 8,25 V switches the horizontal phase detector to a short time constant without affecting the operation of the automatic switch.

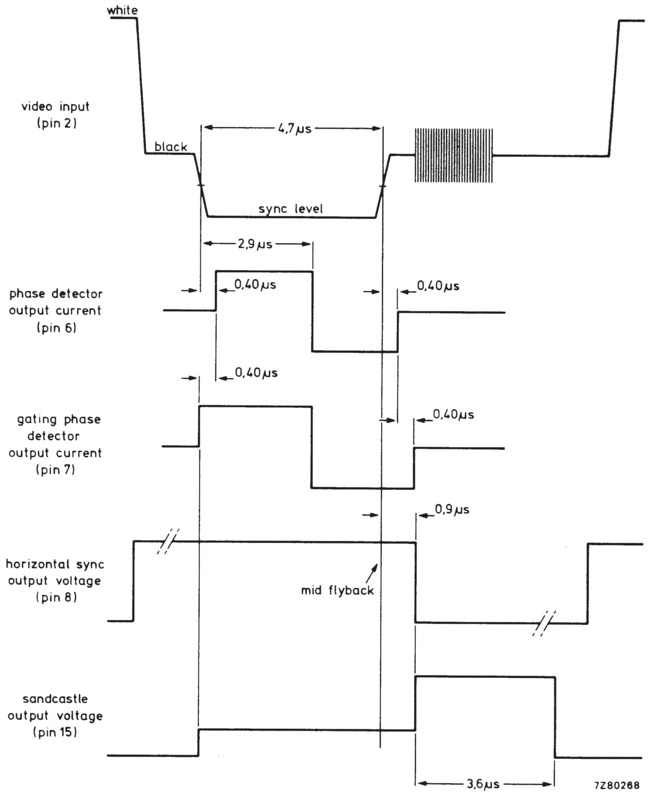
white
video input (pin 2)
black
4,7 μs
sync level
2,9 μs
phase detector output current (pin 6)
0,40 μs
0,40 μs
0,40 μs
gating phase detector output current (pin 7)
0,40 μs
0,9 μs
horizontal sync output voltage (pin 8)
mid flyback
sandcastle output voltage (pin 15)
3,6 μs
7Z80288

Fig. 2 Phase relationship between the input and output signals of the TDA3571B.

## APPLICATION INFORMATION (see also Fig. 3)

The function is described against the corresponding pin number.

### 1. Vertical output pulse

A 10 kΩ resistor must be connected between pin 1 and the positive vertical supply line at pin 18. The pulse is obtained from the 625 divider circuit when standard input signals are received or from the sync separator when the signals are non-standard. The pulse is inhibited when no video transmitter is detected.

### 2. Video input

The video input signal must have negative-going sync pulses. The top-sync level can vary between 1 V and 3,5 V without affecting the sync separator operation. The slicing level is fixed at 50% for the sync pulse amplitude range 0,07 to 1 V which provides good sync separation down to pulses with an amplitude of 70 mV peak-to-peak. The slicing level is increased for sync pulses in excess of 1 V peak-to-peak. The noise gate is activated at an input level $< 1$ V, thus when noise gating is required the top sync level should be close to the minimum level of 1 V. When i.f. circuits with a noise gate are used (TDA2540; TDA2541) the noise gate of the TDA3571B is not required.

### 3. Sync separator slicing level output

The sync separator slicing level is determined on this pin. A slicing level of 50% is obtained by comparing this level with the black level of the video signal, which is detected at pin 4. The slicing level P is determined by the following formula:

$$P = \frac{R_S}{R_S + T_{hor}/T_{sync} \times 0{,}35\ k\Omega} \times 100\% = \frac{R_S}{R_S + 5{,}6\ k\Omega} \times 100\%$$

where $R_S$ is the resistor (in kΩ) between pins 3 and 4. The capacitor that is connected to pin 3 must be between 0,47 μF and 4,7 μF.

### 4. Black level detector output

The black level of the input signal is detected on this pin. This is required to obtain good sync separator operation. A 47 μF capacitor in series with a resistor of 82 Ω must be connected to this pin. A 5,6 kΩ resistor connected between pin 3 and pin 4 results in a slicing level of 50%.

### 5. Vertical sync pulse integrator biasing network

The vertical sync pulse is obtained by integrating the composite sync signal in an internal RC-network. An external RC-network is required for the correct biasing of this circuit for various input conditions. Typical values are: R = 68 kΩ; C = 10 μF. The resistor influences the delay of the **direct** vertical sync pulse.

### 6. Horizontal phase detector output

The control voltage for the horizontal oscillator is obtained on this pin. The output current is about 2 mA.

### 7. Reference voltage horizontal frequency control stage

This pin has two functions. It is used to decouple the reference voltage for the frequency control of the horizontal (so a good suppression of interference is obtained which may be present on the supply line). It also controls the reference waveform for symmetrical gating of the horizontal synchronization, thus providing good noise immunity.

## APPLICATION INFORMATION (continued)

### 8. Horizontal sync pulse output

This pulse is obtained from the horizontal oscillator via a divider circuit. The duty factor is 54%. The trailing edge of this pulse occurs 0,9 μs after the end of the video sync pulse input at pin 2. Because of this phase relationship the horizontal sync pulse can drive directly the TDA2581.

### 9. Video transmitter identification output

This is an emitter-follower output which will be inactive (high-impedance) when the level at pin 10 is >3,5 V (video transmitter detected). The output will be active high when the level at pin 10 is < 1,6 V (no video transmitter detected). This feature can be used for search-tuning and sound-muting.

### 10. Video transmitter identification

A 47 nF capacitor must be connected to this pin. It charges to a level of 8 V when a sync pulse is detected, and discharges to a level of < 1 V when no sync pulse is detected.

### 11. Gating switch

This pin is used to switch the time constant of the flywheel filter. The pin condition is determined by the coincidence detector (pin 12). During in-sync or when only noise is being received pin 11 assumes ground level, which results in a long time constant and good noise immunity.

### 12. Coincidence detector output

A 1 μF capacitor must be connected to this pin. The output voltage depends on the oscillator condition (synchronized or not) and on the video input signal. There are two switching levels at pin 12. At the first switching level when the output voltage is < 1,85 V, the flywheel filter is switched to a long time constant and the gating of the phase detector is switched on. When the output voltage is > 1,85 V, the flywheel filter has a short time constant, and the gating of the phase detector is switched off. The result is that during noise the flywheel filter time constant remains long thus preventing large shifts in the frequency of the horizontal oscillator (and screening of the horizontal output transformer). At the second switching level when the output voltage is > 8,25 V the sync system is switched to a short time constant while the indirect/direct vertical sync system remains fully operational. This condition is suitable for VCR application.

### 13. Negative supply (ground)

### 14. Positive supply horizontal oscillator

Interference and hum on this supply line can affect the oscillator frequency. It is therefore necessary to have separate decoupling of this pin with respect to pin 18.

### 15. Sandcastle pulse output

This pulse is composed of two parts. The lower part has an amplitude of typ. 4,5 V peak-to-peak and a width of max. 9,2 μs (for phase relationship see Fig. 2). The upper part has a total amplitude in excess of 9 V peak-to-peak and a width of max. 4,4 μs. The leading edge of this pulse has a delay of 0,9 μs with respect to the trailing edge of the sync pulse at the input (pin 2). This pulse can directly drive the burst gate/black level clamp input of the TDA2560.

### 16. RC-network horizontal oscillator

Stable components should be chosen for good frequency stability. For adjusting the frequency a part of the total resistance must be variable. This part must be as small as possible, because of poor stability of variable carbon resistors.
The oscillator can be adjusted when pins 7 and 17 are short circuited (see Fig. 3).

## 17. Horizontal oscillator control pin

## 18. Positive supply sync separator and divider circuit (vertical)

This supply requires only simple decoupling. The typical combined current draw of pins 14 and 18 is 52 mA.

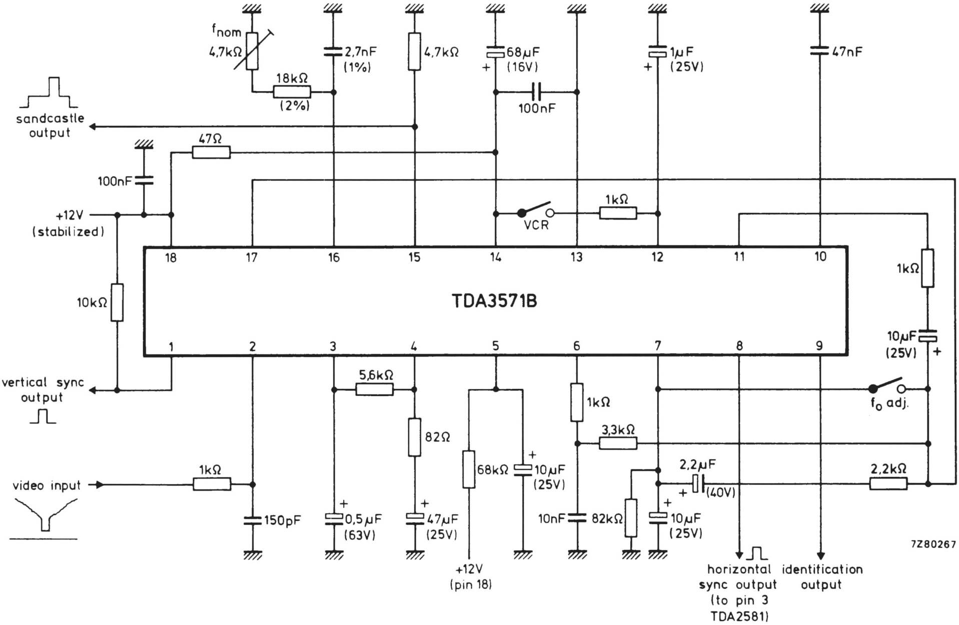
$f_{nom}$
4,7kΩ
18kΩ
(2%)
2,7nF
(1%)
4,7kΩ
68μF
(16V)
100nF
1μF
(25V)
47nF
sandcastle output
47Ω
100nF
+12V
(stabilized)
1kΩ
VCR
10kΩ
TDA3571B
18
17
16
15
14
13
12
11
10
1
2
3
4
5
6
7
8
9
1kΩ
10μF
(25V)
vertical sync output
5,6kΩ
82Ω
68kΩ
10μF
(25V)
1kΩ
3,3kΩ
$f_0$ adj.
video input
1kΩ
150pF
0,5μF
(63V)
47μF
(25V)
10nF
82kΩ
2,2μF
(40V)
10μF
(25V)
2,2kΩ
+12V
(pin 18)
horizontal sync output
(to pin 3
TDA2581)
identification output
7Z80267

Fig. 3 Typical application circuit diagram; for combination of the TDA3571B with the TDA2581.

DEVELOPMENT SAMPLE DATA

This information is derived from development samples made available for evaluation. It does not necessarily imply that the device will go into regular production.

# SYNC COMBINATION WITH TRANSMITTER IDENTIFICATION AND VERTICAL 625 DIVIDER SYSTEM

## GENERAL DESCRIPTION

The TDA3576B is a monolithic integrated circuit for use in colour television receivers. The circuit is optimized for a horizontal and vertical frequency ratio of 625.

### Features

- Horizontal sync separator (including noise inverter) with sliding bias such that the sync pulse is always sliced between top sync level and blanking level
- Phase detector which compares the horizontal sync pulse with the oscillator voltage; this phase detector is gated
- Phase detector which compares the horizontal flyback pulse with the oscillator voltage
- Horizontal oscillator (31,25 kHz)
- Time constant switching of the first control loop (short time constant during catching and reception of VCR signals)
- Burst key pulse generator (sandcastle pulse with three levels)
- Very stable automatic vertical synchronization due to the 625 divider system, without delay after channel change
- Vertical sync pulse separator
- Three voltage level sensor on coincidence detector circuit output
- Video transmitter identification circuit for sound muting and search tuning systems
- Inhibit of vertical sync pulse when no video transmitter is detected

## QUICK REFERENCE DATA

| | | | | |
|---|---|---|---|---|
| Supply voltage (pin 17) | $V_P = V_{17\text{-}10}$ | typ. | 12 | V |
| Supply current (pin 17) | $I_{17}$ | typ. | 70 | mA |
| Sync separator | | | | |
| input voltage level (peak-to-peak value) | $V_{5\text{-}10(p\text{-}p)}$ | | 0,1 to 1 | V |
| slicing level | | typ. | 50 | % |
| Phase-locked-loop | | | | |
| control sensitivity sync to flyback pulse | | typ. | 4 | kHz/μs |
| holding range | Δf | typ. | ± 1000 | Hz |
| catching range | Δf | typ. | ± 900 | Hz |
| Horizontal output pulse (peak-to-peak value) | $V_{11\text{-}10(p\text{-}p)}$ | min. | 11,3 | V |
| Vertical output pulse (peak-to-peak value) | $V_{3\text{-}10(p\text{-}p)}$ | min. | 10 | V |
| Burst key output pulse (peak-to-peak value) | $V_{2\text{-}10(p\text{-}p)}$ | min. | 9 | V |
| Video transmitter identification circuit output voltage (pin 1) | | | | |
| sync pulse present | $V_{1\text{-}10}$ | typ. | 8,4 | V |
| no sync pulse | $V_{1\text{-}10}$ | max. | 1 | V |
| Operating ambient temperature range | $T_{amb}$ | | −25 to + 65 | °C |

## PACKAGE OUTLINE

18-lead DIL; plastic (SOT-102HE4).

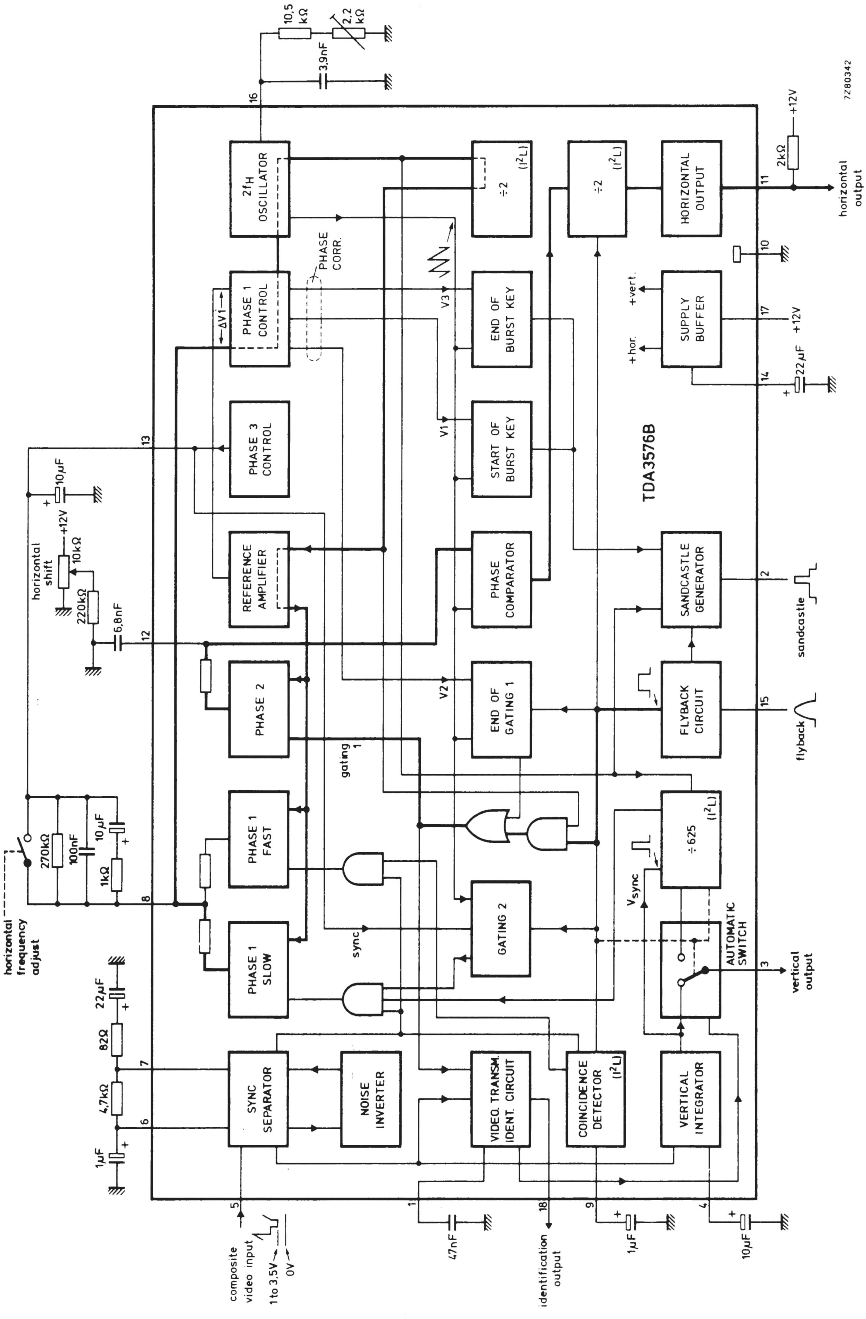
10,5 kΩ
2,2 kΩ
3,9nF
16
2f_H OSCILLATOR
÷2 (I²L)
÷2 (I²L)
HORIZONTAL OUTPUT
2kΩ
+12V
11
horizontal output
7Z80342
PHASE CORR.
ΔV1
PHASE 1 CONTROL
V3
END OF BURST KEY
+vert.
+hor.
SUPPLY BUFFER
10
17
+12V
14
22µF
13
PHASE 3 CONTROL
V1
START OF BURST KEY
TDA3576B
10µF
+12V
horizontal shift
10kΩ
220kΩ
6,8nF
12
REFERENCE AMPLIFIER
PHASE COMPARATOR
SANDCASTLE GENERATOR
2
sandcastle
PHASE 2
V2
END OF GATING 1
FLYBACK CIRCUIT
15
flyback
gating 1
PHASE 1 FAST
÷625 (I²L)
V_sync
270kΩ
100nF
10µF
1kΩ
8
horizontal frequency adjust
PHASE 1 SLOW
sync
GATING 2
AUTOMATIC SWITCH
3
vertical output
22µF
82Ω
7
4,7kΩ
6
1µF
SYNC SEPARATOR
NOISE INVERTER
VIDEO TRANSM. IDENT. CIRCUIT
COINCIDENCE DETECTOR (I²L)
VERTICAL INTEGRATOR
5
composite video input
1 to 3,5V
0V
1
47nF
18
identification output
9
1µF
4
10µF

Fig. 1 Block diagram.

## FUNCTIONAL DESCRIPTION

The video input voltage to drive the sync separator must have negative-going sync, which can be obtained from synchronous demodulators such as TDA2540 and TDA2541.

The slicing level of the sync separator is determined by the value of the resistor between pins 6 and 7. A 4,7 kΩ resistor provides a slicing level midway between the top sync level and the blanking level. Thus the slicing level is independent of the amplitude of the sync pulse input at pin 5.

The nominal top sync level at pin 5 is 3 V, and the amplitude selective noise inverter is activated at 0,7 V.

To obtain good stability the circuit contains three control loops. In the first loop the phase of the horizontal sync pulse is compared with a reference output pulse from the horizontal oscillator. In the second loop the phase of the flyback pulse is compared with the same reference output pulse. The first loop is designed for good noise immunity and the second loop has a fast time constant to compensate quickly for storage variations of the output stage. The second loop also generates a gating signal of about 5,5 μs for use in the transmitter identification circuit. The third control loop generates a second gating signal which is used in the first phase detector. The pulse width is typically 14 μs.

For a short catching time the output current of the first phase detector is not gated but is increased by 5 times during catching. This is caused by the voltage of the coincidence detector at pin 9. For VCR playback conditions the first control loop must be forced to a fast time constant, this is achieved by applying an external voltage of $\geqslant$ 2,7 V to pin 9.

The free running output frequency of the horizontal oscillator is 31,25 kHz. The vertical frequency output is obtained by dividing this double horizontal frequency by 625. The double horizontal frequency is fed via a binary divider to provide the normal 15,625 kHz horizontal output to pin 11.

The sandcastle pulse is generated at pin 2 and has three levels. The burst key pulse is of short duration, typically 4 μs, with an amplitude of 10 V and is the highest level. The second level has a pulse duration equal to the horizontal flyback pulse with an amplitude of 4,5 V and is used for horizontal blanking. The third level, amplitude 2,5 V, is used for vertical blanking and has a pulse duration of 1,34 ms. The last pulse is internally generated by the divider circuit and is only available when a standard video input signal is received. An external vertical blanking pulse can be added to this pin via a suitable series resistor. This pulse will be automatically clamped to 2,5 V.

DEVELOPMENT SAMPLE DATA

The automatic vertical sync block contains the following:

- 625 divider
- In/out-sync detector
- Direct/indirect sync switch
- Identification circuit

It is fed by a signal obtained by integration of the composite video signal and an internally generated, clipped video signal. The vertical sync pulse is sliced out of this integrated signal by an automatically biased clipper. The video part of the signal helps to build up a vertical sync when heavy negative-going reflections (mountains) distort the video signal. The in/out sync-detector considers a signal out-of-sync when fourteen or more successive incoming vertical sync pulses are not in phase with a reference signal from the 625 divider. Therefore a distorted vertical sync signal needs only one out-of-fourteen pulses to be in phase to keep the system in sync. When the fifteenth successive out-of-sync pulse is detected, the direct/indirect sync switch is activated to feed the vertical sync signal directly out of the block at pin 3 (direct sync vertical output).

At the same time the 625 divider is reset by one of the sync pulses. After the reset pulse, if the 7th sliced vertical sync pulse coincides with a 625 divider window, the sync output pulse is presented again by the divider system and switch-over to indirect mode occurs.

In the direct mode, every 7th non-coinciding sliced vertical sync pulse will reset the counter. A non-standard video signal will result in continuous reset pulses and the direct/indirect switch will remain in the direct position.

## FUNCTIONAL DESCRIPTION (continued)

To avoid delay in vertical synchronization, caused by waiting time of the divider circuit after channel change or an unsynchronized camera change in the studio, information is fed from the horizontal coincidence detector to the automatic switch for the vertical sync pulse. The loss of horizontal synchronization sets the automatic switch to direct vertical sync.

When an external voltage between 2,7 V and 8,2 V is applied via pin 9 to the coincidence detector, the horizontal phase detector is switched to a short time constant and the automatic switch to direct vertical sync. A voltage level on pin 9 between 9,2 V and 12 V switches the horizontal phase detector to a short time constant, without affecting the indirect/direct vertical sync system which remains operational. Thus when standard signals are received vertical sync pulses are generated by the divider system.

To avoid disturbance of the horizontal phase detector by the vertical sync pulse the 625 divider system generates an anti-top-flutter pulse. This pulse is applied to the phase 1 detector when a standard video signal is received. The anti-top-flutter pulse is also active for standard VCR signal conditions, voltage at pin 9 $\geqslant$ 9,2 V.

The video transmitter identification circuit detects when a sync pulse occurs during the internal 5,5 $\mu$s gating pulse. This indicates the presence of a video transmitter and results in the capacitor connected to pin 1 being charged to 8,4 V. When no sync pulse is present the capacitor discharges to $<$ 1 V. The voltage at pin 1 is compared with an internal d.c. voltage. The identification output at pin 18 is active when pin 1 is $\leqslant$1,5 V (no video transmitter) and inactive (high impedance) when pin 1 is $>$ 3,5 V, this information can be used for search tuning.

The vertical sync output pulse at pin 3 is inhibited when no video transmitter is identified, which prevents interference or noise affecting the frequency of the vertical output stage. This results in a vertical stable picture, plus vertical stable position information for tuning systems.

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | | |
|---|---|---|---|---|
| Supply voltage (pin 17) | $V_P = V_{17\text{-}10}$ | max. | 13,2 | V |
| Total power dissipation | $P_{tot}$ | max. | 1200 | mW |
| Storage temperature range | $T_{stg}$ | −55 to | +125 | °C |
| Operating ambient temperature range | $T_{amb}$ | −25 to | +65 | °C |

## THERMAL RESISTANCE

| | | | | |
|---|---|---|---|---|
| From junction to ambient (in free air) | $R_{th\,j\text{-}a}$ | = | 50 | K/W |

## CHARACTERISTICS

$V_P = V_{17\text{-}10} = 12$ V; $T_{amb} = 25$ °C; measured in Fig. 3; unless otherwise specified

| parameter | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| **Supply** (pin 17) | | | | | |
| Supply voltage range | $V_P = V_{17\text{-}10}$ | 10,5 | 12 | 13,2 | V |
| Supply current ($V_{17\text{-}10} = 12$ V) | $I_{17}$ | 50 | 70 | 85 | mA |
| Buffer voltage ($V_{17\text{-}10} = 12$ V) | $V_{14\text{-}10}$ | 10,5 | 11 | 11,5 | V |
| **Sync separator and noise gate** (pin 5) | | | | | |
| Top sync level (note 1) | $V_{5\text{-}10}$ | 1,0 | 3,0 | 3,5 | V |
| Sync pulse amplitude (note 2) (peak-to-peak value) | $V_{5\text{-}10(p\text{-}p)}$ | 0,1 | 0,6 | – | V |
| Slicing level (note 3) | | 35 | 50 | 65 | % |
| Delay between sync input at pin 5 and phase detector output at pin 8* | $t_d$ | – | 0,35 | – | μs |
| Noise gate switching level | $V_{5\text{-}10}$ | – | 0,7 | 1,0 | V |
| **Phase detector** (pin 8) | | | | | |
| Control voltage | $V_{8\text{-}10}$ | 0,4 | 2,7 | 5,2 | V |
| Control sensitivity (note 7) | | | | | |
| with slow time constant | | – | 1,0 | – | V/μs |
| with fast time constant | | – | 1,0 | – | V/μs |
| with slow time constant ▲ | | – | 0,7 | – | V/μs |
| **Phase-locked-loop** (pins 8 and 13) | | | | | |
| Holding range (note 4) | Δf | – | ± 1000 | – | Hz |
| Catching range (note 4) | Δf | – | ± 900 | – | Hz |
| Control sensitivity video | | | | | |
| with respect to oscillator** | | – | 2,0 | – | kHz/μs |
| with respect to oscillator▲ | | – | 1,5 | – | kHz/μs |
| with respect to burst key pulse | | – | 7,5 | – | kHz/μs |
| with respect to flyback pulse | | – | 4 | – | kHz/μs |
| Phase modulation due to hum on the supply line; pin 17 (note 4) | | – | – | 1,0 | μs/V |

* See waveforms Fig. 2.

** Without resistor between pins 8 and 13.

▲ 270 kΩ between pins 8 and 13.

**CHARACTERISTICS** (continued)

| parameter | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| **Phase detector** (pin 12) | | | | | |
| Control voltage ($t_d$ = 10 μs) | $V_{12\text{-}10}$ | – | 4,0 | – | V |
| Control sensitivity | | – | 30 | – | V/μs |
| Loop gain phase control * | $\Delta t_d/\Delta t_o$ | – | 250 | – | μs/μs |
| Control range | | | | | |
| C = 6,8 nF (pin 12)* | $t_d$ | 6,5 | – | 24 | μs |
| C = 100 nF (pin 12)* | $t_d$ | 2,2 | – | 24 | μs |
| Phase adjustment | | | | | |
| control sensitivity | | – | 12 | – | μA/μs |
| control range | | –1,5 | – | +3 | μs |
| **Horizontal oscillator** (pin 16) | | | | | |
| Output frequency; $C_{osc}$ = 3,9 nF; $R_{osc}$ = 11,5 kΩ | | | | | |
| free running | $f_o$ | – | 31,250 | – | kHz |
| at pin 11 | $f_{11}$ | – | 15,625 | – | kHz |
| Temperature coefficient | TC | – | $+3 \times 10^4$ | – | $K^{-1}$ |
| Frequency variation | | | | | |
| without tolerance of external components | $\Delta f_o$ | – | – | ±4 | % |
| when supply voltage (pin 17) increases from 10 V to 13,2 V | $\Delta f_o$ | – | 0,2 | – | % |
| at minimum supply voltage | $\Delta f_o$ | – | 1,5 | 5,0 | % |
| **Horizontal output** (pin 11; note 5) | | | | | |
| Maximum supply voltage | $V_{17\text{-}10}$ | – | – | 13,2 | V |
| Voltage at which output is started | $V_{17\text{-}10}$ | 6,2 | 6,7 | 7,2 | V |
| Output voltage high level | $V_{11\text{-}10}$ | – | – | 13,2 | V |
| Output voltage low level | | | | | |
| $I_{11}$ = 10 mA | $V_{11\text{-}10}$ | – | 200 | 400 | mV |
| $I_{11}$ = 50 mA | $V_{11\text{-}10}$ | – | 500 | 700 | mV |
| Output current at voltage low level | $I_{11}$ | – | – | 50 | mA |
| Duration of the output pulse | $t_p$ | | see note 6 | | μs |
| Rise time of the output pulse | $t_r$ | 0,05 | – | 0,3 | μs |
| Protection voltage (pin 11) | | 13 | 14,5 | 15,5 | V |

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* See waveforms Fig. 2.

| parameter | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| **Sandcastle pulse** (pin 2)* | | | | | |
| Output voltage during burst key pulse (peak-to-peak value) | $V_{2\text{-}10(p\text{-}p)}$ | 9 | 10 | – | V |
| Duration of upper level of output pulse | $t_p$ | 3,6 | 4,0 | 4,4 | μs |
| Amplitude of second level of output pulse (peak-to-peak value) | $V_{2\text{-}10(p\text{-}p)}$ | 4,0 | 4,5 | 5,0 | V |
| Duration of second level of output pulse | $t_p$ | | flyback pulse | | μs |
| Amplitude of lower level of output pulse (peak-to-peak value) | $V_{2\text{-}10(p\text{-}p)}$ | 2,0 | 2,5 | 3,0 | V |
| Duration of lower level of output pulse during standard signals (note 8) | $t_p$ | – | 1,34** | – | ms |
| Amplitude at zero level of output pulse | $V_{2\text{-}10}$ | – | – | 1 | V |
| Delay between start of the sync pulse at pin 5 and the rising edge of the burst key pulse at pin 2 | $t_b$ | 4,6 | 4,9 | 5,2 | μs |
| **Phase detector** (pin 13) | | | | | |
| Output voltage | $V_{13\text{-}10}$ | – | 2,8 | – | V |
| Charge current | $I_{13}$ | – | 0,9 | – | mA |
| Discharge current | $I_{13}$ | – | 0,9 | – | mA |
| **Vertical sync pulse** (pin 3) | | | | | |
| Output voltage (peak-to-peak value) | $V_{3\text{-}10(p\text{-}p)}$ | 10 | – | – | V |
| Output current | $I_3$ | – | – | 5 | mA |
| Duration of output pulse during indirect synchronization | $t_p$ | – | 190 | – | μs |
| Phase variation between first vertical sync pulse and start of output pulse in divider mode | | – | – | ± 2,5 | lines |
| **Coincidence detector** (pin 9) | | | | | |
| Switching level (note 7) | $V_{9\text{-}10}$ | 2,1 | 2,4 | 2,7 | V |
| Voltage | | | | | |
| normal conditions (in-sync) | $V_{9\text{-}10}$ | – | 1,3 | – | V |
| out-of-sync | $V_{9\text{-}10}$ | – | 2,7 | – | V |
| during noise | $V_{9\text{-}10}$ | – | 2,1 | – | V |

DEVELOPMENT SAMPLE DATA

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* See waveforms Fig. 2.

** 21 lines.

**CHARACTERISTICS** (continued)

| parameter | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| **Switching levels for VCR** (pin 9) | | | | | |
| Fast time constant for phase 1 | | | | | |
| switching level | $V_{9-10}$ | 2,1 | 2,4 | 2,7 | V |
| input current | $I_9$ | 1,0 | – | 2,0 | mA |
| Vertical sync output indirect/direct with divider system active | | | | | |
| switching level* | $V_{9-10}$ | 8,2 | 8,7 | 9,2 | V |
| input current | $I_9$ | 3,0 | – | 4,0 | mA |
| **Flyback input pulse** (pin 15) | | | | | |
| Switching level | $V_{15-10}$ | – | 0,85 | 1,0 | V |
| Input pulse (peak-to-peak value) | $V_{15-10(p-p)}$ | – | – | 12 | V |
| Input resistance | $R_{15-10}$ | – | 3,5 | – | kΩ |
| Input current | $I_{15}$ | 0,2 | – | 3,0 | mA |
| Delay between the start of the sync pulse at the video input and the leading edge of the flyback pulse | $t_d$ | – | 0,5 | – | μs |
| **Video transmitter identification circuit** | | | | | |
| **Pin 1** | | | | | |
| Sync pulse present | | | | | |
| charge current | $I_1$ | – | +100 | – | μA |
| output voltage | $V_{1-10}$ | – | 8,4 | – | V |
| No sync pulse | | | | | |
| discharge current | $I_1$ | – | –100 | – | μA |
| output voltage | $V_{1-10}$ | – | – | 1 | V |
| Switching level output stage | | | | | |
| pin 18 active when: | $V_{1-10}$ | 1,7 | 2,0 | 2,2 | V |
| pin 18 inactive when: | $V_{1-10}$ | 3,0 | 3,5 | 4,0 | V |
| **Pin 18** (note 9) | | | | | |
| Sync pulse present | | | | | |
| output current inactive | $I_{18}$ | – | – | 1 | μA |
| No sync pulse | | | | | |
| minimum available output current active ($V_{18-10} = 7$ V) | $I_{18}$ | 4,0 | – | – | mA |
| maximum allowed output current | $I_{18}$ | – | – | 10 | mA |
| output voltage active ($I_9 = 1$ mA) | $V_{9-13}$ | 10,5 | 11,0 | $V_{17-10}$ | V |

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* The maximum allowed voltage at pin 9 is $V_P$ (pin 17).

**Notes to characteristics**

1. The video signal at pin 5 must have negative-going sync.
2. Up to 1 V peak-to-peak the slicing level is constant; at amplitudes exceeding 1 V peak-to-peak the slicing level will increase.
3. The slicing level is determined by the value of the resistor between pin 6 and pin 7. The 50% figure is obtained with a 4,7 kΩ resistor. The slicing level P is determined by the formula:

   $P = \frac{R_S}{4880 + R_S} \times 100\%$; where $R_S$ is the resistor between pins 6 and 7.
4. Values of external circuitry as shown in Fig. 1; the voltage in this ratio has a peak-to-peak value.
5. The horizontal output configuration is an open collector with internal high voltage protection during the off-state of the output transistor.
6. The horizontal output pulse width is determined by the horizontal flyback pulse. The circuit is designed such that the horizontal output transistor cannot be switched on during flyback, but is switched on directly after flyback. Thus $t_p$ = switch-off delay of horizontal output stage plus flyback time.
7. When the voltage level at pin 9 is $< 2,1$ V, phase detector 1 (pin 8) is gated. When the level is $> 2,7$ V, the dynamical control sensitivity of the phase detector is raised such that the output current is increased by five times the original amount and the phase detector is not gated.
8. An external vertical blanking pulse can be applied to pin 2 via a series resistor. The required input current is 2 mA. This external pulse is clamped to 2,5 V by internal circuitry.
9. The video transmitter identification output stage at pin 18 consists of a p-n-p current source with an n-p-n emitter-follower.

DEVELOPMENT SAMPLE DATA

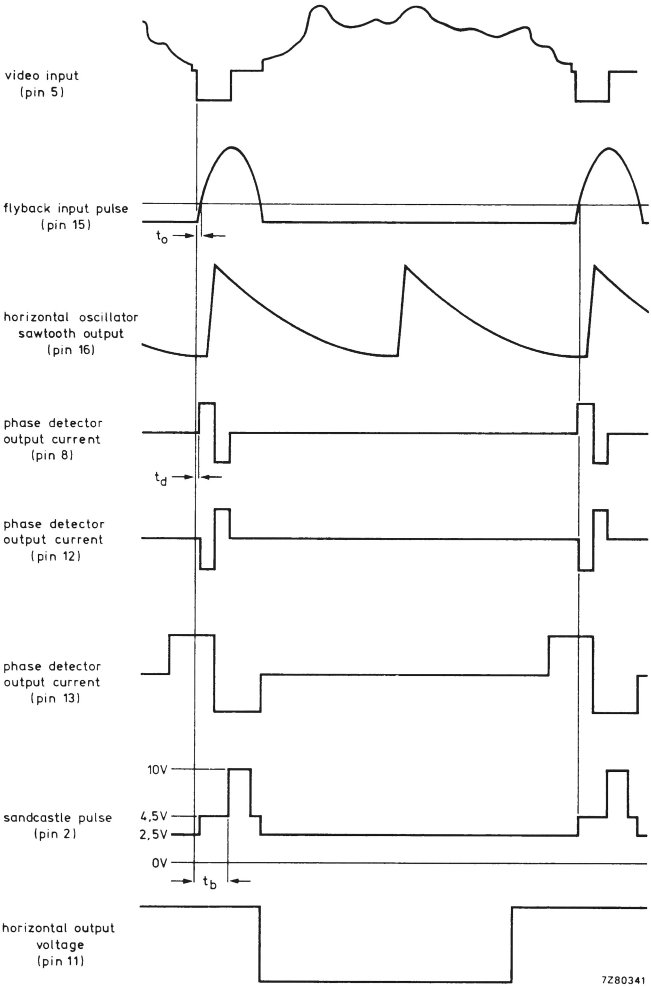

video input
(pin 5)
flyback input pulse
(pin 15)
$t_o$
horizontal oscillator
sawtooth output
(pin 16)
phase detector
output current
(pin 8)
$t_d$
phase detector
output current
(pin 12)
phase detector
output current
(pin 13)
10V
4,5V
2,5V
0V
sandcastle pulse
(pin 2)
$t_b$
horizontal output
voltage
(pin 11)
7Z80341

Fig. 2 Phase relationship between the input and output signals of the TDA3576B.

## APPLICATION INFORMATION (see also Fig. 3)

The function is described against the corresponding pin number.

### 1. Video transmitter identification

A 47 nF capacitor must be connected to this pin. It charges to a level of 8 V when a sync pulse is detected, and discharges to a level of < 1 V when no sync pulse is detected.

### 2. Sandcastle output pulse

This output has three levels. The first and highest level (10 V) is the burst key pulse with a typical duration of 4,0 μs. The second level, for the horizontal blanking, is typically 4,5 V with a pulse duration equal to the horizontal flyback pulse. For the third level an external vertical flyback pulse must be applied to this pin. This pulse will be clamped to 2,5 V by an internal clamping circuit. The input current is typically 2 mA.

### 3. Vertical output pulse

This pulse is obtained from the 625 divider circuit when standard input signals are received or from the sync separator when the signals are non-standard. The pulse is inhibited when no video transmitter is detected. Both pulses have good stability and accuracy and are used to trigger the vertical oscillator.

### 4. Vertical sync pulse integrator biasing network

The vertical sync pulse is obtained by integrating the composite sync signal in an internal RC-network. An external capacitor of 10 μF is required for biasing the vertical sync separator, this provides the vertical sync output pulse with a delay of 37 μs. This value can be changed by an external resistor. A resistor of 470 kΩ between pin 3 and +12 V gives a delay of 45 μs.

### 5. Video input

The video input signal must have negative-going sync pulses. The top-sync level can vary between 1 V and 3,5 V without affecting the sync separator operation. The slicing level is fixed at 50% for the sync pulse amplitude range 0,1 to 1 V which provides good sync separation down to pulses with an amplitude of 100 mV peak-to-peak. The slicing level is increased for sync pulses in excess of 1 V peak-to-peak. The noise gate is activated at an input level < 1 V, thus when noise gating is required the top sync level should be close to the minimum level of 1 V.

### 6. Sync separator slicing level output

The sync separator slicing level is determined on this pin. A slicing level of 50% is obtained by comparing this level with the black level of the video signal, which is detected at pin 7.

### 7. Black level detector output

The black level of the input signal is detected on this pin. This is required to obtain good sync separator operation. A 22 μF capacitor in series with a resistor of 82 Ω must be connected to this pin. A 4,7 kΩ resistor connected between pins 6 and 7 results in a slicing level of 50%.

### 8. Horizontal phase detector output and control oscillator input

The flywheel filter must be connected to this pin. Typical values for the components are a capacitor of 100 nF in parallel with an RC-network of 1 kΩ and 10 μF. Furthermore, a resistor of 270 kΩ should be connected between pins 8 and 13 to limit the free running frequency drift.

The output current of the phase detector depends on the condition of the coincidence detector. The output current is high when the oscillator is out-of-sync. The result is a large catching range, and the phase detector not gated. The output current is low when the oscillator is synchronized and the phase detector is gated; this provides good noise immunity.

## APPLICATION INFORMATION (continued)

### 9. Coincidence detector output

A 1 μF capacitor must be connected to this pin. The output voltage depends on the oscillator condition (synchronized or not) and on the video input signal. The following output voltages can occur:

| | |
|---|---|
| • when in-sync | 1,3 V |
| • when out-of-sync | 2,7 V |
| • during noise at the input | 2,1 V |

There are two switching levels at pin 9. At the first switching level when the output voltage is < 2,1 V, the phase detector output is low and the gating of the phase detector is switched on. When the output voltage is > 2,7 V, the output current of the phase detector is high and the gating of the phase detector is switched off. The result is a large catching range and a high dynamic steepness of the PLL. At the second switching level when the output voltage is > 9,2 V the sync system is switched to a short time constant while the indirect/direct vertical sync system remains fully operational. This condition is suitable for VCR application.

### 10. Negative supply (ground)

### 11. Horizontal sync pulse output

This is an open collector output. The collector resistor mus be chosen such that sufficient current is supplied to the driver stage. The maximum current is 60 mA. The circuit is designed such that the horizontal output transistor cannot be switched on during flyback, but is switched on directly after flyback.

### 12. Control voltage second loop

This voltage controls the output pulse at pin 11 (positive-going edge). The capacitor connected to this pin must have a minimum value of 6,8 nF. A higher value decreases the dynamic-loop gain in the second control loop. When a high dynamic-loop gain is not required a capacitor value of 100 nF is recommended. Horizontal shift is possible by applying an external current to pin 12.

### 13. Reference voltage control loops

The reference voltage must be decoupled by a capacitor of 10 μF.

### 14. Decoupling internal power supply

The IC has two power terminals. The main terminal (pin 17) supplies the output stages, the sync separator and the divider circuit. The specially decoupled terminal (pin 14) supplies the horizontal oscillator. The decoupling capacitor should be 22 μF.

### 15. Flyback input pulse

This pulse is required for the second phase control loop and for generating the horizontal blanking pulse in the sandcastle output. The input current must be at least 0,2 mA and not exceed 3 mA.

### 16. RC-network horizontal oscillator

Stable components should be chosen for good frequency stability. For adjusting the frequency a part of the total resistance must be variable. This part must be as small as possible, because of poor stability of variable carbon resistors. The oscillator can be adjusted when pins 8 and 13 are short circuited (see Fig. 3).

### 17. Positive supply

The supply voltage may vary between 10,5 and 13,2 V. The current-draw is typ. 70 mA and the range is 50 to 85 mA.

### 18. Video transmitter identification output

This is an emitter-follower output which will be inactive (high-impedance) when the level at pin 1 is > 4 V (video transmitter detected). The output will be active high when the level at pin 1 is < 1,7 V (no video transmitter detected). This feature can be used for search-tuning and sound-muting.

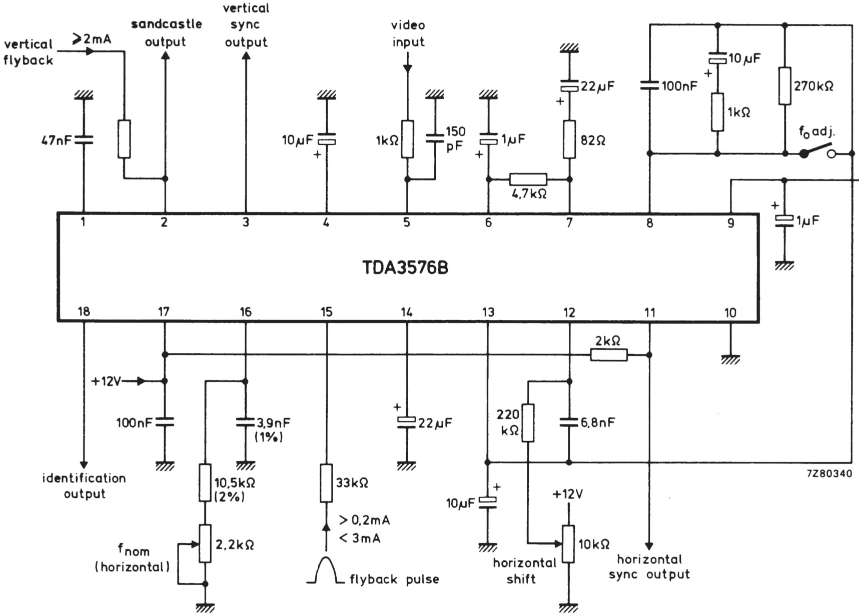

vertical flyback
>2mA
sandcastle output
vertical sync output
video input
+12V
VCR
47nF
10μF
1kΩ
150 pF
1μF
22μF
82Ω
4,7kΩ
100nF
10μF
1kΩ
270kΩ
f0 adj.
10kΩ or 1kΩ
1μF
TDA3576B
1
2
3
4
5
6
7
8
9
18
17
16
15
14
13
12
11
10
2kΩ
+12V
100nF
3,9nF (1%)
22μF
220 kΩ
6,8nF
identification output
10,5kΩ (2%)
33kΩ
10μF
+12V
fnom (horizontal)
2,2kΩ
> 0,2mA
< 3mA
flyback pulse
horizontal shift
10kΩ
horizontal sync output
7Z80340

Fig. 3 Application circuit diagram.

DEVELOPMENT SAMPLE DATA

# SECAM PROCESSOR CIRCUIT

The TDA3590 is a processor circuit that converts SECAM signals into sequential phase modulated signals. This circuit is intended to be used in combination with the TDA3560, TDA3561 or TDA3562 of which the 8,8 MHz oscillator signal is used as the carrier for the modulator. The TDA3590 incorporates the following functions:

- Limiter/amplifier for the chrominance signal
- SECAM demodulator
- Clamp circuit and de-emphasis for the colour difference signals
- Modulator to convert the colour difference signals in sequential phase modulated signals
- Identification circuit which can be used as:
  - — horizontal identification
  - — vertical identification
  - — combination of hor./vert. identification
- Divider circuit which generates the 4,4 MHz carrier signal from the 8,8 MHz signal of the PAL-modulator oscillator
- Sandcastle pulse detector
- SECAM switch and PAL matrix
- Video amplifier

## QUICK REFERENCE DATA

| | | | | |
|---|---|---|---|---|
| Supply voltage | $V_P = V_{17\text{-}2}$ | typ. | 12 | V |
| Supply current | $I_P = I_{17}$ | typ. | 90 | mA |
| **Chrominance amplifier and demodulator** | | | | |
| Input signal PAL (peak-to-peak value) | $V_{4\text{-}2(p\text{-}p)}$ | typ. | 550 | mV |
| Input signal SECAM (peak-to-peak value) | $V_{4\text{-}2(p\text{-}p)}$ | typ. | 100 | mV |
| Output signal PAL (peak-to-peak value) | $V_{8\text{-}2(p\text{-}p)}$ | typ. | 400 | mV |
| Output signal SECAM (peak-to-peak value) | $V_{8\text{-}2(p\text{-}p)}$ | typ. | 1100 | mV |
| **Identification** | | | | |
| Input voltage for horizontal identification | $V_{5\text{-}2}$ | | 0 to 8 | V |
| Input voltage for vertical identification | $V_{5\text{-}2}$ | | 10,5 to 12 | V |
| Voltage at pin 6 for PAL | $V_{6\text{-}2}$ | typ. | 10,3 | V |
| Voltage at pin 6 for SECAM | $V_{6\text{-}2}$ | typ. | 7 | V |
| **Sandcastle pulse detector** | | | | |
| Vertical blanking level | $V_{19\text{-}2}$ | typ. | 1,5 | V |
| Horizontal blanking level | $V_{19\text{-}2}$ | typ. | 3,5 | V |
| Burst gating level | $V_{19\text{-}2}$ | typ. | 7,0 | V |
| **Luminance amplifier** | | | | |
| Luminance input signal (peak-to-peak value) | $V_{16\text{-}2(p\text{-}p)}$ | typ. | 0,5 | V |
| Luminance output signal (peak-to-peak value) | $V_{15\text{-}2(p\text{-}p)}$ | typ. | 1 | V |
| **PAL-matrix and SECAM-switch** | | | | |
| Burst signal amplitude (peak-to-peak value) | $V_{11;12\text{-}2(p\text{-}p)}$ | typ. | 60 | mV |
| Amplification for PAL | | typ. | 0 | dB |
| Amplification for SECAM | | typ. | 6 | dB |

**PACKAGE OUTLINE** 24-lead DIL; plastic with heat spreader (SOT-101B).

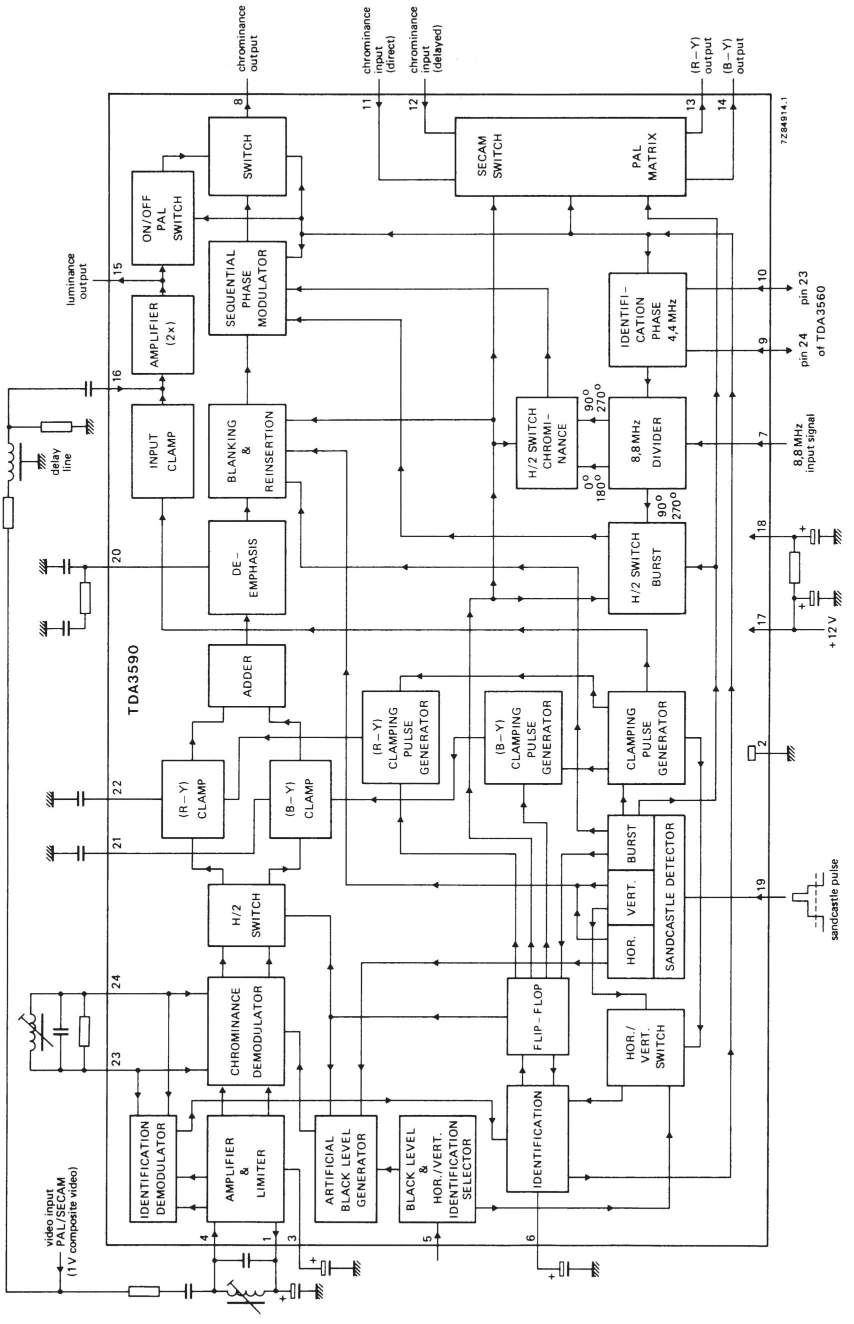

TDA3590
7Z84914.1
chrominance output
8
SWITCH
ON/OFF PAL SWITCH
luminance output
15
AMPLIFIER (2x)
16
INPUT CLAMP
delay line
SEQUENTIAL PHASE MODULATOR
BLANKING & REINSERTION
DE-EMPHASIS
20
ADDER
(R−Y) CLAMP
(B−Y) CLAMP
22
21
H/2 SWITCH
24
23
CHROMINANCE DEMODULATOR
IDENTIFICATION DEMODULATOR
AMPLIFIER & LIMITER
ARTIFICIAL BLACK LEVEL GENERATOR
BLACK LEVEL & HOR./VERT. IDENTIFICATION SELECTOR
IDENTIFICATION
FLIP-FLOP
HOR./VERT. SWITCH
(R−Y) CLAMPING PULSE GENERATOR
(B−Y) CLAMPING PULSE GENERATOR
CLAMPING PULSE GENERATOR
BURST
VERT.
HOR.
SANDCASTLE DETECTOR
19
sandcastle pulse
2
video input PAL/SECAM (1 V composite video)
4
1
3
5
6
chrominance input (direct)
11
chrominance input (delayed)
12
SECAM SWITCH
PAL MATRIX
13
(R−Y) output
14
(B−Y) output
IDENTIFICATION PHASE 4,4 MHz
10
9
pin 23
pin 24
of TDA3560
H/2 SWITCH CHROMINANCE
90°
270°
0°
180°
8,8 MHz DIVIDER
7
8,8 MHz input signal
H/2 SWITCH BURST
18
17
+12 V
+

Fig. 1 Block diagram.

## GENERAL DESCRIPTION

### Demodulation

The TDA3590 comprises a chrominance and an identification demodulator, both using the same reference tuned circuit. The identification circuit automatically detects whether the incoming signal at pin 4 is SECAM or not (NTSC, PAL or black-and-white). When PAL signals are received, they are diverted via pin 16 to the chrominance output (pin 8).

The delay line connected to pin 16 delays the PAL luminance signal. The SECAM signal has the same delay in the processor circuitry. When SECAM signals are received, the PAL signal path is switched off. Then, the SECAM signal is applied to a limiter/amplifier (via a bandpass filter with a bell-shaped response, after which it is demodulated). The (R—Y) and (B—Y) signals are available sequentially, so only one demodulator is necessary. After demodulation the signals are applied to an H/2 switch, which separates the two colour difference signals. Now the signals are applied to the (R—Y) and (B—Y) clamp circuits, where the black levels are clamped to the same d.c. level. The optimum black level can be obtained at the end of the horizontal burst, so the timing of the (R—Y) and (B—Y) clamp is determined by an internally generated pulse of 800 ns, which starts just after the sandcastle burst gate pulse. The two signals are added again after clamping. The signal is applied to the modulator via a de-emphasis, blanking and reinsertion circuit.

If $V_{5\text{-}2} > 2$ V, artificial black levels are inserted during the horizontal blanking period. The clamp circuits then react upon these levels instead of the demodulated burst signals (necessary in case there are no horizontal burst signals available). The inserted signals may not be identical to the detected signals, because of circuitry spread. This can be corrected by detuning the demodulator tuned circuit.

### Modulation

The (R—Y)/(B—Y) ratio is 1,78 at the de-emphasis output (pin 20). The demodulated (R—Y) and (B—Y) signals have a positive phase position for a magenta colour.

A burst signal is added to the demodulated SECAM signal at the input of the modulator. A sequential modulated chrominance signal is present at the modulator output. The modulation carriers of the (R—Y) and (B—Y) signals are 90° out of phase. The burst is modulated in the + (R—Y) direction and is only present during an (R—Y) line. The modulated (R—Y) component has the same phase position as the (R—Y) burst for a magenta colour.

### Identification

The identification circuit compares the voltage difference, which is obtained after demodulation, with the phase of the flip-flop. For horizontal identification this comparison occurs during the internally generated 800 ns pulse. Only SECAM signals have a voltage difference from line to line during comparison. If the phase relationship between both the signals is wrong, the flip-flop will get a reset with an extra input pulse.

The identification detector information is also used for colour killing and for switching to PAL, if required.

The identification (as above) occurs when the horizontal identification system is active. When the vertical identification system is switched on (pin 5), the system only compares the demodulator output voltage during line scanning of the vertical blanking. The further operation is identical to the horizontal identification.

### Sandcastle pulse detector

The sandcastle pulse detector is able to handle a 3-level sandcastle pulse. It detects the various blanking and gating pulses and it generates the correct drive pulses for the clamping circuits.

## GENERAL DESCRIPTION (continued)

### Carrier generation

The carrier signal for the PAL modulator is obtained from the 8,8 MHz oscillator signal of the TDA3560. The frequency of this signal is divided-by-two to obtain 90° shift. These two signals are applied to the modulator. There is a possibility that the two dividers in the TDA3560 (pins 23 and 24) and the TDA3590 are out-of-phase. This can be corrected by connecting pins 9 and 10 of the TDA3590 to pins 24 and 23 of the TDA3560 respectively. At incorrect phase, the TDA3590 divider is reset and correct phase is obtained.

### PAL-matrix and SECAM-switch

The colour difference signals are transmitted sequentially in the SECAM-system, so the modulated PAL-signal from the TDA3590 is also sequential. The consequences are:

- The two colour difference signals are mixed again in the delay line matrix circuit, so that both demodulators get a combination of an (R—Y) and (B—Y) signal. The phase position of the reference carrier must be very accurate for obtaining a proper demodulated signal, otherwise colour errors will occur (e.g. in the NTSC-system).
- Two different signals are added or subtracted in the matrix circuit, which results in an amplitude that has half the amplitude when compared with a normal PAL signal.

  Increase of the chrominance signal in the TDA3590 results in an overdrive of the chrominance amplifier of the TDA3560.

These effects can be avoided by the matrix and switching circuit which is included in the TDA3590. The direct and delayed (from the PAL delay line) signals are applied to the processor where they are matrixed (for PAL) or switched (for SECAM). In the latter condition, the gain of the circuit is twice as high as for the normal PAL reception. The phase accuracy is not critical in this situation, because the two colour difference signals are not mixed.

For SECAM, the (B—Y) output of the SECAM-switch will be a signal without burst. The (R—Y) output of the SECAM-switch only has a burst during the +(R—Y) line. This burst is modulated in the +(R—Y) direction.

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | |
|---|---|---|---|
| Supply voltage | $V_P = V_{17\text{-}2}$ | max. | 13,2 V |
| Total power dissipation | $P_{tot}$ | max. | 1,7 W |
| Storage temperature range | $T_{stg}$ | | −25 to + 150 °C |
| Operating ambient temperature range | $T_{amb}$ | | −25 to + 65 °C |

## CHARACTERISTICS

$V_P$ = 12 V; $T_{amb}$ = 25 °C; unless otherwise specified

| | | | |
|---|---|---|---|
| Supply voltage | $V_P = V_{17\text{-}2}$ | typ.<br> | 12 V<br>10,8 to 13,2 V |
| Supply current | $I_P = I_{17}$ | typ. | 90 mA |
| Total power dissipation | $P_{tot}$ | typ. | 1,1 W |

**Chrominance amplifier and demodulator**

| | | | |
|---|---|---|---|
| Input signal PAL (peak-to-peak value) | $V_{4\text{-}2(p\text{-}p)}$ | typ.<br> | 550 mV<br>55 to 1100 mV |
| Input signal SECAM (peak-to-peak value) | $V_{4\text{-}2(p\text{-}p)}$ | typ.<br> | 100 mV<br>15 to 300 mV |
| Input current | $I_4$ | typ. | 5 μA |
| Input capacitance | $C_{4\text{-}2}$ | < | 5 pF |
| (R—Y)/(B—Y) ratio before modulation (pin 20) | | typ. | 1,78 |
| Relative deviation of the black level of the colour difference signals before modulation | see note 1 | | |
| Output signal PAL (peak-to-peak value) | $V_{8\text{-}2(p\text{-}p)}$ | typ. | 400 mV |
| Output signal SECAM (peak-to-peak value) | $V_{8\text{-}2(p\text{-}p)}$ | typ. | 1100 mV |
| Output impedance | $\lvert Z_{8\text{-}2}\rvert$ | typ. | 50 Ω |
| Input voltage for clamping on the back-porch of the colour difference signals | $V_{5\text{-}2}$ | < | 0,5 V |
| Input voltage for insertion of the artificial black level after demodulation | $V_{5\text{-}2}$ | > | 2 V |
| Input resistance between pins 23 and 24 | $R_{23\text{-}24}$ | typ. | 4 kΩ |
| Input capacitance between pins 23 and 24 | $C_{23\text{-}24}$ | typ. | 17 pF |
| Input current at pin 5<br>$V_{5\text{-}2}$ = 12 V | $I_5$ | < | 25 μA |
| Output current at pin 5<br>$V_{5\text{-}2}$ = 0 V | $-I_5$ | < | 25 μA |

**CHARACTERISTICS** (continued)

**Identification**

| | | | | |
|---|---|---|---|---|
| Input voltage for horizontal identification | $V_{5\text{-}2}$ | | 0 to 8 | V |
| Input voltage for vertical identification | $V_{5\text{-}2}$ | | 10,5 to 12 | V |
| Voltage at pin 6 for PAL | $V_{6\text{-}2}$ | typ. | 10,3 | V |
| Voltage at pin 6 for SECAM | $V_{6\text{-}2}$ | typ. | 7 | V |
| Identification 'on' for SECAM | $V_{6\text{-}2}$ | typ. | 10,7 | V |
| Colour 'off' at SECAM | $V_{6\text{-}2}$ | typ. | 9,20 | V |
| Colour 'on' at SECAM | $V_{6\text{-}2}$ | typ. | 9,05 | V |
| Voltage at pins 9 and 10 for SECAM | $V_{9\text{-}2}$; $V_{10\text{-}2}$ | typ. | 10,5 | V |
| Voltage between pins 9 and 10 for SECAM | $V_{9\text{-}10}$ | < | 3 | mV |
| Permissible voltage at pins 9 and 10 for PAL | $V_{9\text{-}2}$; $V_{10\text{-}2}$ | | 8,2 to 10,3 | V |

**Sandcastle pulse detector and clamping pulse generator**

| | | | | |
|---|---|---|---|---|
| Voltage level at which the vertical blanking pulse is separated | $V_{19\text{-}2}$ | typ. | 1,5<br>1 to 2 | V<br>V |
| required pulse amplitude | $V_{19\text{-}2}$ | | 2 to 3 | V |
| Voltage level at which the horizontal blanking pulse is separated | $V_{19\text{-}2}$ | typ. | 3,5<br>3 to 4 | V<br>V |
| required pulse amplitude | $V_{9\text{-}12}$ | | 4 to 6,5 | V |
| Voltage level at which the burst gating pulse is separated | $V_{19\text{-}2}$ | typ. | 7<br>6,5 to 7,5 | V<br>V |
| required pulse amplitude | $V_{19\text{-}2}$ | > | 7,5 | V |
| Internal clamping pulse duration (see note 2) | $t_p$ | typ. | 0,8 | µs |
| Input current at $V_{19\text{-}2} = 7$ V | $I_2$ | typ. | 10 | µA |

**Carrier generator** (see note 3)

| | | | | |
|---|---|---|---|---|
| Input signal from TDA3560 (peak-to-peak value) | $V_{7\text{-}2(p\text{-}p)}$ | > | 150 | mV |
| Input resistance | $R_{7\text{-}2}$ | typ. | 4,4 | kΩ |

**Luminance amplifier**

| | | | | |
|---|---|---|---|---|
| Input signal (peak-to-peak value) | $V_{16\text{-}2(p\text{-}p)}$ | typ. | 0,5 | V |
| Output signal (peak-to-peak value) at $V_{16\text{-}2(p\text{-}p)} = 0,5$ V | $V_{15\text{-}2(p\text{-}p)}$ | typ. | 1 | V |
| Input current | $I_{16}$ | typ. | 0,15 | µA |
| Output impedance (load: $R_{15\text{-}2} = 2$ kΩ) | $\lvert Z_{15\text{-}2} \rvert$ | typ. | 20 | Ω |
| Frequency response (–3 dB) | f | > | 8 | MHz |

**PAL-matrix and SECAM-switch**

| | | | |
|---|---|---|---|
| Burst signal amplitude (peak-to-peak value) | $V_{11;12(p\text{-}p)}$ | typ. | 60 mV |
| Input impedance | $\lvert Z_{11;12\text{-}2}\rvert$ | typ. | 2 kΩ |
| Amplification for PAL | | typ. | 0 dB |
| Amplification for SECAM | | typ. | 6 dB |
| Difference in amplification from the inputs to one output for PAL | | < | 5 % |
| Phase error from line-to-line in the (R−Y) output for zero-error in the (B−Y) output for PAL | | < | 2,5° |
| Output impedance | $\lvert Z_{13;14\text{-}2}\rvert$ | typ. | 40 Ω |

**Notes to the characteristics**

1. When an artificial black level is inserted after demodulation, the resulting black level deviation depends on the adjustment of the demodulator tuned circuit. It is therefore possible to obtain a value of zero per cent.
2. This pulse starts directly after the burst clamping pulse.
3. The phase delay between the oscillator output of the TDA3560 and the input of the TDA3590 (pin 7) must be adjusted such, that the burst amplitude at pin 28 of the TDA3560 is minimum.

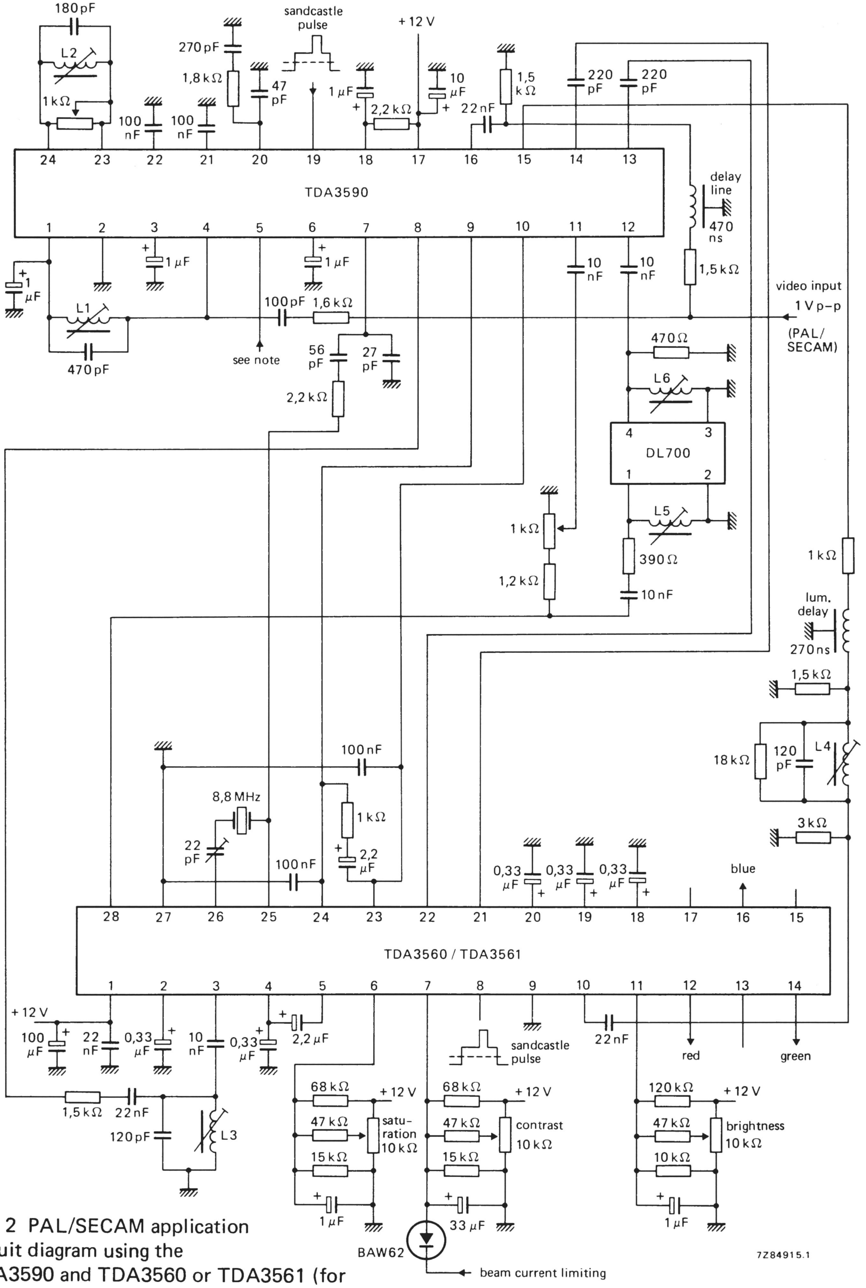

180 pF
L2
1 kΩ
270 pF
1,8 kΩ
100 nF
100 nF
47 pF
sandcastle pulse
+12 V
1 µF
2,2 kΩ
10 µF
22 nF
1,5 kΩ
220 pF
220 pF
24
23
22
21
20
19
18
17
16
15
14
13
TDA3590
1
2
3
4
5
6
7
8
9
10
11
12
delay line
470 ns
1 µF
1 µF
1 µF
10 nF
10 nF
1,5 kΩ
video input
1 V p-p
(PAL/SECAM)
L1
470 pF
100 pF
1,6 kΩ
see note
56 pF
27 pF
2,2 kΩ
470 Ω
L6
4
3
DL700
1
2
L5
1 kΩ
1,2 kΩ
390 Ω
10 nF
1 kΩ
lum. delay
270 ns
1,5 kΩ
18 kΩ
120 pF
L4
3 kΩ
100 nF
8,8 MHz
22 pF
1 kΩ
2,2 µF
100 nF
0,33 µF
0,33 µF
0,33 µF
blue
28
27
26
25
24
23
22
21
20
19
18
17
16
15
TDA3560 / TDA3561
1
2
3
4
5
6
7
8
9
10
11
12
13
14
+12 V
100 µF
22 nF
0,33 µF
10 nF
0,33 µF
2,2 µF
sandcastle pulse
22 nF
red
green
1,5 kΩ
22 nF
120 pF
L3
68 kΩ
+12 V
47 kΩ
satu-ration 10 kΩ
15 kΩ
1 µF
68 kΩ
+12 V
47 kΩ
contrast 10 kΩ
15 kΩ
33 µF
BAW62
beam current limiting
120 kΩ
+12 V
47 kΩ
brightness 10 kΩ
10 kΩ
1 µF
7Z84915.1

Fig. 2 PAL/SECAM application circuit diagram using the TDA3590 and TDA3560 or TDA3561 (for a combination with the TDA3562 see Fig. 3). For note to pin 5 of the TDA3590 see next page.

**Note to Fig. 2**

$V_{5\text{-}2} < 0{,}5$ V : horizontal identification and black level clamping.
$V_{5\text{-}2} > 10{,}5$ V : vertical identification and artificial black level.
$V_{5\text{-}2} = 5$ to 7 V: horizontal identification and artificial black level.

## PINNING

1. Limiter feedback to pin 4.
2. Ground.
3. Limiter feedback.
4. Input limiter; PAL identification input; SECAM chrominance/identification input.
5. Via a d.c. voltage to this pin, the SECAM identification system can be chosen.
   At $V_{5\text{-}2} < 8$ V the processor is preset for horizontal identification.
   At $V_{5\text{-}2} > 10{,}5$ V the processor is preset for vertical identification.
   At $V_{5\text{-}2} < 0{,}5$ V the demodulated black level of the SECAM horizontal burst will be used as black level reference.
   At $V_{5\text{-}2} > 2$ V the demodulated chroma signal will have an artificial black level during the SECAM horizontal burst.
6. Store capacitor of PAL/SECAM identification circuit;
   horizontal identification: 100 nF
   vertical identification: 1 μF
7. Input of 8,8 MHz oscillator signal.
8. PAL/processed SECAM signal output (chrominance output).
9. Identification input of 8,8 MHz divider (to pin 24 of TDA3560).
10. Identification input of 8,8 MHz divider (to pin 23 of TDA3560).
11. Direct chrominance input of PAL matrix/processed SECAM switch.
12. Delayed chrominance input of PAL matrix/processed SECAM switch.
13. PAL/processed SECAM (R−Y) h.f. output.
14. PAL/processed SECAM (B−Y) h.f. output.
15. Luminance output.
16. Luminance/PAL input.
17. Positive supply voltage (+ 12 V).
18. Decoupled positive supply voltage.
19. Three-level sandcastle pulse input. It detects the various blanking and gating pulses and it generates the correct drive pulses for the clamping circuits.
20. De-emphasis is performed at this pin with a 1,8 kΩ resistor and a 270 pF capacitor. To avoid moiré patterns on the screen, additional filtering of the demodulator double-frequency products is obtained by a 47 pF decoupling capacitor.
21. Store capacitor (B−Y) clamp.
22. Store capacitor (R−Y) clamp.
23. Demodulator reference tuned circuit.
24. Demodulator reference tuned circuit. The demodulator reference circuit has to be tuned to a nominal frequency of about 4,33 MHz. The quality factor of the tuned circuit must be nominal 2,45.

## APPLICATION INFORMATION (see Fig. 2)

**The function is described against the corresponding pin number**

### Pin 4. Chrominance input

The SECAM input signal is typically 100 mV peak to peak, while the PAL input signal is about 550 mV peak to peak. This corresponds to a PAL/SECAM ratio of 5,5 (based on 75% saturated colour bar signals). The input signal, which should be free from any sound modulation, is applied single-ended to pin 4 via a filter which provides the required bell-shaped bandpass for SECAM signals. D.C. biasing takes place via coil L1, which has an unloaded quality factor between 80 and 100.

### Pin 8. Chrominance output

During PAL reception, this output is internally connected to the luminance stage, therefore a composite video signal of 0,9 V peak to peak (typical) is present at the output. During SECAM reception, the chrominance output stage is connected to the modulator. The sequentially modulated (R—Y) and (B—Y) signals are then available at the output (amplitudes of typically 1100 mV peak to peak). These signals are applied via a chrominance bandpass filter to the chrominance a.c.c. amplifier in the TDA3560.

### Pin 6. System identification

A 1 $\mu$F capacitor is connected to this pin. During PAL reception, the typical voltage at pin 6 is 10,3 V. The chrominance output stage is then internally connected to the luminance stage and the PAL matrix circuit is activated for normal matrixing of the PAL signals. During SECAM reception, the voltage at pin 6 is about 7 V (typical). The chrominance output stage is connected to the modulator and the SECAM switch is enabled. During noisy SECAM signals, the voltage at pin 6 increases and colour killing/unkilling occurs around 9,20 V and 9,05 V respectively.

### Pin 5. Horizontal/vertical identification

Horizontal or vertical identification can be selected depending on the externally applied voltage at pin 5. When the d.c. level on pin 5 changes with time (pulse information), a combination of horizontal and vertical identification is possible.

*Horizontal identification*

If the voltage at pin 5 is $< 2$ V, horizontal identification occurs with black level clamping. This clamping occurs on the back-porch of the demodulated colour difference signals. If artificial black level insertion is required, the voltage at pin 5 should be $< 8$ V.

*Vertical identification*

If the voltage at pin 5 is $> 10{,}5$ V, vertical identification occurs, i.e. identification on 9 lines in the vertical blanking period. In this mode, the black level is artificially inserted after demodulation.

### Pin 19. Sandcastle pulse

A 3-level sandcastle pulse is required and this can be directly coupled to the sandcastle pulse detector. Horizontal blanking, vertical blanking and burst clamping pulses are separated by the IC. A clamping pulse of 800 ns is generated internally just after the burst gating pulse. The input current is typically 10 $\mu$A at an input signal of 7 V.

**Pins 16 and 15. Luminance input/output**

The input signal at pin 16 should be typically 0,5 V peak to peak. The input impedance is relatively high, so a 22 nF coupling capacitor can be applied. This luminance signal is internally clamped and after a 2 times amplification available at pin 15.

During SECAM reception, the luminance signal is delayed by about 470 ns in a luminance delay line. The chrominance and luminance signals are then correctly timed at the output of the TDA3590.

During PAL reception, the composite video signal passes through this delay line and, after amplification, is available at pins 8 and 15. The nominal amplitude of the signals is 900 mV peak to peak in both cases.

**Pins 11, 12, 13 and 14. SECAM switch and PAL matrix**

During PAL reception, the system identification 'enables' the PAL matrix circuitry. An a.c.c. composite chroma signal (from pin 28 TDA3560) is coupled via the glass delay line to pin 12 of the TDA3590. A direct signal is applied to pin 11 of the TDA3590 via a resistor network. Active matrixing takes place in the IC and consequently (R–Y) and (B–Y) signals are available at pins 13 and 14 respectively. These signals are applied to the TDA3560 demodulators (pins 22 and 21 respectively).

During SECAM reception, the PAL matrix circuitry is 'disabled' and the SECAM switch is 'enabled'. A sequentially modulated (R–Y) and (B–Y) signal is available at pin 28 of the TDA3560. Direct and delayed signals are applied to pins 11 and 12 of the TDA3590, and via the SECAM switch the (R–Y) and (B–Y) signals are applied to their respective demodulator in the TDA3560.

**Pins 17 and 18. Supply voltage (+ 12 V)**

Correct operation is ensured within the supply range of 10,8 V to 13,2 V, and the typical power dissipation of the IC is 1,1 W at 12 V.

Pins 17 and 18 are separated by an external RC filter. Pin 18 is the supply for biasing several current-sinks in the IC and for all the output stages.

This supply voltage separation minimizes crosstalk via the supply lines between various parts of the circuitry. The capacitor at pin 18 must be small ($\approx 1\ \mu F$) so that, if pin 17 is short-circuited to ground, the collector-base junction of a transistor in the IC, through which the discharge current flows, is not damaged.

**Pin 20. De-emphasis**

De-emphasis is performed at this pin with a 1,8 kΩ and a 270 pF capacitor. To avoid moiré patterns on the screen, additional filtering of the 8,8 MHz signal is obtained by a 47 pF decoupling capacitor.

**Pins 21 and 22. Clamping of (R–Y) and (B–Y) signals**

After demodulation, the sequential (R–Y) and (B–Y) signals are separated by means of an H/2 switch and passed-on to their respective clamping circuits, where they are clamped to the same d.c. level. The value of each clamping capacitor should be 100 nF and they may, if desired, be increased to 470 nF.

**Pins 23 and 24. Demodulator reference tuned circuit**

The SECAM signal is applied to the demodulator via the 'bell-filter' and limiter/amplifier. Only one demodulator is used because of the sequential nature of the signal. The reference signal, obtained from the tank circuit, is applied to pins 23 and 24. At $V_{5\text{-}2} > 2$ V, the tuning and damping of the tank circuit should be done in such a way that a minimum modulator output voltage at pin 8 of the TDA3590 is obtained (the (R–Y) and (B–Y) information in the SECAM video signal is switched off). Therefore, any deviations between the black levels (when clamping on the back-porch and when an artificial black level is filled in) can be made minimum.

## APPLICATION INFORMATION (continued)

### Pin 7. Carrier generation

An 8,8 MHz signal from pin 25 of the TDA3560 is applied via pin 7 to the divider circuit in the TDA3590. Two 4,4 MHz signals are obtained with a phase shift of 90° with respect to each other. These signals are applied to the modulator via an H/2 switch. The phase delay of the 8,8 MHz input signal must be adjusted such that the burst amplitude of the chrominance signal at pin 28 (TDA3560) has its minimum amplitude. Under this condition, the burst generated by the TDA3590 is in phase with the (R−Y) reference signal for the demodulator in the TDA3560. Since the a.c.c. of the TDA3560 operates in the + (R−Y) direction, the burst signal at pin 28 of the TDA3560 will have its minimum amplitude.

### Pins 9 and 10. Divider resetting

The output of the burst phase detector of the TDA3560 is connected to pins 9 and 10. At SECAM reception, the differential a.c. current information, obtained from the burst detector (TDA3560), is applied to pins 9 and 10 (TDA3590). This gives information about the phase relationship between the two 4,4 MHz dividers in both ICs. The TDA3590 now generates a minimum relative voltage between pins 9 and 10 at an absolute voltage level of 10,6 V. The result is that the oscillator control function of the TDA3560 is overruled, and the oscillator is set to 2 x 4,43 MHz.

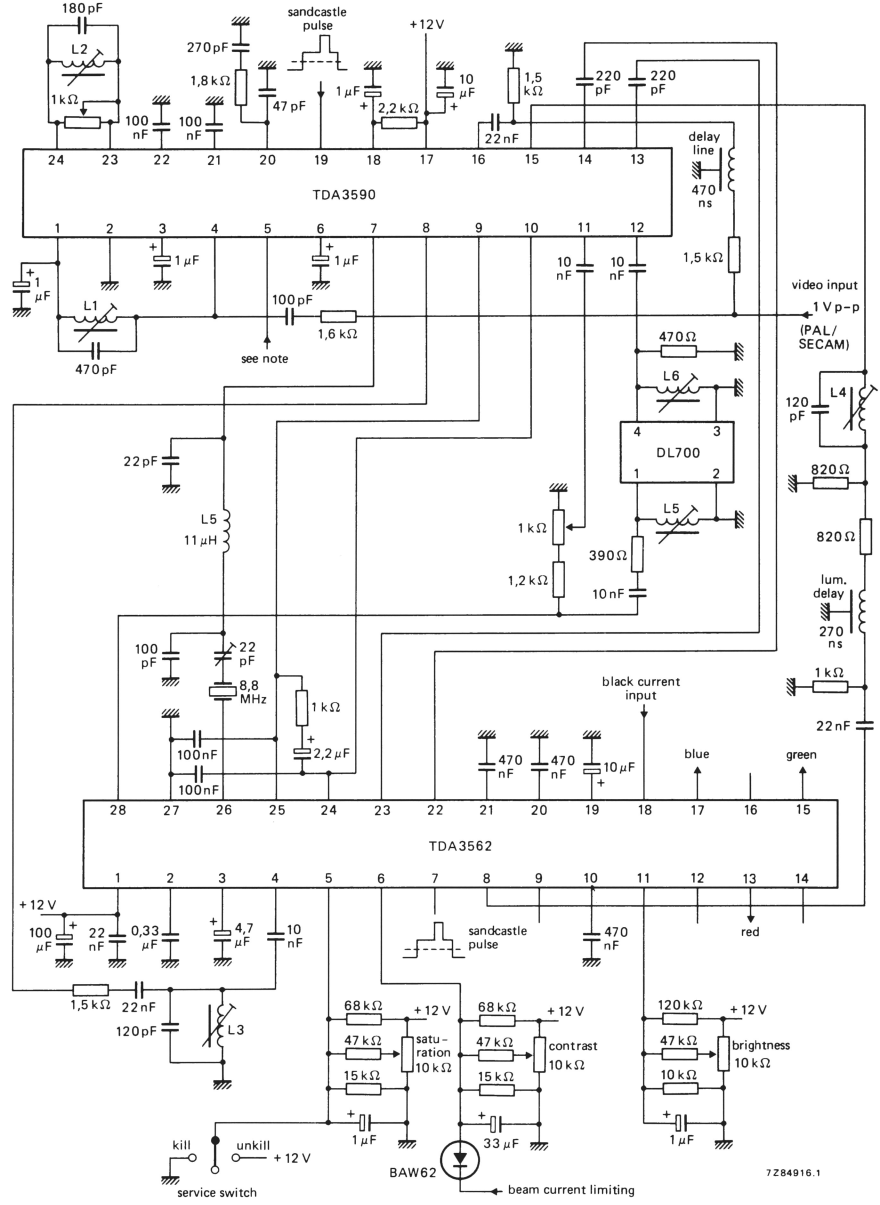

180 pF
L2
1 kΩ
100 nF
100 nF
270 pF
1,8 kΩ
47 pF
sandcastle pulse
1 μF
2,2 kΩ
+12 V
10 μF
22 nF
1,5 kΩ
220 pF
220 pF
delay line
470 ns
24
23
22
21
20
19
18
17
16
15
14
13
TDA3590
1
2
3
4
5
6
7
8
9
10
11
12
1 μF
1 μF
1 μF
L1
470 pF
100 pF
1,6 kΩ
see note
10 nF
10 nF
1,5 kΩ
video input
1 V p-p
(PAL/ SECAM)
470 Ω
L6
DL700
4
3
1
2
L5
L4
120 pF
820 Ω
820 Ω
22 pF
L5
11 μH
1 kΩ
1,2 kΩ
390 Ω
10 nF
lum. delay
270 ns
1 kΩ
22 nF
100 pF
22 pF
8,8 MHz
1 kΩ
2,2 μF
100 nF
100 nF
470 nF
470 nF
10 μF
black current input
blue
green
28
27
26
25
24
23
22
21
20
19
18
17
16
15
TDA3562
1
2
3
4
5
6
7
8
9
10
11
12
13
14
+12 V
100 μF
22 nF
0,33 μF
4,7 μF
10 nF
sandcastle pulse
470 nF
red
1,5 kΩ
22 nF
120 pF
L3
68 kΩ
+12 V
47 kΩ
satu- ration 10 kΩ
15 kΩ
1 μF
68 kΩ
+12 V
47 kΩ
contrast 10 kΩ
15 kΩ
33 μF
120 kΩ
+12 V
47 kΩ
brightness 10 kΩ
10 kΩ
1 μF
kill
unkill
+12 V
service switch
BAW62
beam current limiting
7Z84916.1

Fig. 3 PAL/SECAM application circuit diagram using the TDA3590 and TDA3562.

Note to pin 5 TDA3590: $V_{5\text{-}2} < 2$ V; horizontal identification and black level clamping.

$V_{5\text{-}2} > 10{,}5$ V; vertical identification and artificial black level.

$V_{5\text{-}2} = 5$ to 7 V; horizontal identification and artificial black level.

# SECAM PROCESSOR CIRCUIT

## GENERAL DESCRIPTION

The TDA3590A is pin compatible with the TDA3590. Additional improvements have been made and are described below.

### Luminance amplifier

The luminance amplifier is modified (between pins 16 and 15). The amplifier can now handle input signal levels at pin 16 of up to 1,2 V peak to peak (2,7 V peak to peak −7 dB). The gain of the amplifier is typical 7 dB.

### Horizontal identification with black level re-insertion

The TDA3590A is automatically set to internal horizontal identification with black level re-insertion by means of a voltage divider which presets pin 5 to 6 V.

### Internal current sources at pins 9 and 10

Pins 9 and 10 of the TDA3590A are provided with internal current sources, thus, the two 150 kΩ (1%) resistors currently used in the TDA3590 can be deleted.

### Coupling of system identification between the TDA3590A and TDA3560;61;62

If desired, the identification systems of the TDA3590A and TDA3560;61;62 can be coupled. Under this condition the system choice (PAL, NTSC or SECAM) will take place correctly.

### Spread of internal de-emphasis network

The external de-emphasis component values are changed to R = 1 kΩ and C = 470 pF. The spread of the internal de-emphasis network is now < 15%.

### Suppression of higher harmonics

In addition to the quasi-PAL chrominance signal, odd and even harmonics of the 4,4 MHz signal are also generated at the modulator, which appear at pin 8 of the TDA3590A. These harmonics are suppressed by internal on-chip filters.

### Black level clamping

If artificial black level re-insertion is desired, the burst gating pulse (duration is about 4 μs) is used for black level clamping.

### Burst chrominance ratio for a SECAM signal

For equal saturation of PAL and SECAM signals, a correction in the burst-chrominance ratio of the quasi-PAL signals is made.

### Cross-talk in the SECAM switch

The cross-talk between the (R-Y) and (B-Y) sequential signals in the SECAM switch is improved.

**A COMPLETE DATA SHEET IS AVAILABLE UPON REQUEST**

## GENERAL DESCRIPTION (continued)

### SECAM hysteresis

This hysteresis is improved and will be ± 2 dB when measured at the aerial input. The corresponding d.c. levels for switching the colour ON or OFF at pin 6 of the TDA3590A are:

colour ON: 9,1 V
colour OFF: 9,9 V

### L.F. PAL/SECAM interference

The internal circuit layout of the limiter and SECAM demodulator is improved which will give a better l.f. interference.

### Linearity of the (B-Y) signal

The linearity of the (B-Y) signal is improved and is as follows:

for (R-Y) at $\Delta f = \pm 280$ kHz: 95%
for (B-Y) at $\Delta f = \pm 230$ kHz: 92%

### Zero-point stability of demodulator

The zero-point stability of the demodulator for an input signal change between 10 and 300 mV peak to peak is typically 6 kHz.

### Re-inserted burst

The nominal duration of the re-inserted burst is 2,8 μs (4 μs for the TDA3590). On the one hand this is approximately the duration of the PAL burst and, on the other hand, in combination with the horizontal blanking pulse which is used as a keying pulse in the SECAM switch, it results in a minimum interference of the a.c.c. loop of the TDA3560/61/62 due to spikes etc.

### Phase shift in the PAL matrix

The phase shift between pins 11 and 12 with respect to pin 13 (for $0^{\circ}$ phase shift between pins 11 and 12 with respect to pin 14) is reduced from $2,5^{\circ}$ (nominal) to $1^{\circ}$ (nominal).

### Identification

The burst gate pulse is internally divided into two parts. The first part of 2,8 μs is used for burst timing. The second part of 1,2 μs is used for SECAM signal identification timing.

### Luminance clamping

The luminance clamping circuit is activated during the SECAM signal identification timing.

# SECAM PROCESSOR CIRCUIT

## GENERAL DESCRIPTION

The TDA3591 is a processor circuit that converts SECAM signals into sequential phase-modulated signals. This circuit is intended to be used in combination with the TDA3560, TDA3561A or TDA3562A of which the 8,8 MHz oscillator signal is used as the carrier for the modulator.

### Features

- Limiter/amplifier for the chrominance signal
- SECAM demodulator
- Clamp circuit and de-emphasis for the colour difference signals
- Modulator to convert the colour difference signals in sequential phase-modulated signals
- Identification circuit which can be used as:
  - horizontal identification
  - vertical identification
  - combination of hor./vert. identification
- Divider circuit which generates the 4,4 MHz carrier signal from the 8,8 MHz signal of the PAL-modulator oscillator
- Sandcastle pulse detector
- SECAM switch and PAL matrix
- Video amplifier

## QUICK REFERENCE DATA

| | | | | |
|---|---|---|---|---|
| Supply voltage | $V_P = V_{17\text{-}2}$ | typ. | 12 | V |
| Supply current | $I_P = I_{17}$ | typ. | 90 | mA |
| **Chrominance amplifier and demodulator** | | | | |
| Input signal PAL (peak-to-peak value) | $V_{4\text{-}2(p\text{-}p)}$ | typ. | 550 | mV |
| Input signal SECAM (peak-to-peak value) | $V_{4\text{-}2(p\text{-}p)}$ | | 15 to 300 | mV |
| Output signal PAL (peak-to-peak value) | $V_{8\text{-}2(p\text{-}p)}$ | typ. | 265 | mV |
| Output signal SECAM (peak-to-peak value) | $V_{8\text{-}2(p\text{-}p)}$ | typ. | 1300 | mV |
| **Identification** | | | | |
| Input voltage for horizontal identification | $V_{5\text{-}2}$ | | 0 to 8 | V |
| Input voltage for vertical identification | $V_{5\text{-}2}$ | | 10,5 to 12 | V |
| Voltage at pin 6 for PAL | $V_{6\text{-}2}$ | typ. | 10,1 | V |
| Voltage at pin 6 for SECAM | $V_{6\text{-}2}$ | typ. | 7 | V |
| **Sandcastle pulse detector** | | | | |
| Vertical blanking level | $V_{19\text{-}2}$ | typ. | 1,5 | V |
| Horizontal blanking level | $V_{19\text{-}2}$ | typ. | 3,5 | V |
| Burst gating level | $V_{19\text{-}2}$ | typ. | 7,2 | V |
| **Luminance amplifier** | | | | |
| Luminance input signal (peak-to-peak value) | $V_{16\text{-}2(p\text{-}p)}$ | typ. | 0,45 | V |
| Luminance amplifier gain at 4,4 MHz | | typ. | 5 | dB |
| **PAL-matrix and SECAM-switch** | | | | |
| Burst signal amplitude (peak-to-peak value) | $V_{11;12\text{-}2(p\text{-}p)}$ | typ. | 60 | mV |
| Amplification for PAL (pin 13) | | typ. | −0,3 | dB |
| Amplification for PAL (pin 14) | | typ. | −0,5 | dB |
| Amplification for SECAM | | typ. | 5,5 | dB |

**PACKAGE OUTLINE** 24-lead DIL; plastic with heat spreader (SOT-101B).

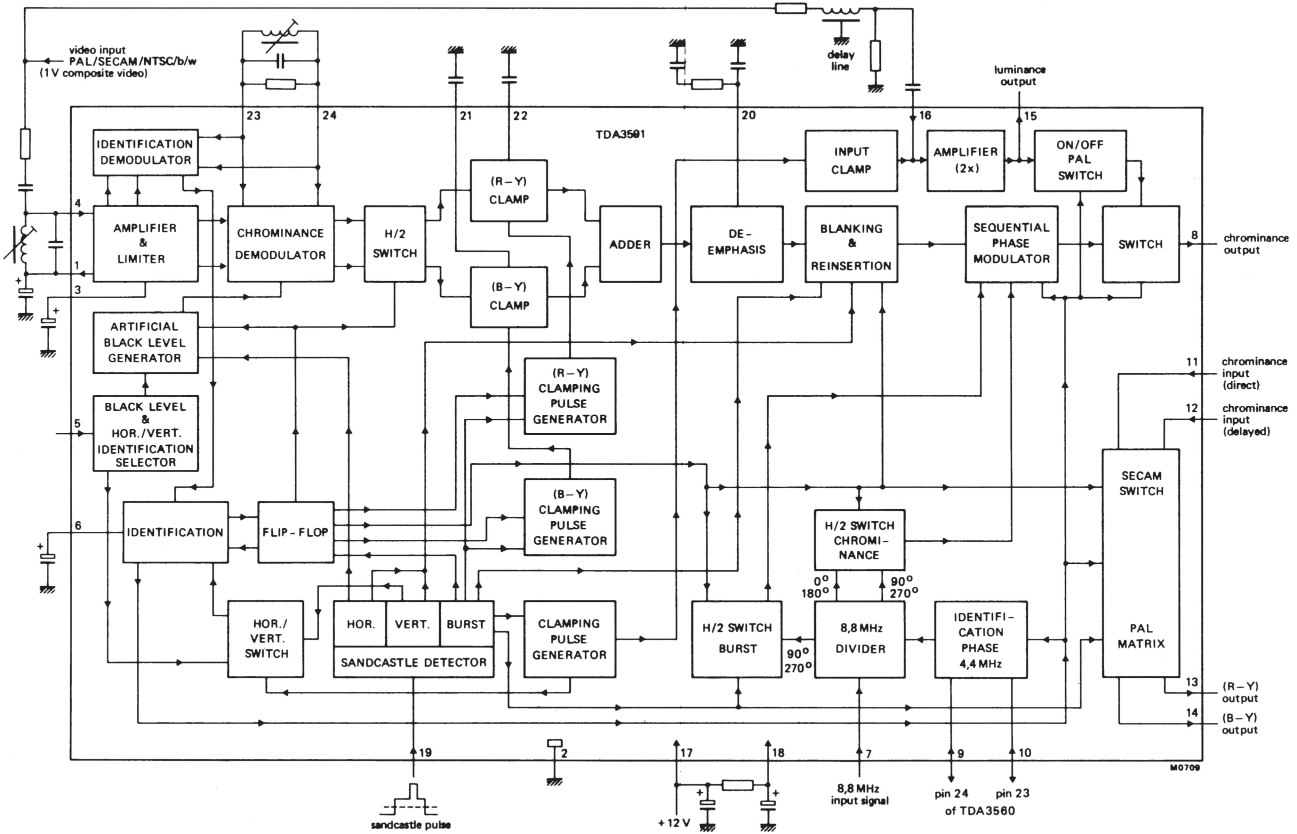

video input
PAL/SECAM/NTSC/b/w
(1V composite video)
delay line
luminance output
chrominance output
chrominance input (direct)
chrominance input (delayed)
(R–Y) output
(B–Y) output
TDA3591
IDENTIFICATION DEMODULATOR
AMPLIFIER & LIMITER
CHROMINANCE DEMODULATOR
H/2 SWITCH
(R–Y) CLAMP
(B–Y) CLAMP
ADDER
DE-EMPHASIS
INPUT CLAMP
BLANKING & REINSERTION
AMPLIFIER (2x)
ON/OFF PAL SWITCH
SEQUENTIAL PHASE MODULATOR
SWITCH
ARTIFICIAL BLACK LEVEL GENERATOR
BLACK LEVEL & HOR./VERT. IDENTIFICATION SELECTOR
(R–Y) CLAMPING PULSE GENERATOR
(B–Y) CLAMPING PULSE GENERATOR
CLAMPING PULSE GENERATOR
IDENTIFICATION
FLIP-FLOP
HOR./VERT. SWITCH
HOR.
VERT.
BURST
SANDCASTLE DETECTOR
H/2 SWITCH CHROMINANCE
H/2 SWITCH BURST
8,8 MHz DIVIDER
IDENTIFICATION PHASE 4,4 MHz
SECAM SWITCH
PAL MATRIX
0° 180°
90° 270°
90° 270°
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
sandcastle pulse
+12 V
8,8 MHz input signal
pin 24
pin 23
of TDA3560
M0709

Fig.1 Block diagram

## FUNCTIONAL DESCRIPTION

### Demodulation

The TDA3591 comprises a chrominance and an identification demodulator, both using the same reference tuned circuit. The identification circuit automatically detects whether the incoming signal at pin 4 is SECAM or not (NTSC, PAL or black-and-white). When PAL signals are received, they are diverted via pin 16 to the chrominance output (pin 8).

The delay line connected to pin 16 delays the PAL luminance signal by 450 ns. The SECAM signal has the same delay in the processor circuitry. When the SECAM signals are received, the PAL signal path is switched off. Then, the SECAM signal is applied to a limiter/amplifier (via a bandpass filter with a bell-shaped response) after which it is demodulated. The (R—Y) and (B—Y) signals are applied sequentially, so only one demodulator is necessary. After demodulation the signals are applied to an H/2 switch, which separates the two colour difference signals. Now the signals are applied to the (R—Y) and (B—Y) clamp circuits, where the black levels are clamped to the same d.c. level. The (R—Y) and (B—Y) clamps are only active during the burst gate period.

If $V_{5\text{-}2} > 2$ V, artificial black levels are inserted during the horizontal blanking period. The clamp circuits then react upon these levels instead of the demodulated burst signals (necessary in case there are no horizontal burst signals available). The inserted signals may not be identical to the detected signals, because of circuitry spread. This can be corrected by detuning the demodulator tuned circuit.

### Modulation

The (R—Y)/(B—Y) ratio is nominally 1,78 at the de-emphasis output (pin 20). The demodulated (R—Y) and (B—Y) signals have a positive phase position for a magenta colour.

A burst signal is added to the demodulated SECAM signal at the input of the modulator. A sequential modulated chrominance signal is present at the modulator output. The modulation carriers of the (R—Y) and (B—Y) signals are 90° out of phase. The burst is modulated in the + (R—Y) direction and is only present during an (R—Y) line. The modulated (R—Y) component for a magenta colour has the same phase position as the (R—Y) burst.

### Identification

The identification circuit compares the voltage difference, which is obtained after demodulation, with the state of the flip-flop. For horizontal identification this comparison occurs during the internally generated 800 ns pulse. Only SECAM signals have a voltage difference from line to line during comparison. If the phase relationship between both the signals is wrong, the flip-flop will be reset by an extra input pulse.

The identification detector information is also used for colour killing and for switching to PAL, if required.

The identification (as above) occurs when the horizontal identification system is active. When the vertical identification system is switched on (pin 5), the system only compares the demodulator output voltage during line scanning of the vertical blanking. The further operation is identical to the horizontal identification.

### Sandcastle pulse detector

The sandcastle pulse detector is able to handle a 3-level sandcastle pulse. It detects the various blanking and gating pulses and it generates the correct drive pulses for the clamping circuits.

## FUNCTIONAL DESCRIPTION (continued)

### Carrier generation

The carrier signal for the PAL modulator is obtained from the 8,8 MHz oscillator signal of the TDA3560. The frequency of this signal is divided-by-two to obtain 90° shift. These two signals are applied to the modulator. There is a possibility that the two dividers in the TDA3560 (pins 23 and 24) and the TDA3591 are out-of-phase. This can be corrected by connecting pins 9 and 10 of the TDA3591 to pins 24 and 23 of the TDA3560 respectively. At incorrect phase, the TDA3591 divider is reset and correct phase is obtained.

### PAL-matrix and SECAM-switch

The colour difference signals are transmitted sequentially in the SECAM-system, so the modulated PAL-signal from the TDA3591 is also sequential. The consequences are:

- The two colour difference signals are mixed again in the delay line matrix circuit, so that both demodulators get a combination of an (R—Y) and (B—Y) signal. The phase position of the reference carrier must be very accurate for obtaining a proper demodulated signal, otherwise colour errors will occur (e.g. in the NTSC-system).
- Two different signals are added or subtracted in the matrix circuit, which results in an amplitude that has half the amplitude when compared with a normal PAL signal.

  Increase of the chrominance signal in the TDA3591 results in an overdrive of the chrominance amplifier of the TDA3560.

These effects are avoided by the matrix and switching circuit which is included in the TDA3591. The direct and delayed signals (from the PAL delay line) are applied to the processor where they are matrixed (for PAL) or switched (for SECAM). In the latter condition, the gain of the circuit is twice as high as for the normal PAL reception. The phase accuracy is not critical in this situation, because the two colour difference signals are not mixed.

For SECAM, the (B—Y) output of the SECAM-switch will be a signal without burst. The (R—Y) output of the SECAM-switch only has a burst during the +(R—Y) line. This burst is modulated in the +(R—Y) direction.

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | | |
|---|---|---|---|---|
| Supply voltage | $V_P = V_{17\text{-}2}$ | max. | 13,2 | V |
| Total power dissipation | $P_{tot}$ | max. | 1,7 | W |
| Storage temperature range | $T_{stg}$ | | −25 to +150 | °C |
| Operating ambient temperature range | $T_{amb}$ | | −25 to +65 | °C |

## CHARACTERISTICS

$V_P$ = 12 V; $T_{amb}$ = 25 °C; unless otherwise specified.

| parameter | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| **Supply** | | | | | |
| Supply voltage (pin 17) | $V_P$ | 10,8 | 12 | 13,2 | V |
| Supply current (pin 17) | $I_P$ | 50 | 90 | 120 | mA |
| Total power dissipation | $P_{tot}$ | — | 1,1 | — | W |
| Thermal resistance from junction to ambient | $R_{th\ j\text{-}a}$ | — | 40 | — | K/W |
| **Chrominance amplifier and demodulator** | | | | | |
| Input signal PAL (peak-to-peak value) | $V_{4\text{-}2(p\text{-}p)}$ | 55 | 550 | 1100 | mV |
| Input signal SECAM (peak-to-peak value) | $V_{4\text{-}2(p\text{-}p)}$ | 15 | — | 300 | mV |
| Input current | $I_4$ | 0,5 | 5 | 20 | µA |
| Input capacitance | $C_{4\text{-}2}$ | — | — | 5 | pF |
| (R—Y)/(B—Y) ratio before modulation (pin 20) | | 1,70 | 1,78 | 1,86 | |
| Relative deviation of the black level of the colour difference signals before modulation (pin 20) (note 1) | | — | 5 | — | % |
| Relative deviation of the black level of the colour difference signals before modulation without the application of a bell-shaped bandpass filter (note 2) | | — | — | 4 | % |
| Output signal PAL (peak-to-peak value) (note 3) | $V_{8\text{-}2(p\text{-}p)}$ | — | 265 | — | mV |
| Output signal SECAM (peak-to-peak value) | $V_{8\text{-}2(p\text{-}p)}$ | — | 1,3 | — | V |
| Output impedance | $\lvert Z_{8\text{-}2}\rvert$ | — | 50 | — | Ω |
| Input voltage for insertion of the artificial black level after demodulation | $V_{5\text{-}2}$ | 2 | — | 12 | V |
| Input resistance between pins 23 and 24 | $R_{23\text{-}24}$ | 3,0 | 4,0 | 5,0 | kΩ |
| Input capacitance between pins 23 and 24 | $C_{23\text{-}24}$ | — | 17 | — | pF |
| **Identification** | | | | | |
| Input voltage for horizontal identification | $V_{5\text{-}2}$ | 0 | — | 8 | V |
| Input voltage for vertical identification | $V_{5\text{-}2}$ | 10,5 | — | 12 | V |
| Input current at pin 5<br>$V_{5\text{-}2}$ = 12 V | $I_5$ | — | 3 | 10 | µA |
| Output current at pin 5<br>$V_{5\text{-}2}$ = 0 V (during horizontal blanking) | $-I_5$ | — | 0,1 | 5 | µA |

## CHARACTERISTICS

$V_P$ = 12 V; $T_{amb}$ = 25 °C; unless otherwise specified.

| parameter | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| **Identification** (continued) | | | | | |
| Voltage pin 6 for PAL | $V_{6\text{-}2}$ | – | 10,1 | – | V |
| Voltage at pin 6 for SECAM | $V_{6\text{-}2}$ | – | 7,0 | – | V |
| Identification 'on' for SECAM | $V_{6\text{-}2}$ | – | 10,6 | – | V |
| Colour 'off' for SECAM | $V_{6\text{-}2}$ | – | 9,25 | – | V |
| Colour 'on' for SECAM | $V_{6\text{-}2}$ | – | 9,1 | – | V |
| Voltage at pin 9 for SECAM | $V_{9\text{-}2}$ | 10,3 | 10,5 | – | V |
| Voltage between pins 9 and 10 for SECAM | $\pm V_{9\text{-}10}$ | – | – | 3 | mV |
| Permissible voltage at pins 9 and 10 for PAL | $V_{9\text{-}2}$;$V_{10\text{-}2}$ | 8,2 | – | 10,2 | V |
| **Sandcastle pulse detector and clamping pulse generator** | | | | | |
| Voltage level at which the vertical blanking pulse is separated | $V_{19\text{-}2}$ | 1 | 1,5 | 2 | V |
| required pulse amplitude | $V_{19\text{-}2(p\text{-}p)}$ | 2 | – | 3 | V |
| Voltage level at which the horizontal blanking pulse is separated | $V_{19\text{-}2}$ | 3 | 3,5 | 4 | V |
| required pulse amplitude | $V_{19\text{-}2(p\text{-}p)}$ | 4 | – | 6,7 | V |
| Voltage level at which the burst gating pulse is separated | $V_{19\text{-}2}$ | 6,7 | 7,2 | 7,7 | V |
| required pulse amplitude | $V_{19\text{-}2(p\text{-}p)}$ | 7,7 | – | 12 | V |
| Internal clamping pulse duration (note 4) | $t_p$ | – | 0,8 | – | µs |
| Input current at $V_{19\text{-}2}$ = 7 V | $I_2$ | – | 10 | 40 | µA |
| **Carrier generator (note 5)** | | | | | |
| Input signal from TDA3560 (peak-to-peak value) | $V_{16\text{-}2(p\text{-}p)}$ | 150 | – | – | mV |
| Input impedance | $\lvert Z_{7\text{-}2}\rvert$ | – | 1 | – | kΩ |
| Input resistance | $R_{7\text{-}2}$ | 3,5 | – | 5,5 | kΩ |
| **Luminance amplifier** | | | | | |
| Input signal (peak-to-peak value) | $V_{16\text{-}2(p\text{-}p)}$ | – | 0,45 | 0,7 | V |
| Luminance amplifier gain at 4,4 MHz | | 4 | 5 | 6 | dB |
| Input current | $I_{16}$ | – | 0,15 | 1 | µA |
| Output impedance (2 mA load current) | $\lvert Z_{15\text{-}2}\rvert$ | – | 20 | – | Ω |
| Frequency response (–3 dB) | f | 6 | – | – | MHz |

| parameter | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| **PAL-matrix and SECAM-switch** | | | | | |
| Burst signal amplitude at pins 11 and 12 (peak-to-peak value) | $V_{11,12(p\text{-}p)}$ | – | 60 | – | mV |
| Input resistance at pins 11 and 12 | $R_{11;12\text{-}12}$ | 1,5 | 2 | 2,5 | kΩ |
| Amplification for PAL | | | | | |
| pin 13 | | –1,3 | –0,3 | +0,7 | dB |
| pin 14 | | –1,5 | –0,5 | +0,5 | dB |
| Amplification for SECAM (pins 13 and 14) | | 4,5 | 5,5 | 6,5 | dB |
| Difference in amplification from the inputs to one output for PAL (note 6) | ΔG | – | – | 0,5 | dB |
| Phase error from line to line in the (R–Y) output for zero error in the (B–Y) output for PAL | | – | 2 | 3,5 | deg |
| Output impedance at pins 13 and 14 | $\|Z_{13;14-2}\|$ | – | 50 | – | Ω |

**Notes to characteristics**

1. A nominal value of 5% is obtained for clamping on the back porch of the colour difference signals. This value is related to the demodulated (B–Y) signal at Δf = 230 kHz. When an artificial black level is inserted after demodulation, the resulting black level deviation depends on the adjustment of the demodulator tuned circuit. It is therefore possible to obtain a value of zero percent.
2. This value is related to the demodulated (B–Y) signal at Δf = 230 kHz.
3. The luminance amplifier input voltage (peak-to-peak value) must be typically 0,45 V based on 75% saturated colour bar signals.
4. This pulse starts directly after the burst clamping pulse.
5. The phase delay between the oscillator output of the TDA3560 and the 8,8 MHz input of the TDA3591 (pin 7) must be adjusted so as to minimize the burst amplitude at pin 28 of the TDA3560.
6. $\Delta G = G_{11\text{-}13}/G_{12\text{-}13}$ and/or $G_{11\text{-}14}/G_{12\text{-}14}$.

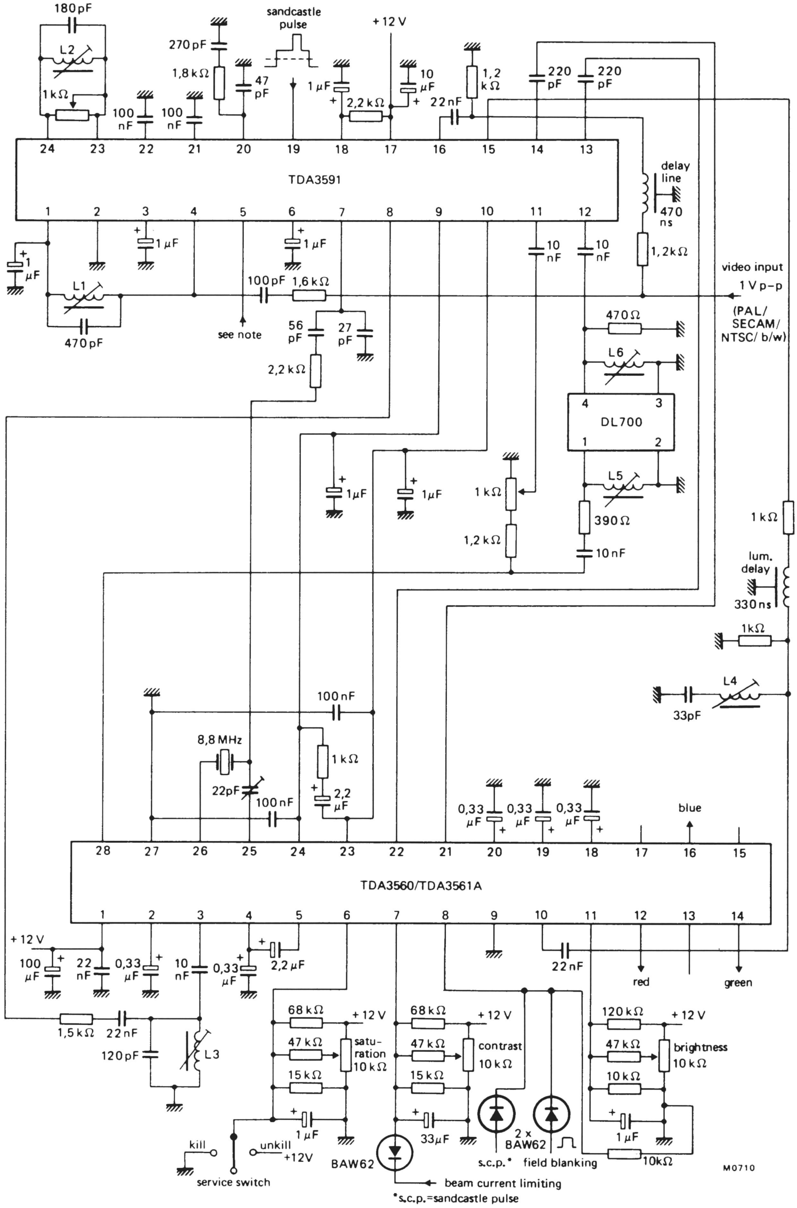

180 pF
L2
1 kΩ
270 pF
1,8 kΩ
47 pF
100 nF
100 nF
sandcastle pulse
+12 V
1 µF
2,2 kΩ
10 µF
22 nF
1,2 kΩ
220 pF
220 pF
24
23
22
21
20
19
18
17
16
15
14
13
TDA3591
1
2
3
4
5
6
7
8
9
10
11
12
delay line
470 ns
1 µF
1 µF
1 µF
L1
470 pF
100 pF
1,6 kΩ
see note
56 pF
27 pF
2,2 kΩ
10 nF
10 nF
1,2 kΩ
video input
1 V p-p
(PAL/ SECAM/ NTSC/ b/w)
470 Ω
L6
4
3
DL700
1
2
L5
390 Ω
10 nF
1 kΩ
1,2 kΩ
1 µF
1 µF
1 kΩ
lum. delay
330 ns
1 kΩ
L4
33 pF
100 nF
8,8 MHz
22 pF
100 nF
1 kΩ
2,2 µF
0,33 µF
0,33 µF
0,33 µF
blue
28
27
26
25
24
23
22
21
20
19
18
17
16
15
TDA3560/TDA3561A
1
2
3
4
5
6
7
8
9
10
11
12
13
14
+12 V
100 µF
22 nF
0,33 µF
10 nF
0,33 µF
2,2 µF
22 nF
red
green
1,5 kΩ
22 nF
120 pF
L3
68 kΩ
+12 V
47 kΩ
saturation 10 kΩ
15 kΩ
1 µF
68 kΩ
+12 V
47 kΩ
contrast 10 kΩ
15 kΩ
33 µF
120 kΩ
+12 V
47 kΩ
brightness 10 kΩ
10 kΩ
1 µF
10 kΩ
kill
unkill
+12V
service switch
BAW62
2 x BAW62
s.c.p.*
field blanking
beam current limiting
*s.c.p.=sandcastle pulse
M0710

Fig.2 PAL/SECAM application circuit diagram using the TDA3591 and TDA3560; (for a combination with the TDA3562A see Fig.3). For note to pin 5 of the TDA3591 see next page.

**Note to Fig. 2**

$V_{5\text{-}2} < 0{,}5$ V : horizontal identification and black level clamping.
$V_{5\text{-}2} > 10{,}5$ V : vertical identification and artificial black level.
$V_{5\text{-}2} = 5$ to 7 V: horizontal identification and artificial black level.

## PINNING

1. Limiter feedback to pin 4.
2. Ground.
3. Limiter feedback.
4. Input limiter; PAL identification input; SECAM chrominance/identification input.
5. Via a d.c. voltage to this pin, the SECAM identification system can be chosen.
   At $V_{5\text{-}2} < 8$ V the processor is preset for horizontal identification.
   At $V_{5\text{-}2} > 10{,}5$ V the processor is preset for vertical identification.
   At $V_{5\text{-}2} < 0{,}5$ V the demodulated black level of the SECAM horizontal burst will be used as black level reference.
   At $V_{5\text{-}2} > 2$ V the demodulated chroma signal will have an artificial black level during the SECAM horizontal burst.
6. Store capacitor of PAL/SECAM identification circuit;
   horizontal identification: 100 nF
   vertical identification: 1 μF
7. Input of 8,8 MHz oscillator signal.
8. PAL/processed SECAM signal output (chrominance output).
9. Identification input of 8,8 MHz divider (to pin 24 of TDA3560).
10. Identification input of 8,8 MHz divider (to pin 23 of TDA3560).
11. Direct chrominance input of PAL matrix/processed SECAM switch.
12. Delayed chrominance input of PAL matrix/processed SECAM switch.
13. PAL/processed SECAM (R–Y) h.f. output.
14. PAL/processed SECAM (B–Y) h.f. output.
15. Luminance output.
16. Luminance/PAL input.
17. Positive supply voltage (+ 12 V).
18. Decoupled positive supply voltage.
19. Three-level sandcastle pulse input. It detects the various blanking and gating pulses and it generates the correct drive pulses for the clamping circuits.
20. De-emphasis is performed at this pin with a 1,8 kΩ resistor and a 270 pF capacitor. To avoid moiré patterns on the screen, additional filtering of the demodulator double-frequency products is obtained by a 47 pF decoupling capacitor.
21. Store capacitor (B–Y) clamp.
22. Store capacitor (R–Y) clamp.
23. Demodulator reference tuned circuit.
24. Demodulator reference tuned circuit. The demodulator reference circuit has to be tuned to a nominal frequency of about 4,33 MHz. The quality factor of the tuned circuit must be nominal 2,45.

## APPLICATION INFORMATION (see Fig. 2)

**The function is described against the corresponding pin number**

### Pin 4. Chrominance input

The SECAM input signal is typically 100 mV peak to peak, while the PAL input signal is about 550 mV peak to peak. This corresponds to a PAL/SECAM ratio of 5,5 (based on 75% saturated colour bar signals). The input signal, which should be free from any sound modulation, is applied single-ended to pin 4 via a filter which provides the required bell-shaped bandpass for SECAM signals. D.C. biasing takes place via coil L1, which has an unloaded quality factor between 80 and 100.

### Pin 8. Chrominance output

During PAL reception, this output is internally connected to the luminance stage, therefore a composite video signal of 0,9 V peak to peak (typical) is present at the output. During SECAM reception, the chrominance output stage is connected to the modulator. The sequentially modulated (R—Y) and (B—Y) signals are then available at the output (amplitudes of typically 1300 mV peak to peak). These signals are applied via a chrominance bandpass filter to the chrominance a.c.c. amplifier in the TDA3560.

### Pin 6. System identification

A 1 μF capacitor is connected to this pin. During PAL reception, the typical voltage at pin 6 is 10,1 V. The chrominance output stage is then internally connected to the luminance stage and the PAL matrix circuit is activated for normal matrixing of the PAL signals. During SECAM reception, the voltage at pin 6 is about 7 V (typical). The chrominance output stage is connected to the modulator and the SECAM switch is enabled. During noisy SECAM signals, the voltage at pin 6 increases and colour killing/unkilling occurs around 9,25 V and 9,1 V respectively.

### Pin 5. Horizontal/vertical identification

Horizontal or vertical identification can be selected depending on the externally applied voltage at pin 5. When the d.c. level on pin 5 changes with time (pulse information), a combination of horizontal and vertical identification is possible.

*Horizontal identification*

If the voltage at pin 5 is < 2 V, horizontal identification occurs with black level clamping. This clamping occurs on the back-porch of the demodulated colour difference signals. If artificial black level insertion is required, the voltage at pin 5 should be < 8 V.

*Vertical identification*

If the voltage at pin 5 is > 10,5 V, vertical identification occurs, i.e. identification on 9 lines in the vertical blanking period. In this mode, the black level is artificially inserted after demodulation.

### Pin 19. Sandcastle pulse

A 3-level sandcastle pulse is required and this can be directly coupled to the sandcastle pulse detector. Horizontal blanking, vertical blanking and burst clamping pulses are separated by the IC. A clamping pulse of 800 ns is generated internally just after the burst gating pulse. The input current is typically 10 μA at an input signal of 7,2 V.

### Pins 16 and 15. Luminance input/output

The input signal at pin 16 should be typically 0,5 V peak to peak. The input impedance is relatively high, so a 22 nF coupling capacitor can be applied. This luminance signal is internally clamped and after a 2 times amplification available at pin 15.

During SECAM reception, the luminance signal is delayed by about 470 ns in a luminance delay line. The chrominance and luminance signals are then correctly timed at the output of the TDA3591.

During PAL reception, the composite video signal passes through this delay line and, after amplification, is available at pins 8 and 15. The nominal amplitude of the signals is 900 mV peak to peak in both cases.

### Pins 11, 12, 13 and 14. SECAM switch and PAL matrix

During PAL reception, the system identification 'enables' the PAL matrix circuitry. An a.c.c. composite chroma signal (from pin 28 TDA3560) is coupled via the glass delay line to pin 12 of the TDA3591. A direct signal is applied to pin 11 of the TDA3591 via a resistor network. Active matrixing takes place in the IC and consequently (R—Y) and (B—Y) signals are available at pins 13 and 14 respectively. These signals are applied to the TDA3560 demodulators (pins 22 and 21 respectively).

During SECAM reception, the PAL matrix circuitry is 'disabled' and the SECAM switch is 'enabled'. A sequentially modulated (R—Y) and (B—Y) signal is available at pin 28 of the TDA3560. Direct and delayed signals are applied to pins 11 and 12 of the TDA3591, and via the SECAM switch the (R—Y) and (B—Y) signals are applied to their respective demodulator in the TDA3560.

### Pins 17 and 18. Supply voltage (+ 12 V)

Correct operation is ensured within the supply range of 10,8 V to 13,2 V, and the typical power dissipation of the IC is 1,1 W at 12 V.

Pins 17 and 18 are separated by an external RC filter. Pin 18 is the supply for biasing several current-sinks in the IC and for all the output stages.

This supply voltage separation minimizes crosstalk via the supply lines between various parts of the circuitry. The capacitor at pin 18 must be small ($\approx 1\ \mu F$) so that, if pin 17 is short-circuited to ground, the collector-base junction of a transistor in the IC, through which the discharge current flows, is not damaged.

### Pin 20. De-emphasis

De-emphasis is performed at this pin with a 1,8 kΩ and a 270 pF capacitor. To avoid moiré patterns on the screen, additional filtering of the 8,8 MHz signal is obtained by a 47 pF decoupling capacitor.

### Pins 21 and 22. Clamping of (R—Y) and (B—Y) signals

After demodulation, the sequential (R—Y) and (B—Y) signals are separated by means of an H/2 switch and passed-on to their respective clamping circuits, where they are clamped to the same d.c. level. The value of each clamping capacitor should be 100 nF and they may, if desired, be increased to 470 nF.

### Pins 23 and 24. Demodulator reference tuned circuit

The SECAM signal is applied to the demodulator via the 'bell-filter' and limiter/amplifier. Only one demodulator is used because of the sequential nature of the signal. The reference signal, obtained from the tank circuit, is applied to pins 23 and 24. At $V_{5-2} > 2$ V, the tuning and damping of the tank circuit should be done in such a way that a minimum modulator output voltage at pin 8 of the TDA3591 is obtained (the (R—Y) and (B—Y) information in the SECAM video signal is switched off). Therefore, any deviations between the black levels (when clamping on the back-porch and when an artificial black level is filled in) can be made minimum.

## APPLICATION INFORMATION (continued)

### Pin 7. Carrier generation

An 8,8 MHz signal from pin 25 of the TDA3560 is applied via pin 7 to the divider circuit in the TDA3591. Two 4,4 MHz signals are obtained with a phase shift of 90° with respect to each other. These signals are applied to the modulator via an H/2 switch. The phase delay of the 8,8 MHz input signal must be adjusted such that the burst amplitude of the chrominance signal at pin 28 (TDA3560) has its minimum amplitude. Under this condition, the burst generated by the TDA3591 is in phase with the (R–Y) reference signal for the demodulator in the TDA3560. Since the a.c.c. of the TDA3560 operates in the + (R–Y) direction, the burst signal at pin 28 of the TDA3560 will have its minimum amplitude.

### Pins 9 and 10. Divider resetting

The output of the burst phase detector of the TDA3560 is connected to pins 9 and 10. At SECAM reception, the differential a.c. current information, obtained from the burst detector (TDA3560), is applied to pins 9 and 10 (TDA3591). This gives information about the phase relationship between the two 4,4 MHz dividers in both ICs. The TDA3591 now generates a minimum relative voltage between pins 9 and 10 at an absolute voltage level of 10,6 V. The result is that the oscillator control function of the TDA3560 is overruled, and the oscillator is set to 2 x 4,43 MHz.

DEVELOPMENT SAMPLE DATA

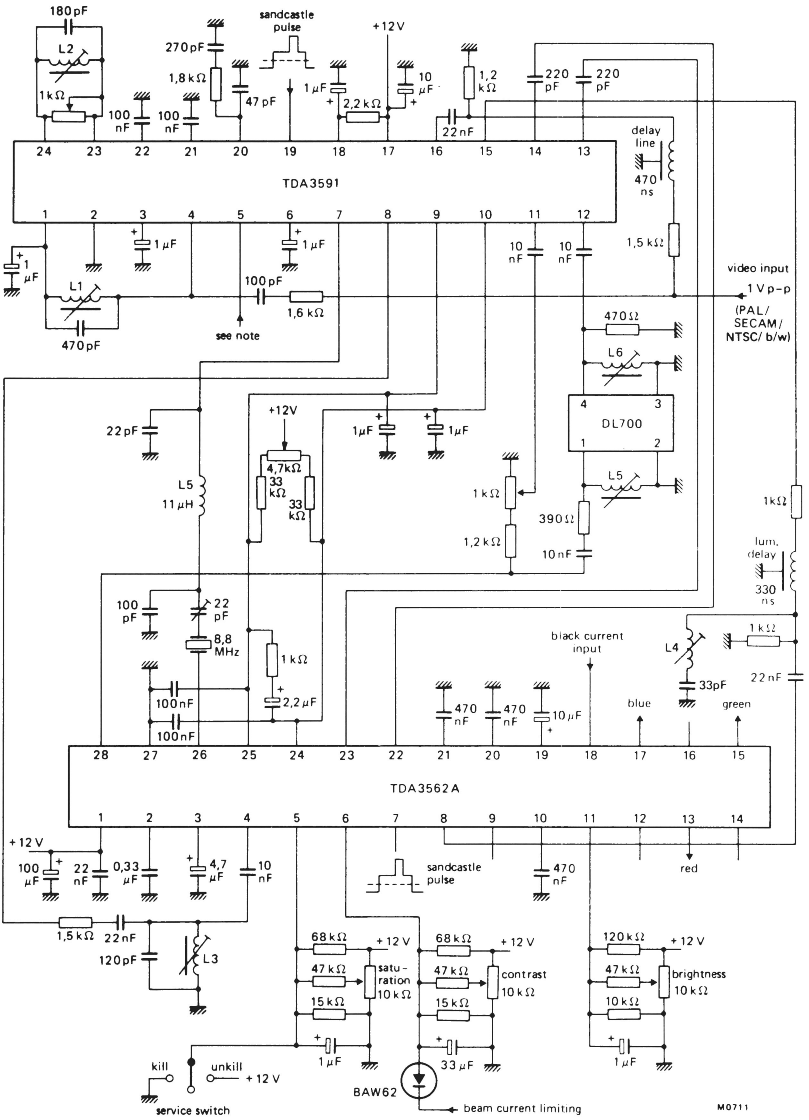

180 pF
L2
1 kΩ
270 pF
1,8 kΩ
47 pF
100 nF
100 nF
sandcastle pulse
+12 V
1 μF
2,2 kΩ
10 μF
22 nF
1,2 kΩ
220 pF
220 pF
delay line
470 ns
TDA3591
24
23
22
21
20
19
18
17
16
15
14
13
1
2
3
4
5
6
7
8
9
10
11
12
1 μF
1 μF
1 μF
L1
470 pF
100 pF
1,6 kΩ
see note
10 nF
10 nF
1,5 kΩ
video input
1 V p-p
(PAL/ SECAM/ NTSC/ b/w)
470 Ω
L6
DL700
4
3
1
2
L5
390 Ω
10 nF
1 kΩ
1,2 kΩ
22 pF
L5
11 μH
+12V
4,7 kΩ
33 kΩ
33 kΩ
1 μF
1 μF
1 kΩ
lum. delay
330 ns
100 pF
22 pF
8,8 MHz
1 kΩ
2,2 μF
100 nF
100 nF
black current input
L4
1 kΩ
33pF
22 nF
470 nF
470 nF
10 μF
blue
green
TDA3562A
28
27
26
25
24
23
22
21
20
19
18
17
16
15
1
2
3
4
5
6
7
8
9
10
11
12
13
14
+12 V
100 μF
22 nF
0,33 μF
4,7 μF
10 nF
sandcastle pulse
470 nF
red
1,5 kΩ
22 nF
120 pF
L3
68 kΩ
+12 V
47 kΩ
satu-ration 10 kΩ
15 kΩ
1 μF
68 kΩ
+12 V
47 kΩ
contrast 10 kΩ
15 kΩ
33 μF
120 kΩ
+12 V
47 kΩ
brightness 10 kΩ
10 kΩ
1 μF
kill
unkill
+ 12 V
service switch
BAW62
beam current limiting
M0711

Fig.4 PAL/SECAM application circuit diagram using the TDA3591 and the TDA3562A.

Note to pin 5 TDA3591: $V_{5\text{-}2} < 2$ V; horizontal identification and black level clamping.

$V_{5\text{-}2} > 10{,}5$ V; vertical identification and artificial black level.

$2\text{ V} < V_{5\text{-}2} < 10{,}5$ horizontal identification and artificial black level.

# VERTICAL DEFLECTION CIRCUIT

## GENERAL DESCRIPTION

TDA3650 is a monolithic integrated circuit for vertical deflection in large screen colour television receivers.

The circuit incorporates the following functions:

- Oscillator
- Synchronization circuit
- Blanking pulse generator
- Sawtooth generator
- S-correction and linearity control
- Comparator and drive circuit
- Output stage
- Flyback generator
- Voltage stabilizer
- Thermal protection circuit
- Guard circuit
- Output stage protection

## QUICK REFERENCE DATA

| | | | | |
|---|---|---|---|---|
| Supply voltage range (pin 13) | $V_{P1} = V_{13\text{-}12}$ | | 0 to 30 | V |
| Output current (peak-to-peak value) | $I_{3(p\text{-}p)}$ | typ. | 2,2 | A |
| Operating junction temperature | $T_j$ | max. | 150 | °C |
| Thermal resistance from junction to copper heat spreader (mounting base) | $R_{th\ j\text{-}mb}$ | max. | 4 | K/W |

## PACKAGE OUTLINE

TDA3650: 13-lead SIL bent to DIL; plastic power (SOT-141B).

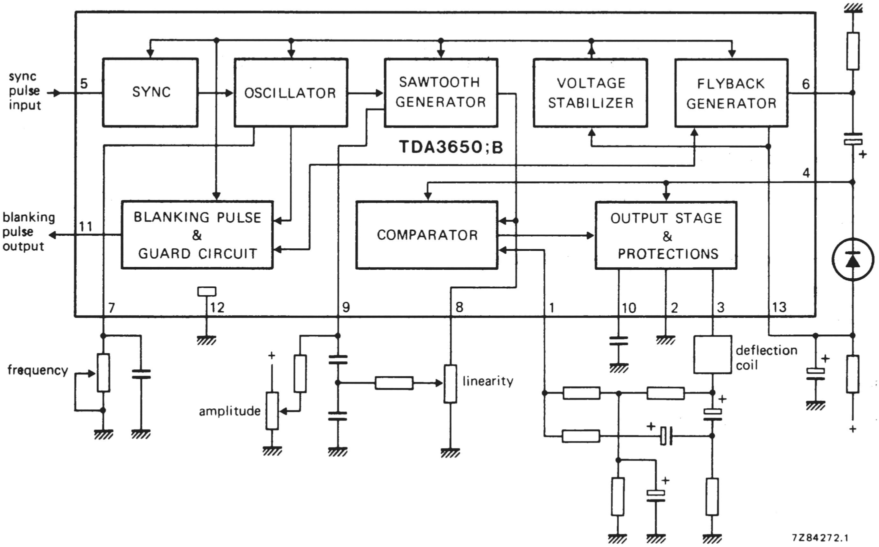

sync pulse input
5
SYNC
OSCILLATOR
SAWTOOTH GENERATOR
VOLTAGE STABILIZER
FLYBACK GENERATOR
6
TDA3650;B
4
blanking pulse output
11
BLANKING PULSE & GUARD CIRCUIT
COMPARATOR
OUTPUT STAGE & PROTECTIONS
7
12
9
8
1
10
2
3
13
frequency
amplitude
linearity
deflection coil
7Z84272.1

Fig. 1 Block diagram.

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

**Voltages**

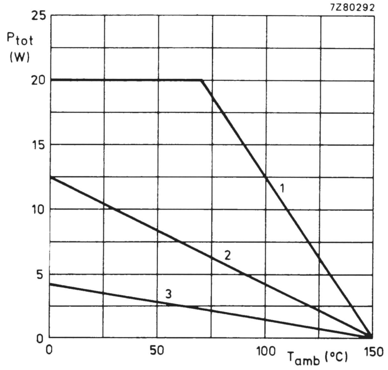
| | | | | |
|---|---|---|---|---|
| Pin 1; feedback voltage | $V_{1\text{-}12}$ | max. | 6 | V |
| Pin 3; output voltage | $V_{3\text{-}12}$ | max. | 50 | V |
| Pin 4; supply voltage output stage | $V_{4\text{-}12}$ ($V_{P2}$) | max. | 47 | V |
| Pin 5; sync voltage | $V_{5\text{-}12}$ | max. | 6 | V |
| Pin 11; blanking pulse | $V_{11\text{-}12}$ | max. | 6 | V |
| Pin 13; supply voltage | $V_{13\text{-}12}$ ($V_{P1}$) | max. | 30 | V |

**Currents**

| | | | | |
|---|---|---|---|---|
| Pin 3; repetitive peak output current | $\pm I_{3RM}$ | max. | 2,8 | A |
| Pin 3; non-repetitive peak output current | $\pm I_{3SM}$ | max. | 6 | A |
| Pin 6; flyback generator | $I_6$ | max. | 2,8 | A |
| Pin 11; blanking pulse | $I_{11}$ | max. | 10 | mA |

Total power dissipation internally limited by the thermal protection circuit (see also Fig. 2)

| | | | | |
|---|---|---|---|---|
| Storage temperature range | $T_{stg}$ | | −65 to + 150 | °C |
| Operating junction temperature | $T_j$ | max. | 150 | °C |



(1) Mounted on infinite heatsink.
(2) Mounted on heatsink of 8 K/W.
(3) Without heatsink.

Fig. 2 Total power dissipation derating curves.

## THERMAL RESISTANCE

| | | | | |
|---|---|---|---|---|
| From junction to mounting base | $R_{th\ j\text{-}mb}$ | = | 4 | K/W |

## CHARACTERISTICS

$V_S$ = 26 V; pins 2 and 12 connected; $T_{amb}$ = 25 °C unless otherwise specified

| parameter | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| **Supply** | | | | | |
| Supply voltage range (note 1); $V_{P1}$ | $V_{13\text{-}2}$ | 10 | – | 30 | V |
| Supply voltage range output stage; $V_{P2}$ | $V_{4\text{-}2}$ | 10 | – | 47 | V |
| Supply current (without load) | $I_{13}$ | – | 55 | – | mA |
| **Output** (pin 3) | | | | | |
| Output voltage (note 2) | | | | | |
| minimum | $V_{3\text{-}2}$ | – | 2,5 | 3,0 | V |
| maximum | $V_{3\text{-}2}$ | $V_{P2}-3$ | $V_{P2}-2{,}5$ | 50 | V |
| Output current (peak-to-peak value) | $I_{3(p\text{-}p)}$ | – | 2,2 | 2,8 | A |
| Output current temperature dependency | $\Delta I_3/\Delta T$ | – | –0,03 | – | %/K |
| **Sync** (pin 5) | | | | | |
| Input voltage | $V_{5\text{-}12}$ | 1,0 | – | 6,0 | V |
| Sync pulse width (note 4) | $t_p$ | – | – | 200 | μs |
| Input impedance during oscillator scan | $\|Z_{5\text{-}12}\|$ | 1,8 | 2,2 | 2,6 | kΩ |
| **Oscillator** (pin 7) | | | | | |
| Input current during scan | $I_7$ | – | 1,0 | 3,0 | μA |
| Tracking range (note 5) | | 18 | 20 | 24 | % |
| Frequency dependency | | | | | |
| with temperature | $\Delta f/\Delta T$ | – | – | –0,02 | Hz/K |
| with supply voltage | $\Delta f/\Delta V_{P1}$ | – | – | –0,03 | Hz/V |
| Tolerance of frequency adjustment range | $\Delta f_o/f_o$ | – | – | ± 3,5 | % |
| **Sawtooth generator** (pin 9) | | | | | |
| Sawtooth voltage | | | | | |
| range | $V_{9\text{-}12}$ | 1,6 | – | 3,8 | V |
| tolerance of minimum voltage level | $V_{9\text{-}12}$ | 1,45 | 1,6 | 1,7 | V |
| Input resistance of pin 9 | | | | | |
| during scan | $R_{9\text{-}12}$ | 0,5 | – | – | MΩ |
| during oscillator flyback | $R_{9\text{-}12}$ | 500 | 650 | 800 | Ω |
| Voltage offset between pins 8 and 9 | $V_{8\text{-}9}$ | – | 40 | 100 | mV |
| **Blanking pulse generator** (pin 11) | | | | | |
| Output voltage; $I_{11}$ = 0 | $V_{11\text{-}12}$ | 5,5 | 6,0 | 6,5 | V |
| Blanking pulse width (note 3) | $t_p$ | 1,3 | 1,4 | 1,5 | ms |
| Blanking pulse dependence with oscillator frequency (note 3) | $\Delta t_p/\Delta f$ | – | –0,024 | – | ms/Hz |
| Output impedance during blanking | $\|Z_{11\text{-}12}\|$ | – | 400 | 550 | Ω |
| Blanking pulse output current | $I_{11}$ | – | – | 10 | mA |

| parameter | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| **Comparator** (pin 1) | | | | | |
| Input voltage | $V_{1\text{-}12}$ | 2,3 | – | 3,8 | V |
| Input voltage temperature dependency | $\Delta V_{1\text{-}12}/\Delta T$ | – | 1,0 | – | mV/K |
| Tolerance of d.c. level | $\Delta V_{1\text{-}12}$ | – | – | ± 150 | mV |
| Open loop voltage gain (note 6) $V_{3\text{-}12}/V_{1\text{-}12}$ at 1000 Hz | $G_o$ | – | 64 | – | dB |
| Frequency response (note 6) at –3 dB | f | – | 10 | – | kHz |
| Input current | $I_1$ | – | – | 5 | μA |
| External load impedance of pin 8 | $\lvert Z_{8\text{-}12}\rvert$ | 12 | – | – | kΩ |
| **Flyback generator** (pin 6) | | | | | |
| Maximum output voltage (note 2) | $V_{6\text{-}2}$ | $V_{P1}-5$ | $V_{P1}-3$ | – | V |
| Output current (peak-to-peak value) | $I_{6(p\text{-}p)}$ | – | 2,2 | 2,8 | A |
| **Thermal data** | | | | | |
| Junction temperature thermal protection switching level | $T_j$ | 158 | 175 | 198 | °C |
| Thermal resistance from junction to copper heat spreader (mounting base) | $R_{th\ j\text{-}mb}$ | – | – | 4 | K/W |

**Notes to characteristics**

1. When the flyback generator is used, the maximum supply voltage must be chosen such that during flyback the voltage at pin 3 and pin 4 (supply voltage output stage) does not exceed 50 V.
2. These values (pin 3) are obtained at an output current of 2,8 A peak-to-peak (knee voltages of the output transistors). For an output current of 1 A peak-to-peak the maximum knee voltage is 2,5 V.

   The output voltage of the flyback generator is given at an output current of 2,8 A peak-to-peak ($I_6$). For an output current of 1 A peak-to-peak the output voltage at pin 3 will be $V_{P1} - 2,5$ V.
3. These values are obtained with the free running oscillator frequency adjusted to 45,5 kHz (22 ms) and an external 150 Ω resistor connected to pin 7 in series with the 150 nF capacitor. Without the 150 Ω resistor the width of the blanking pulse is 1,6 ± 0,1 ms.
4. The width of the synchronization pulse must be smaller than the oscillator flyback.
5. These values are obtained with the free running oscillator frequency adjusted to 45,5 kHz (22 ms).
6. These values are obtained with a load resistance of 1 kΩ between pin 3 and ground, and a 4,7 nF decoupling capacitor connected between pin 10 and ground.

## APPLICATION INFORMATION

The function is described against the corresponding pin number.

### 1. Comparator and drive circuit

The current flowing through the deflection coils is measured across an external series resistor. The signal across this resistor is fed to the comparator via pin 1, where it is compared with the internally generated sawtooth signal. The output of the comparator drives the output stage. Pin 1 is also used for d.c. feedback of the output stage (mid-point setting).

### 2. Negative supply (ground) for the output stage

### 3. Output stage

The output stage provides the current to the deflection coils. The vertical deflection coil is connected to this pin, via a series connection of a coupling capacitor and a feedback resistor to ground. The output stage is protected against over-voltages and over-currents by a SOAR-protection circuit. When one of the transistors exceeds its operational threshold the drive current is reduced to a safe level. Temperature protection reduces the drive of the output stage when the junction temperature exceeds 170 °C.

### 4. Positive supply of output stage

This supply is obtained from the flyback generator. An electrolytic capacitor between pins 4 and 6, a diode between pins 4 and 13, and a resistor between pins 6 and ground must be connected for correct operation of the flyback generator.

### 5. Synchronization input

When the voltage applied to pin 5 reaches a level of 0,7 V the lower switching level is increased thus initiating the charge cycle of the oscillator capacitor. The synchronization circuit is inhibited during oscillator flyback time.

### 6. Flyback generator

The flyback generator reduces power dissipation in the vertical stage. As a result a lower power supply can be chosen (26 V for 30AX application). Whereas the voltage during flyback is increased to 45 V (depending on the design of external components), the maximum increase of the voltage during flyback is nearly factor 2.

The capacitor between pins 6 and 4 is charged via the external diode during the scan period. Then, when the flyback generator is activated by the oscillator flyback pulse, the voltage across the capacitor is connected in series with the supply voltage to provide the required flyback voltage. At the end of the oscillator pulse the drive of the flyback generator is maintained by the flyback voltage of the deflection circuit.

### 7. Oscillator

The oscillator frequency is determined by the values of the external resistor and capacitor connected in parallel to pin 7. The capacitor is discharged via the resistor which is connected to ground. The voltage on the capacitor is compared with an internal voltage from the voltage stabilizer (lower switching level). When this lower switching level is reached the capacitor is charged via an internal 500 Ω resistor. At the same time the comparator voltage is increased (higher switching level). When the voltage on the capacitor reaches the higher switching level the charge current is switched off and the capacitor is discharged again.

### 8. S-correction and linearity circuit

From pin 8 an adjustable parabolic current is fed back to the mid-point of the sawtooth generator capacitors at pin 9 to provide linearity control. The external components connected between pins 8 and 9 together with the d.c. feedback circuitry at pin 1 define the S-shape of the deflection current.

### 9. Sawtooth generator

The sawtooth signal is obtained by charging the capacitors connected to pin 9 via an external resistor. Variation of the charge current will vary the amplitude of the signal. During oscillator flyback time the capacitors are discharged to an internally fixed voltage level.

### 10. Output stage decoupling

A low value capacitor must be connected to pin 10 for decoupling of the output driver stage.

### 11. Blanking pulse generator

The blanking pulse duration is determined by the oscillator sawtooth signal. The guard circuit provides continuous blanking when the vertical deflection current is absent.

### 12. Negative supply (ground) of small-signal part

### 13. Positive supply

The supply voltage at this pin is used to supply the flyback generator, the voltage stabilizer and the protection circuits.

The following application data are measured in a typical 30AX system (Fig. 3).

| parameter | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| **Supply** (pin 13) | | | | | |
| Supply voltage* | $V_{13\text{-}12}$ | 22 | 26 | 30 | V |
| Supply current* | $I_{13}$ | 260 | 320 | 380 | mA |
| **Output** (pin 3) | | | | | |
| Output voltage (peak value) | $V_{3\text{-}2}$ | – | – | 50 | V |
| Output voltage (mid-point) | $V_{3\text{-}2}$ | – | 13 | – | V |
| Output current (peak-to-peak value)** | $I_{3(p\text{-}p)}$ | 1,6 | 2,1 | 2,4 | A |
| Flyback time▲ | $t_{f1}$ | – | 0,7 | 0,9 | ms |
| Total power dissipation in IC▲ | $P_{tot}$ | – | 4,6 | 5,0 | W |
| Total power consumption | P | 5,2 | 8,5 | 11,5 | W |
| Blanking time | $t_p$ | – | 1,45 | – | ms |
| Non-linearity | | – | – | 3 | % |
| Thermal resistance of heatsink | $R_{th\ h\text{-}a}$ | – | 8 | – | K/W |
| Ambient temperature | $T_{amb}$ | – | – | 65 | °C |

* These values are obtained with a supply voltage ($V_S$) of 26 V and an output current of 2,1 A peak-to-peak. When the supply voltage is decreased to 22 V the output current changes to 1,6 A peak-to-peak and the supply current to 260 mA. When the supply voltage is increased to 30 V the output current increases to 2,4 A peak-to-peak and the supply current to 380 mA. But when the circuit is adjusted for an output current of 2,1 A peak-to-peak at a supply voltage of 30 V, the supply current remains at 320 mA (see note 1 to characteristics).

** Including 6% overscan.

▲ With the supply voltage $V_S$ = 26 V.

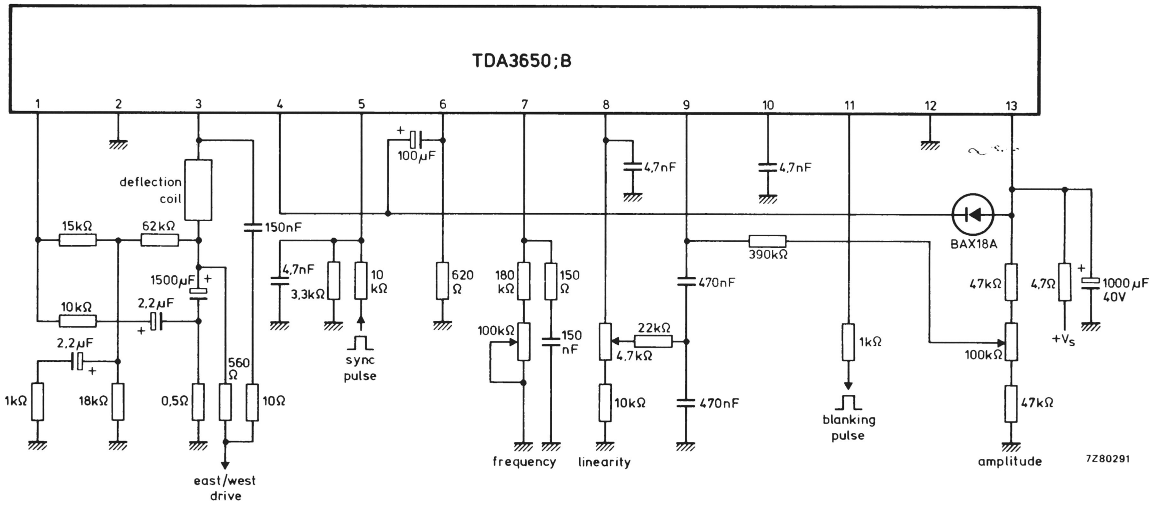

TDA3650;B
1
2
3
4
5
6
7
8
9
10
11
12
13
deflection coil
15kΩ
62kΩ
150nF
1500µF
+
10kΩ
2,2µF
+
2,2µF
+
1kΩ
18kΩ
0,5Ω
560 Ω
10Ω
east/west drive
4,7nF
3,3kΩ
10 kΩ
sync pulse
+
100µF
620 Ω
180 kΩ
150 Ω
100kΩ
150 nF
frequency
4,7nF
22kΩ
4,7kΩ
10kΩ
linearity
470nF
470nF
4,7nF
390kΩ
1kΩ
blanking pulse
BAX18A
47kΩ
100kΩ
47kΩ
amplitude
4,7Ω
+Vs
+
1000µF 40V
7Z80291

Fig. 3 Complete vertical deflection circuit for 30AX.

This information is derived from development samples
made available for evaluation. It does not necessarily
imply that the device will go into regular production.

# VERTICAL DEFLECTION CIRCUIT

The TDA3651 is a vertical deflection output circuit for drive of various deflection systems with deflection currents up to 2 A peak-to-peak.

The circuit incorporates the following functions:

- Driver
- Output stage
- Thermal protection and output stage protection
- Flyback generator
- Voltage stabilizer

## QUICK REFERENCE DATA

| | | | | |
|---|---|---|---|---|
| Supply voltage (pin 9) | $V_P$ | typ. | 26 | V |
| Output current (peak-to-peak value) | $I_{5(p\text{-}p)}$ | $<$ | 2 | A |
| Operating junction temperature | $T_j$ | max. | 150 | °C |
| Thermal resistance from junction to tab | $R_{th\,j\text{-}tab}$ | typ. | 10 | K/W |

## PACKAGE OUTLINE

9-lead SIL; plastic (SOT-110B).

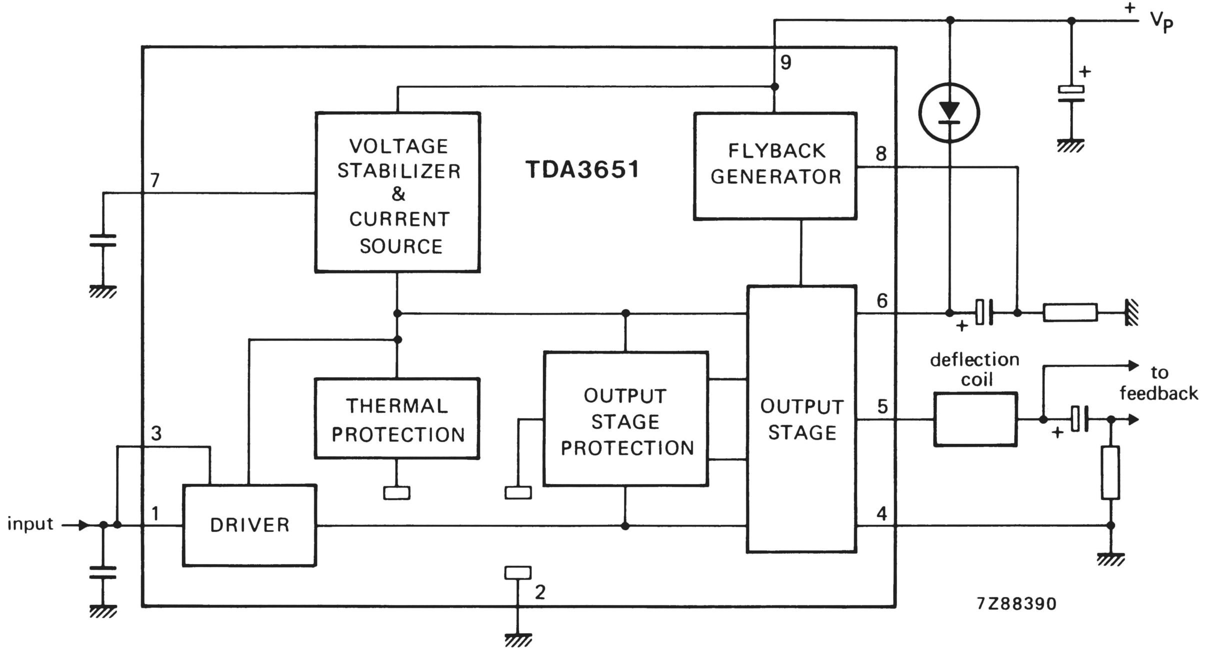

+ V_P
9
8
6
5
4
7
3
1
2
VOLTAGE STABILIZER & CURRENT SOURCE
TDA3651
FLYBACK GENERATOR
THERMAL PROTECTION
OUTPUT STAGE PROTECTION
OUTPUT STAGE
DRIVER
input
deflection coil
to feedback
+
7Z88390

Fig. 1 Block diagram.

## GENERAL DESCRIPTION

### Output stage and protection circuit

Pin 5 is the output pin. The supply for the output stage is fed to pin 6 and the output stage ground is connected to pin 4. The output transistors of the class-B output stage can each deliver 1 A maximum. The 'upper' power transistor is protected against short-circuit currents to ground, whereas, during flyback, the 'lower' power transistor is protected against too high voltages which may occur during adjustments.
Moreover, the output transistors have been given extra solidity by means of special measures in the internal circuit layout.
A thermal protection circuit is incorporated to protect the IC against too high dissipation. This circuit is 'active' at 175 °C and then reduces the deflection current to such a value that the dissipation cannot increase.

### Driver and switching circuit

Pin 1 is the input for the driver of the output stage. The signal at pin 1 is also applied to pin 3 which is the input of a switching circuit. When the flyback starts, this switching circuit rapidly turns off the lower output stage and so limits the turn-off dissipation. It also allows a quick start of the flyback generator.
Pin 3 is connected externally to pin 1, in order to allow for different applications in which pin 3 is driven separately from pin 1.

### Flyback generator

The capacitor at pin 6 is charged to a maximum voltage, which is equal to the supply voltage $V_P$ (pin 9), during scan.
When the flyback starts and the voltage at the output pin (pin 5) exceeds the supply voltage (pin 9), the flyback generator is activated. Then $V_P$ is connected in series (via pin 8) with the voltage across the capacitor.
The voltage at the supply pin (pin 6) of the output stage will then be maximum twice $V_P$. Lower voltages can be chosen by changing the value of the external resistor at pin 8.

### Voltage stabilizer

The internal voltage stabilizer provides a stabilized supply of 6 V for drive of the output stage, so the drive current of the output stage is not affected by supply voltage variations. The stabilized voltage is available at pin 7.
A decoupling capacitor of 2,2 μF can be connected to this pin.

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

**Voltages** (pins 4 and 2 externally connected to ground)

| | | | |
|---|---|---|---|
| Output voltage (pin 5) | $V_{5\text{-}4}$ | max. | 50 V |
| Supply voltage (pin 9) | $V_{9\text{-}4} = V_P$ | max. | 50 V |
| Supply voltage output stage (pin 6) | $V_{6\text{-}4}$ | max. | 50 V |
| Input voltage (pins 1 and 3) | $V_{1\text{-}2}; V_{3\text{-}2}$ | max. | $V_P$ |

**Currents**

| | | | |
|---|---|---|---|
| Repetitive peak output current (pin 5) | $\pm I_{5RM}$ | max. | 1 A |
| Non-repetitive peak output current (pin 5) | $\pm I_{5SM}$ | max. | 1,5 A* |
| Repetitive peak flyback generator output current (pin 8) | $I_{8RM}$ | max. | −1,0 A<br>+ 1,1 A |
| Non-repetitive peak flyback generator output current (pin 8) | $I_{8SM}$ | max. | −1,5 A<br>+ 1,6 A* |

**Temperatures**

| | | |
|---|---|---|
| Storage temperature range | $T_{stg}$ | −65 to + 150 °C |
| Operating ambient temperature range | $T_{amb}$ | −25 to + 65 °C |
| Operating junction temperature range | $T_j$ | −25 to + 150 °C |

## CHARACTERISTICS

$T_{amb} = 25\ ^{o}C$; $V_P = 26$ V; pins 4 and 2 externally connected to ground; unless otherwise specified.

| | | | |
|---|---|---|---|
| Output current (peak-to-peak value) | $I_{5(p\text{-}p)}$ | typ.<br>< | 1,5 A<br>2,0 A |
| Flyback generator output current | $-I_8$ | typ.<br>< | 0,85 A<br>1,1 A |
| Flyback generator output current | $I_8$ | typ.<br>< | 0,75 A<br>1,0 A |

**Output voltages**

| | | | |
|---|---|---|---|
| Peak voltage during flyback | $V_{5\text{-}4M}$ | < | 50 V |
| Saturation voltage to supply at $-I_5 = 1$ A | $-V_{5\text{-}6sat}$ | typ.<br>< | 2,5 V<br>3,0 V |
| Saturation voltage to ground at $I_5 = 1$ A | $V_{5\text{-}4sat}$ | typ.<br>< | 2,5 V<br>3,0 V |
| Saturation voltage to supply at $-I_5 = 0{,}75$ A | $-V_{5\text{-}6sat}$ | typ.<br>< | 2,2 V<br>2,7 V |
| Saturation voltage to ground at $I_5 = 0{,}75$ A | $V_{5\text{-}4sat}$ | typ.<br>< | 2,2 V<br>2,7 V |

---

* Non-repetitive duty factor maximum 3,3%.

DEVELOPMENT SAMPLE DATA

| | | | |
|---|---|---|---|
| **Supply** | | | |
| Supply voltage | $V_{9\text{-}2;4}$ | | 10 to 50 V* |
| Supply voltage output stage | $V_{6\text{-}4}$ | < | 50 V* |
| Supply current (no load and no quiescent current) | $I_9$ | typ.<br>< | 9 mA<br>12 mA |
| Quiescent current (see Fig. 2) | $I_4$ | typ. | 38 mA<br>25 to 52 mA |
| Variation of quiescent current with temperature | | typ. | −0,04 mA/K |
| **Flyback generator** | | | |
| Saturation voltage at $-I_8 = 1{,}1$ A | $V_{9\text{-}8sat}$ | typ.<br>< | 1,6 V<br>2,1 V |
| Saturation voltage at $I_8 = 1$ A | $V_{8\text{-}9sat}$ | typ.<br>< | 2,5 V<br>3,0 V |
| Saturation voltage at $I_8 = 0{,}85$ A | $V_{9\text{-}8sat}$ | typ.<br>< | 1,4 V<br>1,9 V |
| Saturation voltage at $I_8 = 0{,}75$ A | $V_{8\text{-}9sat}$ | typ.<br>< | 2,3 V<br>2,8 V |
| Flyback generator active if: | $V_{5\text{-}9}$ | > | 4 V |
| Leakage current | $-I_8$ | typ.<br>< | 5 μA<br>100 μA |
| Input current for $\pm I_5 = 1$ A | $I_1$ | typ. | 230 μA<br>175 to 380 μA |
| Input voltage during scan | $V_{1\text{-}2}$ | typ. | 1,9 V<br>0,9 to 2,7 V |
| Input current during scan | $I_3$ | | 0,01 to 2,5 mA |
| Input voltage during scan | $V_{3\text{-}2}$ | | 0,9 to $V_P$ V |
| Input voltage during flyback | $V_{3\text{-}2}$ | | 0 to 0,2 V |
| Voltage at pin 7 | $V_{7\text{-}2}$ | typ. | 6,1 V<br>5,6 to 6,6 V |
| Load current of pin 7 | $I_7$ | < | 2 mA |
| Unloaded voltage at pin 7 during flyback | $V_{7\text{-}2}$ | typ. | 15 V |
| Junction temperature of switching on the thermal protection | $T_j$ | typ. | 175 °C<br>158 to 192 °C |
| Thermal resistance from junction to tab | $R_{th\,j\text{-}tab}$ | typ.<br>< | 10 K/W<br>12 K/W |
| Power dissipation | see Fig. 3 | | |
| Open loop gain at 1 kHz; $R_{load} = 1\ k\Omega$ | $G_o$ | typ. | 36 dB |
| Frequency response (−3 dB); $R_{load} = 1\ k\Omega$ | f | typ. | 60 kHz |

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* The maximum supply voltage should be chosen such that during flyback the voltage at pin 5 does not exceed 50 V.

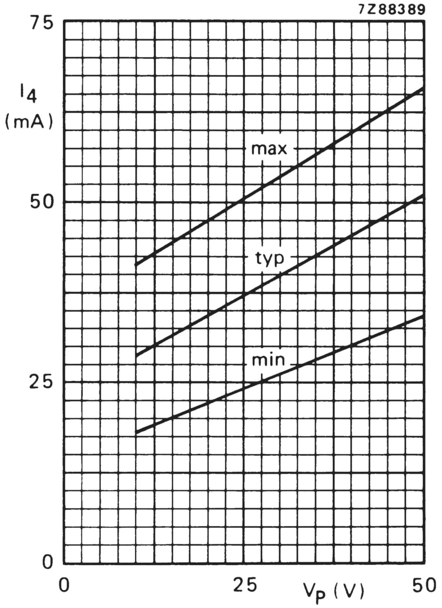

Fig. 2 Quiescent current $I_4$ as a function of supply voltage $V_P$.

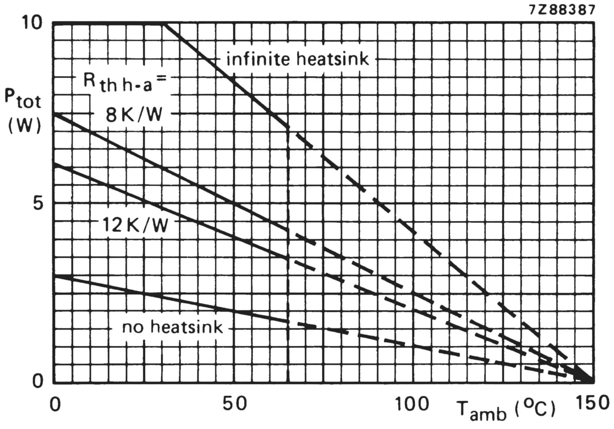

Fig. 3 Power derating curves.

## APPLICATION INFORMATION

The following application data are measured in a typical application as shown in Figs 4 and 5.

| | | | | |
|---|---|---|---|---|
| Deflection current (including 6% overscan) peak-to-peak value | $I_{5(p\text{-}p)}$ | typ. | 0,87 | A |
| Supply voltage | $V_{9\text{-}4}$ | typ. | 26 | V |
| Total supply current | $I_{tot}$ | typ. | 148 | mA |
| Peak output voltage during flyback | $V_{5\text{-}4M}$ | < | 50 | V |
| Saturation voltage to supply | $V_{5\text{-}6sat}$ | typ.<br>< | 2,0<br>2,5 | V<br>V |
| Saturation voltage to ground | $V_{5\text{-}4sat}$ | typ.<br>< | 2,0<br>2,5 | V<br>V |
| Flyback time | $t_{fl}$ | typ.<br>< | 0,95<br>1,2 | ms<br>ms |
| Total power dissipation in IC | $P_{tot}$ | typ. | 2,5 | W |
| Operating ambient temperature | $T_{amb}$ | < | 65 | °C |

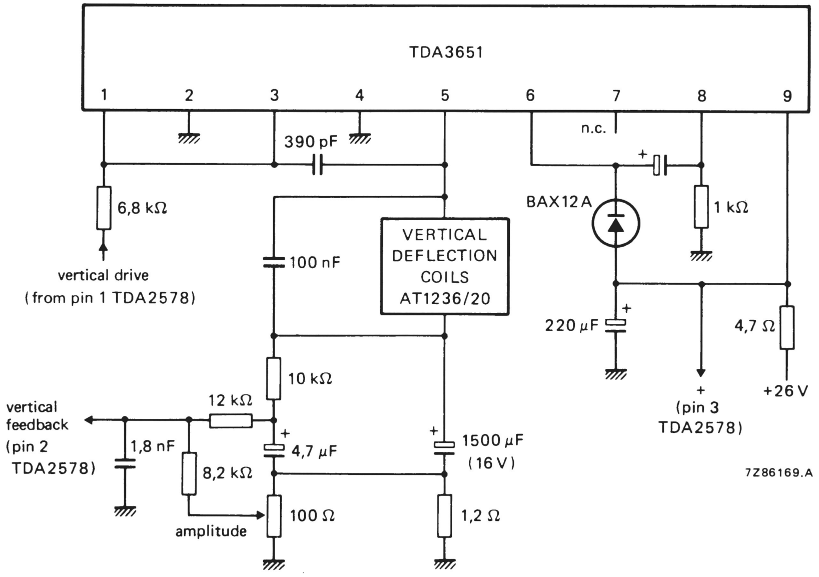
TDA3651
1
2
3
4
5
6
7
8
9
390 pF
n.c.
+
6,8 kΩ
BAX12A
1 kΩ
vertical drive
(from pin 1 TDA2578)
100 nF
VERTICAL
DEFLECTION
COILS
AT1236/20
220 μF
4,7 Ω
+
(pin 3
TDA2578)
+26 V
10 kΩ
vertical
feedback
(pin 2
TDA2578)
12 kΩ
1,8 nF
8,2 kΩ
4,7 μF
1500 μF
(16 V)
7Z86169.A
100 Ω
1,2 Ω
amplitude

Fig. 4 Typical application circuit diagram of the TDA3651 (vertical output), when used in combination with the TDA2578 (see Fig. 5).

Note to deflection coils AT1236/20: L = 29 mH, R = 13,6 Ω; deflection current without overscan is 0,82 A peak-to-peak and EHT voltage is 25 kV.

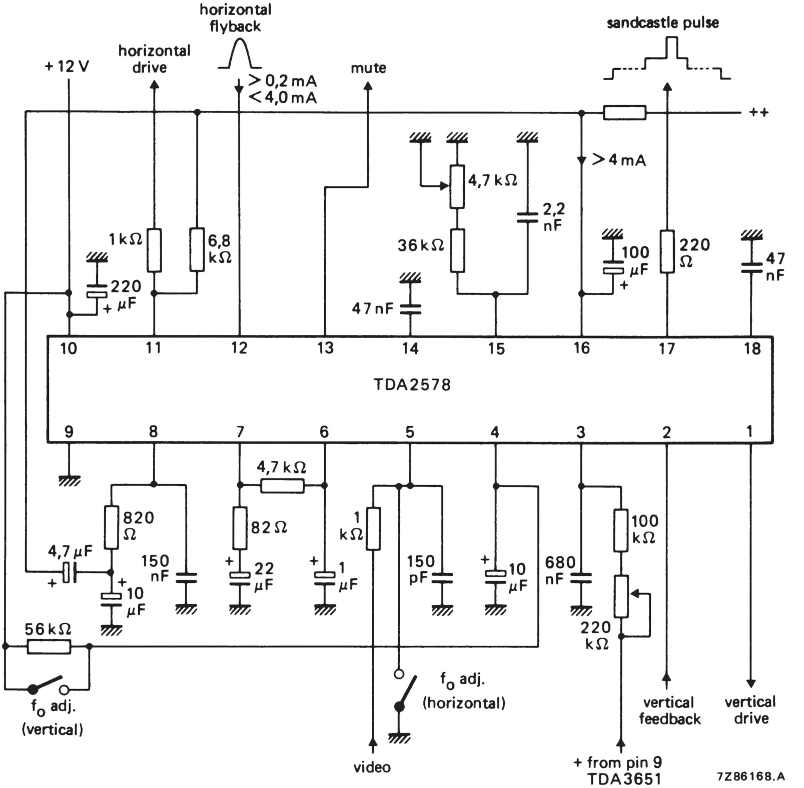
horizontal flyback
horizontal drive
+12 V
> 0,2 mA
< 4,0 mA
mute
sandcastle pulse
++
> 4 mA
4,7 kΩ
2,2 nF
36 kΩ
47 nF
1 kΩ
6,8 kΩ
220 μF
100 μF
220 Ω
47 nF
TDA2578
10
11
12
13
14
15
16
17
18
9
8
7
6
5
4
3
2
1
4,7 kΩ
820 Ω
82 Ω
1 kΩ
100 kΩ
4,7 μF
150 nF
22 μF
1 μF
150 pF
10 μF
680 nF
10 μF
56 kΩ
220 kΩ
f0 adj. (vertical)
f0 adj. (horizontal)
video
+ from pin 9 TDA3651
vertical feedback
vertical drive
7Z86168.A

Fig. 5 Typical application circuit diagram; for combination of the TDA2578 with the TDA3651 see Fig. 4.

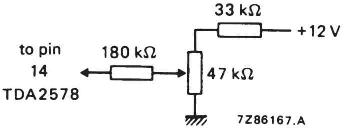
to pin 14 TDA2578
180 kΩ
33 kΩ
+12 V
47 kΩ
7Z86167.A

Fig. 6 Circuit configuration at pin 14 for phase adjustment.

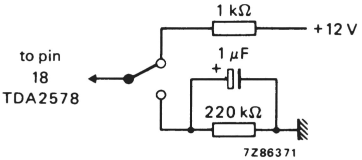
to pin 18 TDA2578
1 kΩ
+12 V
1 μF
220 kΩ
7Z86371

Fig. 7 Circuit configuration at pin 18 for VCR mode.
1 kΩ resistor between pin 18 and + 12 V: without mute function.
220 kΩ between pin 18 and ground: with mute function.

# VERTICAL DEFLECTION CIRCUIT

The TDA3651A;AQ is a vertical deflection output circuit for drive of various deflection systems with deflection currents up to 2 A peak-to-peak.

The circuit incorporates the following functions:

- Driver
- Output stage
- Thermal protection and output stage protection
- Flyback generator
- Voltage stabilizer

## QUICK REFERENCE DATA

| | | | | |
|---|---|---|---|---|
| Supply voltage (pin 9) | $V_P$ | typ. | 26 | V |
| Output current (peak-to-peak value) | $I_{5(p-p)}$ | < | 2 | A |
| Operating junction temperature | $T_j$ | max. | 150 | °C |
| Thermal resistance from junction to mounting base | $R_{th\ j-mb}$ | typ. | 3 | K/W |

## PACKAGE OUTLINES

TDA3651A: 9-lead SIL; plastic power (SOT-131B).

TDA3651AQ: 9-lead SIL bent to DIL; plastic power (SOT-157B).

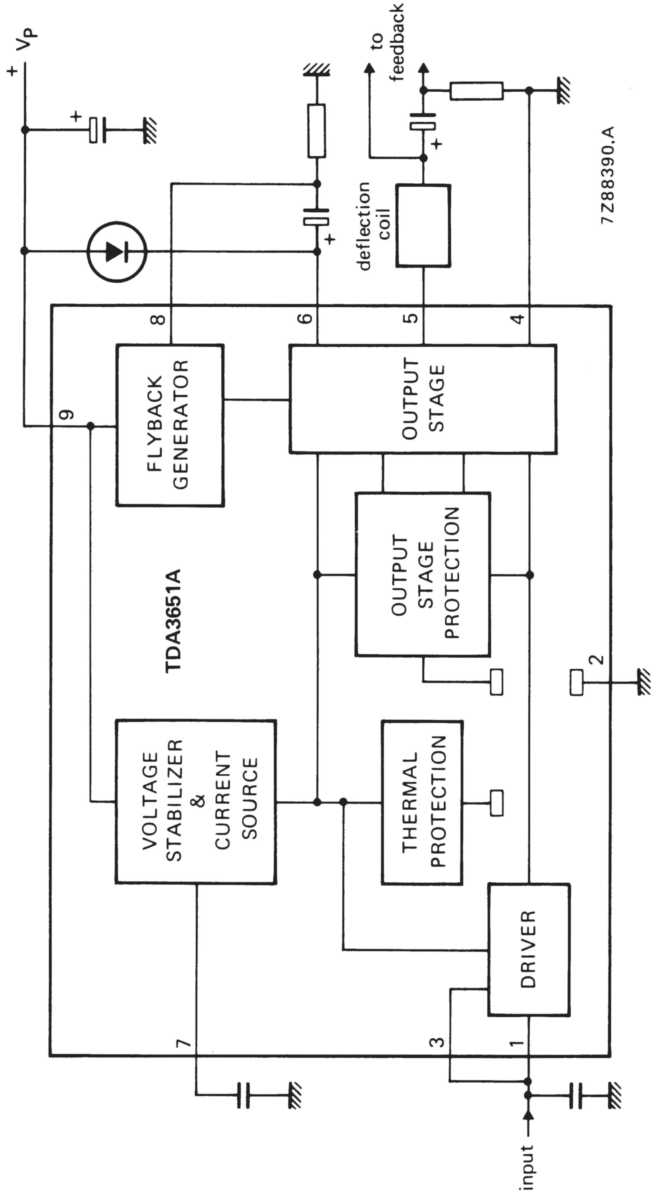
+ VP
+
to feedback
+
deflection coil
+
7Z88390.A
9
8
6
5
4
FLYBACK GENERATOR
OUTPUT STAGE
TDA3651A
OUTPUT STAGE PROTECTION
2
VOLTAGE STABILIZER & CURRENT SOURCE
THERMAL PROTECTION
DRIVER
7
3
1
input

Fig. 1 Block diagram.

## GENERAL DESCRIPTION

### Output stage and protection circuit

Pin 5 is the output pin. The supply for the output stage is fed to pin 6 and the output stage ground is connected to pin 4. The output transistors of the class-B output stage can each deliver 1 A maximum. The 'upper' power transistor is protected against short-circuit currents to ground, whereas, during flyback, the 'lower' power transistor is protected against too high voltages which may occur during adjustments.
Moreover, the output transistors have been given extra solidity by means of special measures in the internal circuit layout.
A thermal protection circuit is incorporated to protect the IC against too high dissipation. This circuit is 'active' at 175 °C and then reduces the deflection current to such a value that the dissipation cannot increase.

### Driver and switching circuit

Pin 1 is the input for the driver of the output stage. The signal at pin 1 is also applied to pin 3 which is the input of a switching circuit. When the flyback starts, this switching circuit rapidly turns off the lower output stage and so limits the turn-off dissipation. It also allows a quick start of the flyback generator. Pin 3 is connected externally to pin 1, in order to allow for different applications in which pin 3 is driven separate from pin 1.

### Flyback generator

The capacitor at pin 6 is charged to a maximum voltage, which is equal to the supply voltage $V_P$ (pin 9), during scan.
When the flyback starts and the voltage at the output pin (pin 5) exceeds the supply voltage (pin 9), the flyback generator is activated. The $V_P$ is connected in series (via pin 8) with the voltage across the capacitor.
The voltage at the supply pin (pin 6) of the output stage will then be maximum twice $V_P$. Lower voltages can be chosen by changing the value of the external resistor at pin 8.

### Voltage stabilizer

The internal voltage stabilizer provides a stabilized supply of 6 V for drive of the output stage, so the drive current of the output stage is not affected by supply voltage variations. The stabilized voltage is available at pin 7.
A decoupling capacitor of 2,2 μF can be connected to this pin.

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | |
|---|---|---|---|
| **Voltages** (pins 4 and 2 externally connected to ground) | | | |
| Output voltage (pin 5) | $V_{5\text{-}4}$ | max. | 50 V |
| Supply voltage (pin 9) | $V_{9\text{-}4} = V_P$ | max. | 50 V |
| Supply voltage output stage (pin 6) | $V_{6\text{-}4}$ | max. | 50 V |
| Input voltage (pins 1 and 3) | $V_{1\text{-}2}; V_{3\text{-}2}$ | max. | $V_P$ |
| **Currents** | | | |
| Repetitive peak output current (pin 5) | $\pm I_{5RM}$ | max. | 1 A |
| Non-repetitive peak output current (pin 5) | $\pm I_{5SM}$ | max. | 1,5 A* |
| Repetitive peak flyback generator output current (pin 8) | $I_{8RM}$ | max. | −1,0 A<br>+1,1 A |
| Non-repetitive peak flyback generator output current (pin 8) | $I_{8SM}$ | max. | −1,5 A<br>+1,6 A* |
| **Temperatures** | | | |
| Storage temperature range | $T_{stg}$ | | −65 to + 150 °C |
| Operating ambient temperature range | $T_{amb}$ | | −25 to + 65 °C |
| Operating junction temperature range | $T_j$ | | −25 to + 150 °C |

## CHARACTERISTICS

$T_{amb} = 25\ ^{o}C$; $V_P = 26$ V; pins 4 and 2 externally connected to ground; unless otherwise specified.

| | | | |
|---|---|---|---|
| Output current (peak-to-peak value) | $I_{5(p\text{-}p)}$ | typ.<br>$<$ | 1,5 A<br>2,0 A |
| Flyback generator output current | $-I_8$ | typ.<br>$<$ | 0,85 A<br>1,1 A |
| Flyback generator output current | $I_8$ | typ.<br>$<$ | 0,75 A<br>1,0 A |
| **Output voltages** | | | |
| Peak voltage during flyback | $V_{5\text{-}4M}$ | $<$ | 50 V |
| Saturation voltage to supply at $-I_5 = 1$ A | $-V_{5\text{-}6sat}$ | typ.<br>$<$ | 2,5 V<br>3,0 V |
| Saturation voltage to ground at $I_5 = 1$ A | $V_{5\text{-}4sat}$ | typ.<br>$<$ | 2,5 V<br>3,0 V |
| Saturation voltage to supply at $-I_5 = 0,75$ A | $-V_{5\text{-}6sat}$ | typ.<br>$<$ | 2,2 V<br>2,7 V |
| Saturation voltage to ground at $I_5 = 0,75$ A | $V_{5\text{-}4sat}$ | typ.<br>$<$ | 2,2 V<br>2,7 V |

---

* Non-repetitive duty factor maximum 3,3%.

| | | | | |
|---|---|---|---|---|
| **Supply** | | | | |
| Supply voltage | $V_{9\text{-}2;\,4}$ | | 10 to 50 | V* |
| Supply voltage output stage | $V_{6\text{-}4}$ | < | 50 | V* |
| Supply current (no load and no quiescent current) | $I_9$ | typ.<br>< | 9<br>12 | mA<br>mA |
| Quiescent current (see Fig. 2) | $I_4$ | typ. | 38<br>25 to 52 | mA<br>mA |
| Variation of quiescent current with temperature | | typ. | −0,04 | mA/K |
| **Flyback generator** | | | | |
| Saturation voltage at $-I_8 = 1{,}1$ A | $V_{9\text{-}8sat}$ | typ.<br>< | 1,6<br>2,1 | V<br>V |
| Saturation voltage at $I_8 = 1$ A | $V_{8\text{-}9sat}$ | typ.<br>< | 2,5<br>3,0 | V<br>V |
| Saturation voltage at $I_8 = 0{,}85$ A | $V_{9\text{-}8sat}$ | typ.<br>< | 1,4<br>1,9 | V<br>V |
| Saturation voltage at $I_8 = 0{,}75$ A | $V_{8\text{-}9sat}$ | typ.<br>< | 2,3<br>2,8 | V<br>V |
| Flyback generator active if: | $V_{5\text{-}9}$ | > | 4 | V |
| Leakage current | $-I_8$ | typ.<br>< | 5<br>100 | μA<br>μA |
| Input current for ± $I_5 = 1$ A | $I_1$ | typ. | 230<br>175 to 380 | μA<br>μA |
| Input voltage during scan | $V_{1\text{-}2}$ | typ. | 1,9<br>0,9 to 2,7 | V<br>V |
| Input current during scan | $I_3$ | | 0,01 to 2,5 | mA |
| Input voltage during scan | $V_{3\text{-}2}$ | | 0,9 to $V_P$ | V |
| Input voltage during flyback | $V_{3\text{-}2}$ | | 0 to 0,2 | V |
| Voltage at pin 7 | $V_{7\text{-}2}$ | typ. | 6,1<br>5,6 to 6,6 | V<br>V |
| Load current of pin 7 | $I_7$ | < | 2 | mA |
| Unloaded voltage at pin 7 during flyback | $V_{7\text{-}2}$ | typ. | 15 | V |
| Junction temperature of switching on the thermal protection | $T_j$ | typ. | 175<br>158 to 192 | °C<br>°C |
| Thermal resistance from junction to mounting base | $R_{th\,j\text{-}mb}$ | typ.<br>< | 3<br>4 | K/W<br>K/W |
| Power dissipation | see Fig. 3 | | | |
| Open loop gain at 1 kHz; $R_{load} = 1$ kΩ | $G_o$ | typ. | 36 | dB |
| Frequency response (−3 dB); $R_{load} = 1$ kΩ | f | typ. | 60 | kHz |

DEVELOPMENT SAMPLE DATA

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* The maximum supply voltage should be chosen such that during flyback the voltage at pin 5 does not exceed 50 V.

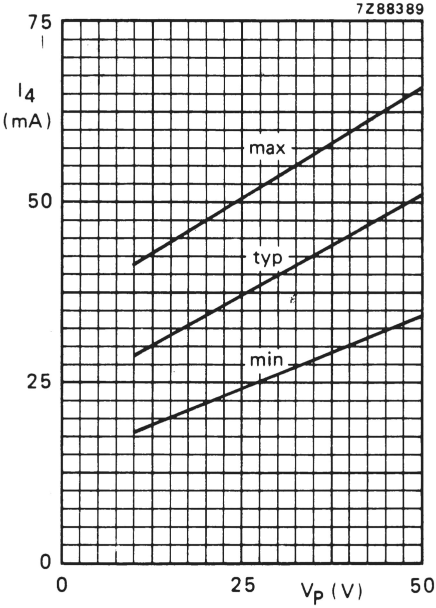

Fig. 2 Quiescent current $I_4$ as a function of supply voltage $V_P$.

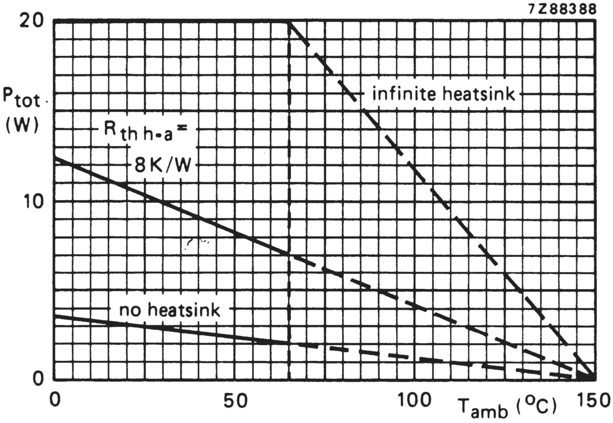

Fig. 3 Power derating curves.

## APPLICATION INFORMATION

The following application data are measured in a typical application as shown in Figs 4 and 5.

| | | | | |
|---|---|---|---|---|
| Deflection current (including 6% overscan) peak-to-peak value | $I_{5(p\text{-}p)}$ | typ. | 0,87 | A |
| Supply voltage | $V_{9\text{-}4}$ | typ. | 26 | V |
| Total supply current | $I_{tot}$ | typ. | 148 | mA |
| Peak output voltage during flyback | $V_{5\text{-}4M}$ | < | 50 | V |
| Saturation voltage to supply | $V_{5\text{-}6sat}$ | typ.<br>< | 2,0<br>2,5 | V<br>V |
| Saturation voltage to ground | $V_{5\text{-}4sat}$ | typ.<br>< | 2,0<br>2,5 | V<br>V |
| Flyback time | $t_{fl}$ | typ.<br>< | 0,95<br>1,2 | ms<br>ms |
| Total power dissipation in IC | $P_{tot}$ | typ. | 2,5 | W |
| Operating ambient temperature | $T_{amb}$ | < | 65 | °C |

DEVELOPMENT SAMPLE DATA

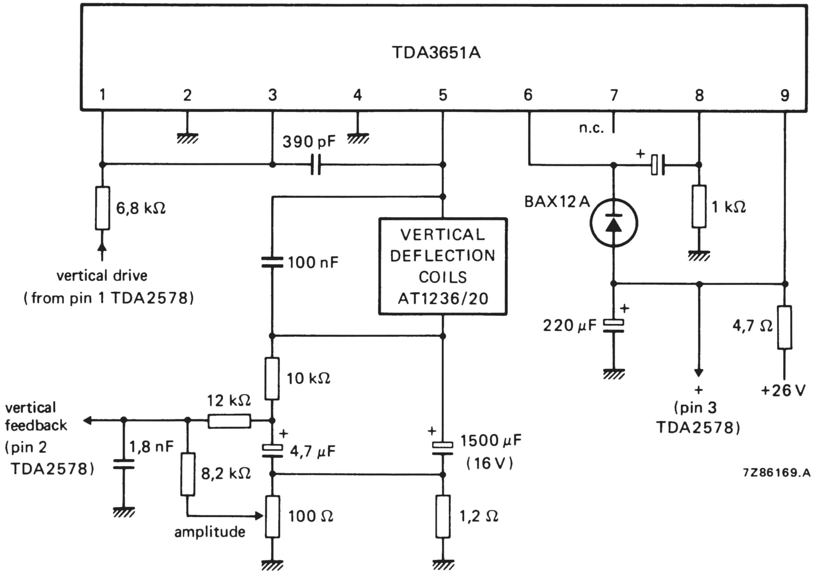
TDA3651A
1
2
3
4
5
6
7
8
9
n.c.
390 pF
6,8 kΩ
vertical drive
(from pin 1 TDA2578)
100 nF
VERTICAL DEFLECTION COILS AT1236/20
BAX12A
1 kΩ
220 µF
4,7 Ω
+
(pin 3 TDA2578)
+26 V
10 kΩ
12 kΩ
vertical feedback
(pin 2 TDA2578)
1,8 nF
8,2 kΩ
4,7 µF
1500 µF
(16 V)
100 Ω
amplitude
1,2 Ω
7Z86169.A

Fig. 4 Typical application circuit diagram of the TDA3651A (vertical output), when used in combination with the TDA2578 (see Fig. 5).

Note to deflection coils AT1236/20: L = 29 mH, R = 13,6 Ω; deflection current without overscan is 0,82 A peak-to-peak and EHT voltage is 25 kV.

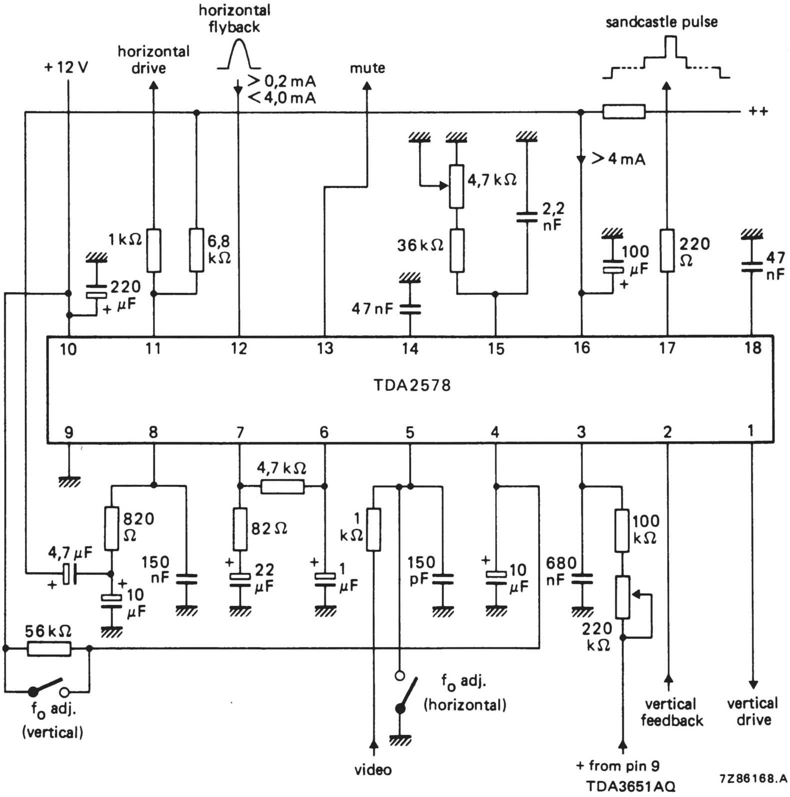
horizontal flyback
sandcastle pulse
+12 V
horizontal drive
> 0,2 mA
< 4,0 mA
mute
++
> 4 mA
4,7 kΩ
2,2 nF
36 kΩ
1 kΩ
6,8 kΩ
220 μF
47 nF
100 μF
220 Ω
47 nF
TDA2578
4,7 kΩ
820 Ω
82 Ω
1 kΩ
4,7 μF
150 nF
22 μF
1 μF
150 pF
10 μF
680 nF
100 kΩ
10 μF
220 kΩ
56 kΩ
f0 adj. (vertical)
f0 adj. (horizontal)
video
+ from pin 9 TDA3651AQ
vertical feedback
vertical drive
7Z86168.A

Fig. 5 Typical application circuit diagram; for combination of the TDA2578 with the TDA3651A see Fig. 4.

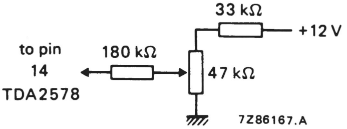
to pin 14 TDA2578
180 kΩ
33 kΩ
+12 V
47 kΩ
7Z86167.A

Fig. 6 Circuit configuration at pin 14 for phase adjustment.

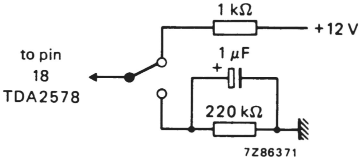
1 kΩ
+12 V
to pin 18 TDA2578
1 μF
220 kΩ
7Z86371

Fig. 7 Circuit configuration at pin 18 for VCR mode.
1 kΩ resistor between pin 18 and + 12 V: without mute function.
220 kΩ between pin 18 and ground: with mute function.

# VERTICAL DEFLECTION CIRCUIT

## GENERAL DESCRIPTION

The TDA3652 is an integrated power output circuit for vertical deflection in systems with deflection currents up to 3 A peak to peak.

### Features

- Driver
- Output stage and protection circuits
- Flyback generator
- Voltage stabilizer

## QUICK REFERENCE DATA

| | | | | |
|---|---|---|---|---|
| Supply voltage (pin 9) | $V_{9\text{-}4} = V_P$ | | 0 to 40 | V |
| Output current (peak-to-peak value) | $I_{5(p\text{-}p)}$ | max. | 3 | A |
| Operating junction temperature | $T_j$ | max. | 150 | °C |
| Thermal resistance from junction to mounting base | $R_{th\ j\text{-}mb}$ | max. | 4 | K/W |

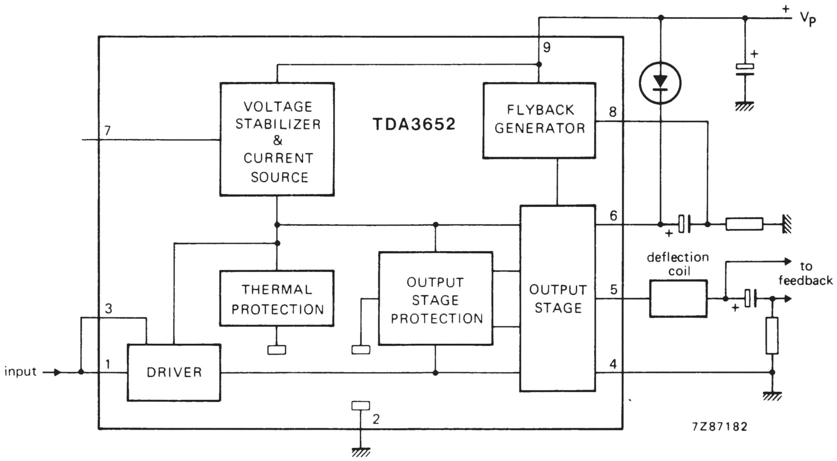
+ $V_P$
9
+
VOLTAGE STABILIZER & CURRENT SOURCE
TDA3652
FLYBACK GENERATOR
8
7
6
+
deflection coil
to feedback
THERMAL PROTECTION
OUTPUT STAGE PROTECTION
OUTPUT STAGE
5
+
3
input
1
DRIVER
4
2
7Z87182

Fig. 1 Block diagram.

## PACKAGE OUTLINES

TDA3652: 9-lead SIL; plastic (SOT-131B).
TDA3652Q: 9-lead SIL bent to DIL; plastic (SOT-157B).

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | |
|---|---|---|---|
| **Voltages** (pins 4 and 2 externally connected to ground) | | | |
| Output voltage (pin 5) | $V_{5\text{-}4}$ | | 0 to 50 V |
| Supply voltage (pin 9) | $V_{9\text{-}4} = V_P$ | | 0 to 40 V |
| Supply voltage output stage (pin 6) | $V_{6\text{-}4}$ | | 0 to 50 V |
| Driver input voltage (pin 1) | $V_{1\text{-}2}$ | | 0 to $V_P$ V* |
| Switching circuit input voltage (pin 3) | $V_{3\text{-}2}$ | | 0 to 5,6 V |
| **Currents** | | | |
| Repetitive peak output current (pin 5) | $\pm I_{5RM}$ | max. | 1,5 A |
| Non-repetitive peak output current (pin 5) | $\pm I_{5SM}$ | max. | 3 A** |
| Repetitive peak flyback generator output current (pin 8) | $I_{8RM}$ | max. | −1,5 A<br>+1,6 A |
| Non-repetitive peak flyback generator output current (pin 8) | $\pm I_{8SM}$ | max. | 3 A** |
| **Temperatures** | | | |
| Storage temperature range | $T_{stg}$ | | −65 to +150 °C |
| Operating ambient temperature range | $T_{amb}$ | | −25 to +65 °C |
| Operating junction temperature range | $T_j$ | | −25 to +150 °C |

---

* The maximum input voltage should not exceed the supply voltage ($V_P$ at pin 9). In most applications pin 1 is connected to pin 3; the maximum input voltage should then not exceed 5,6 V.

** Non-repetitive duty factor maximum 3,3%.

## CHARACTERISTICS

$V_P$ = 26 V; $T_{amb}$ = 25 °C; pins 4 and 2 externally connected to ground; unless otherwise specified

| parameter | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| **Supply** | | | | | |
| Supply voltage; pin 9 | $V_P$ | 10 | – | 40 | V* |
| Supply voltage output stage; pin 6 | $V_{6\text{-}4}$ | – | – | 50 | V* |
| Supply current (no load and no quiescent current); pin 9 | $I_P$ | – | 9 | 12 | mA |
| Quiescent current (see Fig. 2) | $I_4$ | 25 | 40 | 65 | mA |
| Variation of quiescent current with temperature | $\Delta I_4$ | – | –0,04 | – | mA/K |
| **Output current** | | | | | |
| Output current (pin 5) (peak-to-peak value) | $I_{5(p\text{-}p)}$ | – | 2,5 | 3,0 | A |
| Output current flyback generator (pin 8) | $-I_8$ | – | 1,35 | 1,6 | A |
| Output current flyback generator (pin 8) | $I_8$ | – | 1,25 | 1,5 | A |
| **Output voltage** | | | | | |
| Peak voltage during flyback | $V_{5\text{-}4M}$ | – | – | 50 | V |
| Saturation voltage to supply at $-I_5$ = 1,5 A | $-V_{5\text{-}6sat}$ | – | 2,5 | 3,0 | V |
| Saturation voltage to ground at $I_5$ = 1,5 A | $V_{5\text{-}4sat}$ | – | 2,5 | 3,0 | V |
| Saturation voltage to supply at $-I_5$ = 1 A | $-V_{5\text{-}6sat}$ | – | 2,2 | 2,7 | V |
| Saturation voltage to ground at $I_5$ = 1 A | $V_{5\text{-}4sat}$ | – | 2,2 | 2,7 | V |
| **Flyback generator** | | | | | |
| Saturation voltage at $-I_8$ = 1,6 A | $V_{9\text{-}8sat}$ | – | 1,6 | 2,1 | V |
| Saturation voltage at $I_8$ = 1,5 A | $V_{8\text{-}9sat}$ | – | 2,5 | 3,0 | V |
| Saturation voltage at $-I_8$ = 1,1 A | $V_{9\text{-}8sat}$ | – | 1,4 | 1,9 | V |
| Saturation voltage at $I_8$ = 1 A | $V_{8\text{-}9sat}$ | – | 2,3 | 2,8 | V |
| Flyback generator active if: | $V_{5\text{-}9}$ | 4 | – | – | V |
| Leakage current at pin 8 | $-I_8$ | – | 5 | 100 | µA |
| Input current for $I_5$ = 4 A at pin 1 (peak-to-peak value) | $I_{1(p\text{-}p)}$ | 190 | 240 | 400 | µA |
| Input voltage during scan (pin 1) | $V_{1\text{-}2}$ | 1,3 | 2,0 | 3,5 | V |
| Input current during scan (pin 3) | $I_3$ | 0,01 | – | 2,5 | mA |

* The maximum supply voltage should be chosen such that during flyback the voltage at pin 5 does not exceed 50 V.

**CHARACTERISTICS** (continued)

| parameter | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| **Flyback generator** (continued) | | | | | |
| Input voltage during scan (pin 3) | $V_{3\text{-}2}$ | 0,9 | – | 5,6 | V |
| Input voltage during flyback (pin 3) | $V_{3\text{-}2}$ | 0 | – | 0,2 | V |
| **General data** | | | | | |
| Junction temperature of switching on the thermal protection | $T_j$ | 158 | 175 | 192 | °C |
| Thermal resistance from junction to mounting base | $R_{th\ j\text{-}mb}$ | – | – | 4 | K/W |
| Total power dissipation | $P_{tot}$ | | see Fig. 3 | | |
| Open-loop gain at 1 kHz | $G_o$ | – | 36 | – | dB |
| Frequency response (–3 dB) at $R_L$ = 1 kΩ | f | – | 50 | – | kHz |

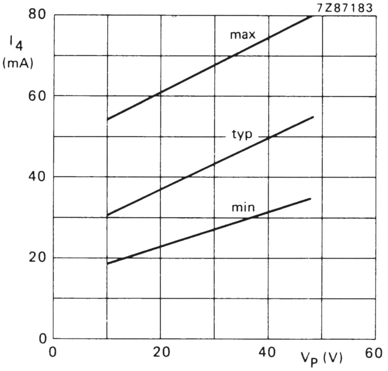

Fig. 2 Quiescent current ($I_4$) as a function of supply voltage ($V_P$).

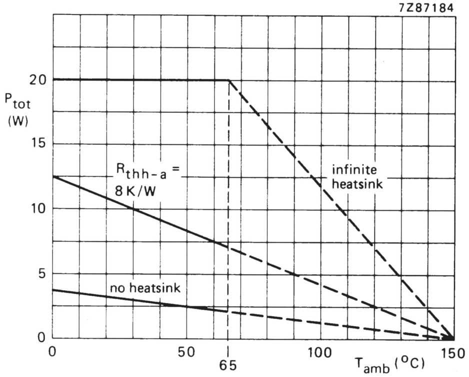

Fig. 3 Power derating curve.

## APPLICATION INFORMATION

The function is described against the corresponding pin number.

### 1. Driver

This is the input for the driver of the output stage.

### 2. Negative supply (ground)

### 3. Switching circuit

This pin is normally connected externally to pin 1. It is also possible to use this pin to drive the switching circuit for different applications. This switching circuit rapidly turns off the lower output stage at the end of scan and also allows for a quick start of the flyback generator.

### 4. Output stage ground

### 5 and 6. Output stage and protection circuits

Pin 5 is the output pin and pin 6 is the output stage supply pin. The output stage is a class-B type with each transistor capable of delivering 1,5 A maximum. The "upper" output transistor is protected against short-circuit currents to ground. The base of the "lower" power transistor is connected to ground during flyback and so it is protected against too high flyback pulses which may occur during adjustments. In addition the output transistors are protected by a special layout of the internal circuit. The circuit is protected thermally against excessive dissipation by a circuit which operates at temperatures of 175 °C upwards causing the output current to drop to a value such that the dissipation cannot increase.

### 7. Voltage stabilizer

The internal voltage stabilizer provides a stabilized supply voltage of 6 V for drive of the output stage, so the drive current is not influenced by the various voltages of different applications.

### 8 and 9. Flyback generator

Pin 8 is the output pin of the flyback generator. Depending on the value of the external resistor at pin 8, the capacitor at pin 6 will be charged to a fixed level during the scan period. The maximum height of this level is equal to the supply voltage at pin 9 ($V_P$). When the flyback starts and the flyback pulse at pin 5 exceeds the supply voltage, the flyback generator is activated and then the supply voltage is connected in series (via pin 8) with the voltage across the capacitor. The voltage at the supply pin (pin 6) of the output stage will then be not more than twice the supply voltage.

This information is derived from development samples made available for evaluation. It does not necessarily imply that the device will go into regular production.

# PAL SYNCHRONIZATION PROCESSOR FOR VIDEO RECORDERS

## GENERAL DESCRIPTION

The TDA3700A is a monolithic integrated circuit for PAL synchronization processing in video recorders.

### Features

- Sync separator with noise inverter
- Phase detector with 2 time constants for oscillator synchronization
- Automatic identification of normal synchronization signals (625 lines referred to CCIR)
- Colour subcarrier oscillator with separate output (625 kHz sinewave) and 1:40 divider
- Separate horizontal and vertical coincidence detectors
- Internal production of a complete standard synchronization pulse
- Vertical synchronization pulse output
- Output for indicating detection of first or second half-picture lines
- Burst gate pulse output (externally adjustable phase relationship)
- H/8 signal output and H/8 signal correction/inversion inputs
- Record (REC/TV; REC/VCR)/playback (PB) selector

## QUICK REFERENCE DATA

| | | | |
|---|---|---|---|
| Supply voltage (pin 22) | $V_P = V_{22\text{-}23}$ | typ. | 12 V |
| Supply current (pin 22) | $I_P = I_{22}$ | typ. | 85 mA |
| **Sync separator** | | | |
| Sync pulse amplitude (peak-to-peak value) | $V_{4\text{-}23(p\text{-}p)}$ | typ. | 0,3 V |
| **Phase detector** | | | |
| Catching range | $\Delta f$ | typ. | ±5 % |
| **Vertical sync pulse** | | | |
| Output voltage (peak-to-peak value) | $V_{27\text{-}23}$ | min. | 10 V |
| **Half-picture line identification pulse** (pin 26) | | | |
| Output voltage | | | |
| 1st half picture | $V_{26\text{-}23}$ | min. | 10 V |
| 2nd half picture | $V_{26\text{-}23}$ | max. | 1 V |
| **H/8 signal output** (pin 20) | | | |
| Amplitude of output pulse (peak-to-peak value) | $V_{20\text{-}23(p\text{-}p)}$ | min. | 10 V |

## PACKAGE OUTLINE

28-lead DIL; plastic (SOT-117).

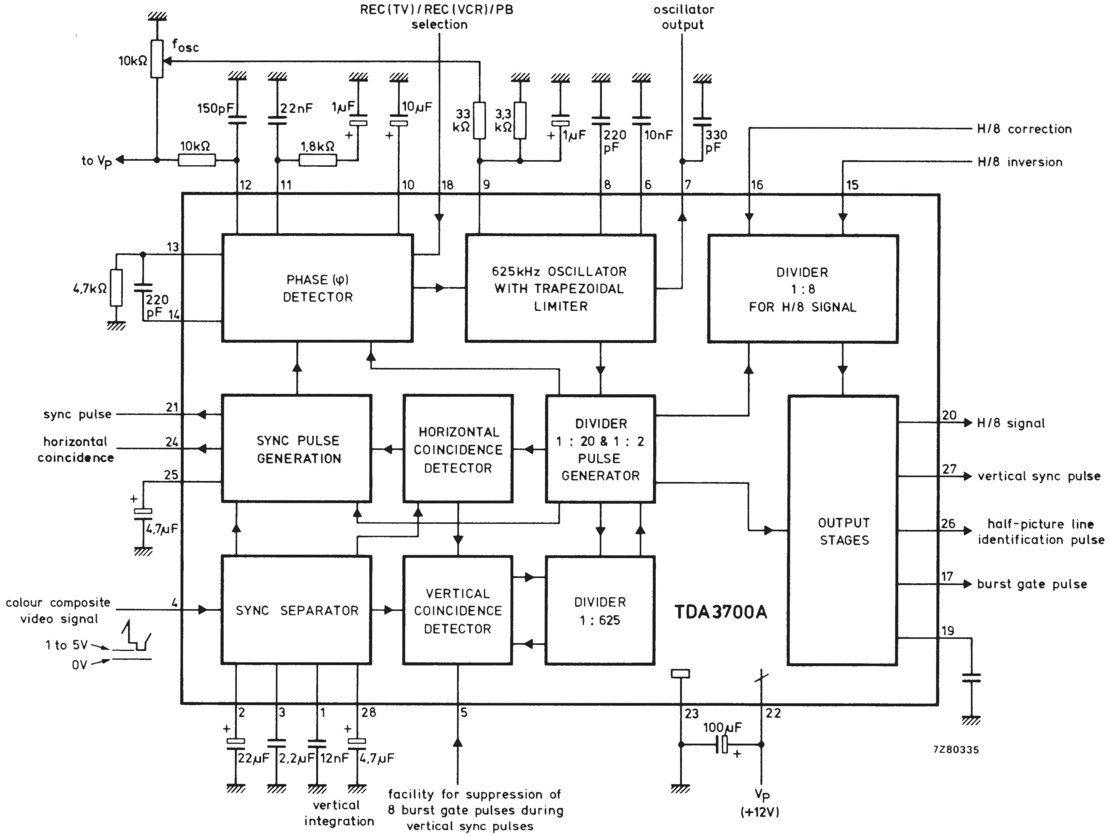
REC(TV)/REC(VCR)/PB selection
oscillator output
f<sub>osc</sub>
10kΩ
150pF
22nF
1µF
10µF
33 kΩ
3,3 kΩ
1µF
220 pF
10nF
330 pF
to V<sub>P</sub>
10kΩ
1,8kΩ
12
11
10
18
9
8
6
7
16
15
H/8 correction
H/8 inversion
13
14
4,7kΩ
220 pF
PHASE (φ) DETECTOR
625kHz OSCILLATOR WITH TRAPEZOIDAL LIMITER
DIVIDER 1 : 8 FOR H/8 SIGNAL
sync pulse
21
horizontal coincidence
24
25
4,7µF
SYNC PULSE GENERATION
HORIZONTAL COINCIDENCE DETECTOR
DIVIDER 1 : 20 & 1 : 2 PULSE GENERATOR
OUTPUT STAGES
20
H/8 signal
27
vertical sync pulse
26
half-picture line identification pulse
17
burst gate pulse
19
colour composite video signal
4
1 to 5V
0V
SYNC SEPARATOR
VERTICAL COINCIDENCE DETECTOR
DIVIDER 1 : 625
TDA3700A
2
3
1
28
22µF
2,2µF
12nF
4,7µF
vertical integration
5
facility for suppression of 8 burst gate pulses during vertical sync pulses
23
22
100µF
V<sub>P</sub> (+12V)
7Z80335

Fig. 1 Block diagram.

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | | |
|---|---|---|---|---|
| Supply voltage range (pin 22) | $V_P = V_{22\text{-}23}$ | max. | 13,2 | V |
| Voltage range at pins 4, 12, 15, 16, 18, 24 to pin 23 (ground) | $V_{n\text{-}23}$ | | 0 to $V_P$ | V |
| Voltage range at pin 9 | $V_{9\text{-}23}$ | | 0,3 $V_P$ to 0,7 $V_P$ | V |
| Voltage at pin 5 | $V_{5\text{-}23}$ | min. | 0 | V |
| Currents | | | | |
| at pins 17, 20, 21, 24, 26, 27 | $I_n$ | max. | 20 | mA |
| at pin 5 | $I_5$ | max. | 50 | µA |
| at pin 7 | $\pm I_7$ | max. | 1 | mA |
| Total power dissipation | $P_{tot}$ | max. | 1,5 | W |
| Storage temperature range | $T_{stg}$ | | −25 to + 125 | °C |
| Operating ambient temperature range | $T_{amb}$ | | 0 to + 70 | °C |

## CHARACTERISTICS

$V_P = V_{22\text{-}23} = 12$ V; $T_{amb} = 25\ ^oC$; measured in Fig. 1; unless otherwise specified

| parameter | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| **Supply** (pin 22) | | | | | |
| Supply voltage range | $V_P = V_{22\text{-}23}$ | 9,6 | – | 13,2 | V |
| Supply current | $I_P = I_{22}$ | – | 85 | – | mA |
| **Sync separator** (pin 4) | | | | | |
| Colour composite video input voltage (note 1) (peak-to-peak value) | $V_{4\text{-}23(p\text{-}p)}$ | – | 1 | – | V |
| Sync pulse amplitude (peak-to-peak value) | $V_{4\text{-}23(p\text{-}p)}$ | 0,1 | 0,3 | 0,6 | V |
| Slicing level, relative to sync pulse amplitude | | – | 50 | – | % |
| Output voltage (peak-to-peak value) | $V_{21\text{-}23(p\text{-}p)}$ | 10 | – | – | V |
| Output current (peak-to-peak value) | $I_{21(p\text{-}p)}$ | – | – | 5 | mA |
| Delay between signal at input pin 4 and sync pulse at output pin 21 (note 2) | $t_d$ | – | 0,4 | – | μs |
| Phase adjustment control (pin 12) | | – | ± 1 | – | μs |
| **Phase detector** | | | | | |
| D.C. control voltages | | | | | |
| pin 10 | $V_{10\text{-}23}$ | – | 3 | – | V |
| pin 11 | $V_{11\text{-}23}$ | – | $V_{10\text{-}23}$ | – | V |
| Catching range | $\Delta f$ | – | ± 5 | – | % |
| Control sensitivity (note 3) | | – | 4,25 | – | kHz/μs |
| **625 kHz oscillator** | | | | | |
| Output frequency with $C_{osc} = 220$ pF (pin 8); $R_{osc} = 3{,}6\ k\Omega$ (pin 9) at pin 7 (note 4) | $f_o$ | 575 | 625 | 675 | kHz |
| Output sinewave ($C_{7\text{-}23} = 330$ pF) (peak-to-peak value) | $V_{7\text{-}23(p\text{-}p)}$ | – | 3,2 | – | V |
| D.C. output voltage | $V_{7\text{-}23}$ | – | 6,0 | – | V |
| 2nd harmonic suppression | $\alpha_{2nd}$ | 35 | – | – | dB |
| 3rd harmonic suppression | $\alpha_{3rd}$ | 30 | – | – | dB |
| **Horizontal coincidence detector** | | | | | |
| D.C. output voltage | | | | | |
| no coincidence; $I_{24} = 5$ mA | $V_{24\text{-}23}$ | – | – | 2 | V |
| coincidence | $V_{24\text{-}23}$ | – | 12 | – | V |

| parameter | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| **Vertical sync pulse** (note 5) | | | | | |
| Output voltage (peak-to-peak value) | $V_{27\text{-}23(p\text{-}p)}$ | 10 | – | – | V |
| Output current (peak-to-peak value) | $I_{27(p\text{-}p)}$ | – | – | 4,5 | mA |
| Duration of internally generated output pulse | $t_p$ | – | 160 | – | μs |
| Delay between input signal at pin 4 and start of output pulse at pin 27 | $t_d$ | – | 11 | – | μs |
| Duration of the separated vertical sync pulse | $t_p$ | – | 190 | – | μs |
| Delay between input signal at pin 4 and start of output pulse at pin 27 | $t_d$ | – | 12 | – | μs |
| **Half-picture line identification pulse** (pin 26) | | | | | |
| Output voltage | | | | | |
| 1st half picture | $V_{26\text{-}23}$ | 10 | – | – | V |
| 2nd half picture | $V_{26\text{-}23}$ | – | – | 1 | V |
| Output current (peak-to-peak value) | $I_{26(p\text{-}p)}$ | – | – | 4,5 | mA |
| Duration of output pulse | $t_p$ | – | 20 | – | ms |
| **Burst gate pulse** (pin 17) | | | | | |
| Amplitude of output pulse (peak-to-peak value) | $V_{17\text{-}23(p\text{-}p)}$ | 10 | – | – | V |
| Output current (peak-to-peak value) | $I_{17(p\text{-}p)}$ | – | – | 5 | mA |
| Duration of output pulse | $t_p$ | – | 4 | – | μs |
| Delay between rising edge of horizontal sync pulse at pin 4 and rising edge of gate pulse at pin 17 | | | | | |
| without external capacitor (pin 19) | $t_d$ | – | 5,1 | – | μs |
| with external capacitor (pin 19) | $\Delta t_d/\Delta C$ | – | 3 | – | ns/pF |
| **H/8 signal output** (pin 20) | | | | | |
| Amplitude of output pulse (peak-to-peak value) | $V_{20\text{-}23(p\text{-}p)}$ | 10 | – | – | V |
| Output current (peak-to-peak value) | $I_{20(p\text{-}p)}$ | – | – | 5 | mA |
| Duration of output pulse at $V_{15\text{-}23} = V_{16\text{-}23} > 5$ V | $t_p$ | – | 256 | – | μs |
| Delay between rising edge of horizontal sync pulse at pin 4 and rising edge of H/8 at pin 20 | $t_d$ | – | – | 2,5 | μs |
| H/8 signal correction (note 6) | | | | | |
| input voltage for 'correction' | $V_{16\text{-}23}$ | – | – | 2 | V |
| input voltage for 'no correction' | $V_{16\text{-}23}$ | 5 | – | – | V |
| H/8 signal inversion | | | | | |
| input voltage for 'inversion' | $V_{15\text{-}23}$ | – | – | 2 | V |
| input voltage for 'no inversion' | $V_{15\text{-}23}$ | 5 | – | – | V |

**CHARACTERISTICS** (continued)

| parameter | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| **REC (TV)/REC (VCR)/PB selection** | | | | | |
| REC (TV) | | | | | |
| input voltage | $V_{18\text{-}23}$ | – | – | 2 | V |
| input current ($V_{18\text{-}23}$ = 2 V) | $I_{18}$ | – | – | 200 | μA |
| REC (VCR) | | | | | |
| input voltage | $V_{18\text{-}23}$ | 4 | – | 8 | V |
| input current ($V_{18\text{-}23}$ = 8 V) | $I_{18}$ | – | – | 1 | mA |
| PB | | | | | |
| input voltage | $V_{18\text{-}23}$ | 10 | – | – | V |
| input current ($V_{18\text{-}23}$ = 12 V) | $I_{18}$ | – | – | 2 | mA |

**Notes to characteristics**

1. The sync separator input signal is shown in Fig. 2.

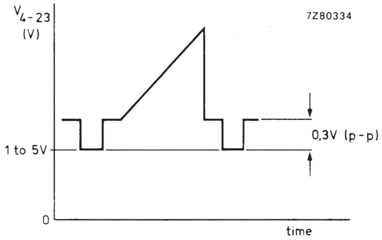

Fig. 2 Colour composite video input signal at pin 4.

2. The internally produced standard sync pulse is available at pin 21 when: horizontal and vertical coincidence is detected, that is, a standard input signal is applied to pin 4 and the record/playback selector is in the record mode.
3. The control sensitivity of the phase detector depends on the horizontal frequency.
4. Balance of the oscillator output frequency is achieved when pins 10 and 11 are short-circuited.
5. The vertical sync pulse is also available without application of the colour composite video signal provided the record/playback selector is in the record mode.
6. During active correction of the H/8 signal one of 8 input pulses of the 1:8 divider circuit will be rejected in a time interval of 4 half-picture lines.

## APPLICATION INFORMATION

DEVELOPMENT SAMPLE DATA

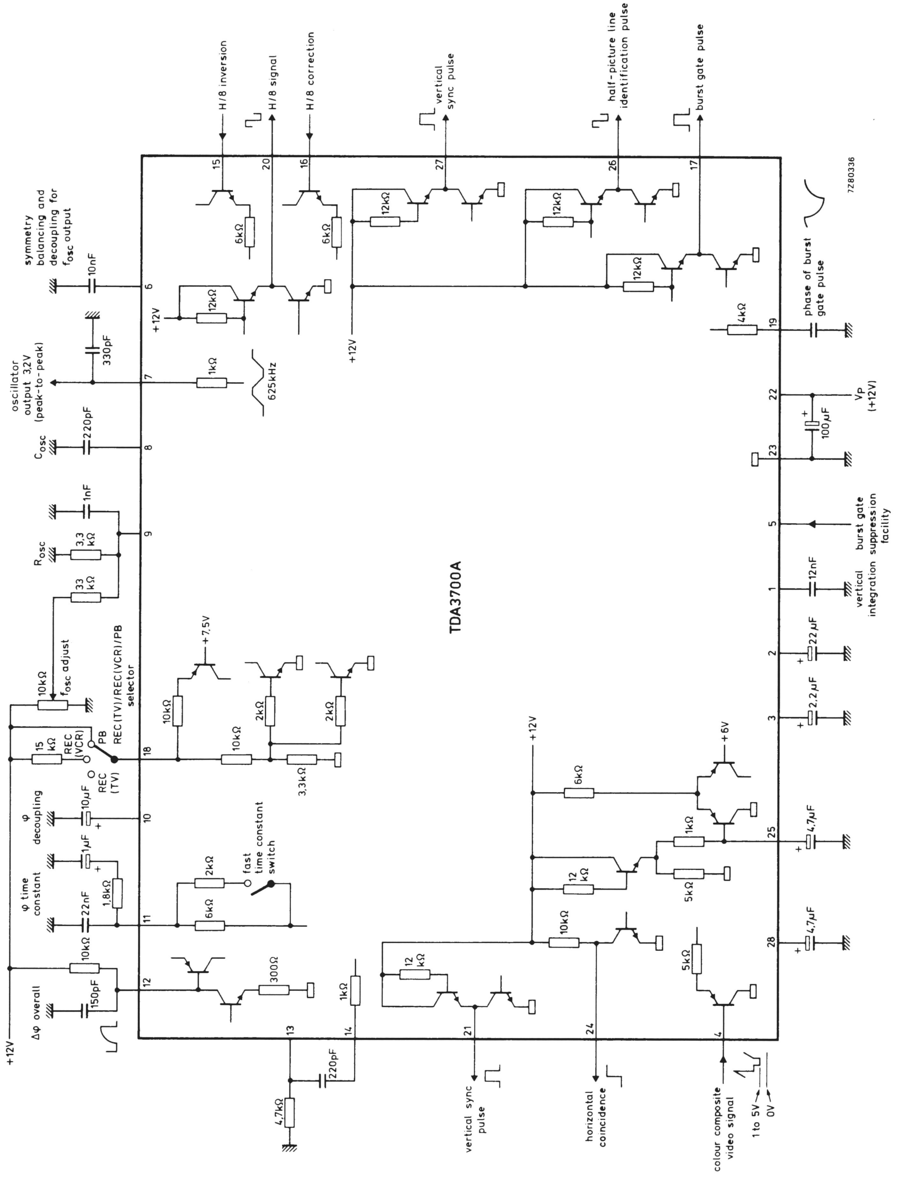
TDA3700A
+12V
Δφ overall
150pF
10kΩ
12
300Ω
φ time constant
22nF
1μF
1,8kΩ
11
6kΩ
2kΩ
fast time constant switch
φ decoupling
10μF
10
REC (TV)
REC (VCR)
PB
REC(TV)/REC(VCR)/PB selector
15 kΩ
18
10kΩ
+7,5V
2kΩ
3,3kΩ
10kΩ
f<sub>osc</sub> adjust
33 kΩ
R<sub>osc</sub>
3,3 kΩ
1nF
9
C<sub>osc</sub>
220pF
8
oscillator output 3,2V (peak-to-peak)
330pF
1kΩ
7
625kHz
symmetry balancing and decoupling for f<sub>osc</sub> output
10nF
6
12kΩ
6kΩ
H/8 inversion
15
H/8 signal
20
H/8 correction
16
vertical sync pulse
27
half-picture line identification pulse
26
burst gate pulse
17
4kΩ
19
phase of burst gate pulse
22
V<sub>P</sub> (+12V)
100μF
23
burst gate suppression facility
5
vertical integration
12nF
1
22μF
2
2,2μF
3
+6V
+12V
25
4,7μF
28
1kΩ
5kΩ
12 kΩ
13
4,7kΩ
220pF
14
1kΩ
12 kΩ
21
vertical sync pulse
24
horizontal coincidence
4
colour composite video signal
1 to 5V
0V
7Z80336

Fig. 3 Application circuit diagram.

# CHROMINANCE SIGNAL/MIXER FOR VIDEO RECORDERS

## GENERAL DESCRIPTION

The TDA3710 is a monolithic integrated circuit for chrominance signal processing in video recorders.

### Features

- Automatic gain controlled preamplifier with record/playback selection
- Signal mixer with balancing stage for phase inversion of chrominance signal
- H/8-control for subcarrier phase inversion
- Amplifier with record/playback selected burst pre- and de-emphasis
- Output stage for the 625 kHz chrominance signal, with facility for being disabled by colour killer, record/playback mode switch and external track sensing circuit
- Amplitude detector with automatic gain control for the preamplifier
- 4,43 MHz voltage controlled oscillator (VCO) for recording and 4,43 MHz local oscillator for playback
- Phase discriminator controlled synchronization of the voltage controlled oscillator
- Subcarrier mixer, disabled for SECAM operation
- H/2 demodulator for the production of PAL identification and colour killing signals
- Flip-flop for PAL identification
- Burst pulse stage for the production of non-delayed (BK1) and delayed (BK2) keying pulses
- Colour killing stage with hysteresis and heterodyned H/2 signal
- Threshold voltage detector for SECAM operation or forced colour on/off
- Voltage stabilization with external reference voltage (5,6 V)
- Internal record/playback and PAL/SECAM selection.

## QUICK REFERENCE DATA

| | | | | |
|---|---|---|---|---|
| Supply voltage (pin 10) | $V_P = V_{10\text{-}16}$ | typ. | 10 | V |
| Supply current (pin 10) | $I_P = I_{10}$ | typ. | 61 | mA |
| **Inputs** | | | | |
| Chrominance signal | | | | |
| 4,43 MHz for record (peak-to-peak value) | $V_{2\text{-}16(p\text{-}p)}$ | typ. | 200 | mV |
| 625 kHz for playback (peak-to-peak value) | $V_{1\text{-}16(p\text{-}p)}$ | typ. | 200 | mV |
| **Outputs** | | | | |
| Chrominance signal | | | | |
| 4,43 MHz (peak-to-peak value) | $V_{23\text{-}16(p\text{-}p)}$ | typ. | 470 | mV |
| 625 kHz (peak-to-peak value) | $V_{26\text{-}16(p\text{-}p)}$ | typ. | 2 | V |

## PACKAGE OUTLINE

28-lead DIL; plastic (SOT-117).

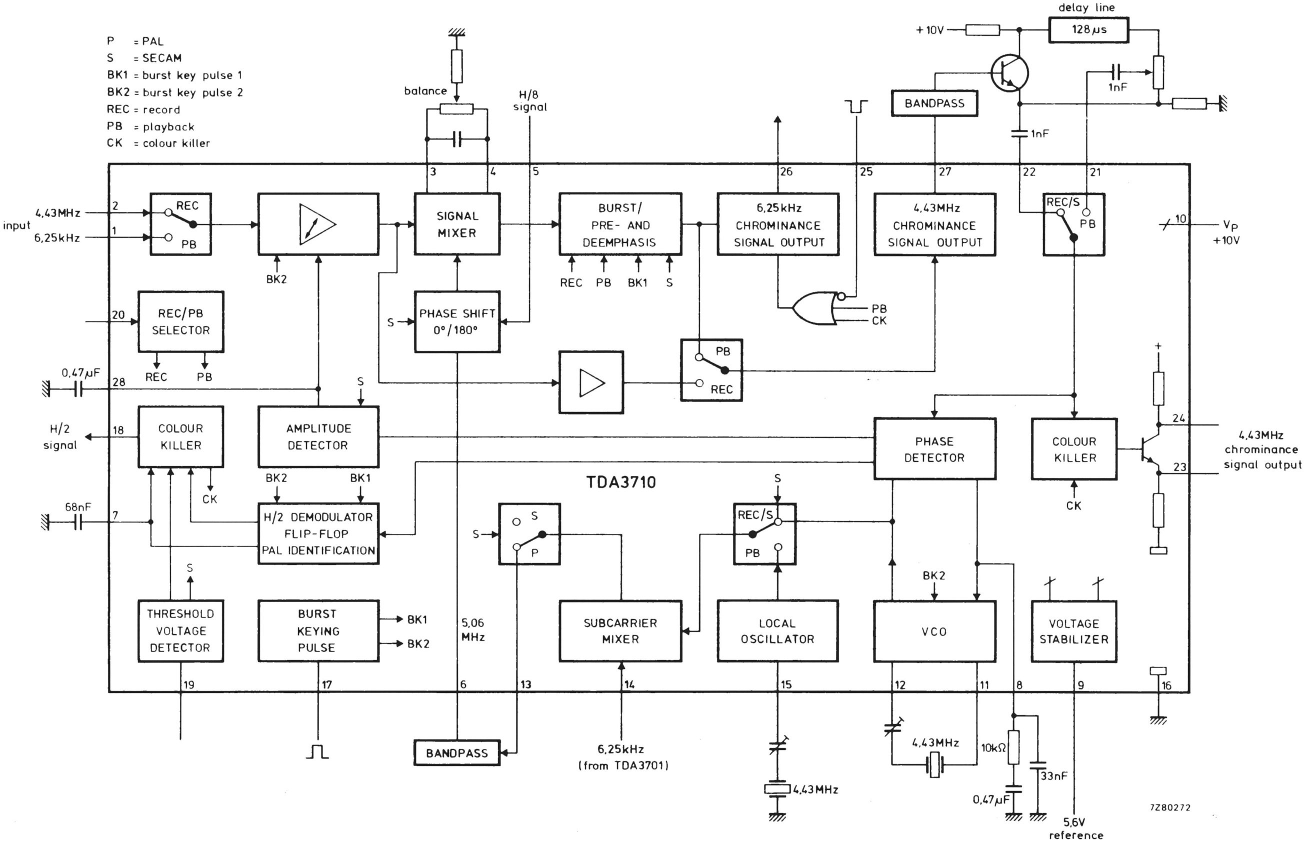
P = PAL
S = SECAM
BK1 = burst key pulse 1
BK2 = burst key pulse 2
REC = record
PB = playback
CK = colour killer
balance
H/8 signal
delay line
128 μs
+10V
1nF
1nF
BANDPASS
input
4,43MHz
6,25kHz
REC
PB
BK2
SIGNAL MIXER
BURST/ PRE- AND DEEMPHASIS
REC
PB
BK1
S
6,25kHz CHROMINANCE SIGNAL OUTPUT
4,43MHz CHROMINANCE SIGNAL OUTPUT
REC/S
PB
VP
+10V
REC/PB SELECTOR
REC
PB
PHASE SHIFT 0°/180°
S
PB
CK
PB
REC
0,47μF
S
H/2 signal
COLOUR KILLER
AMPLITUDE DETECTOR
PHASE DETECTOR
COLOUR KILLER
CK
+
4,43MHz chrominance signal output
BK2
BK1
CK
TDA3710
68nF
H/2 DEMODULATOR FLIP-FLOP PAL IDENTIFICATION
S
S
P
REC/S
PB
S
BK2
S
THRESHOLD VOLTAGE DETECTOR
BURST KEYING PULSE
BK1
BK2
5,06 MHz
SUBCARRIER MIXER
LOCAL OSCILLATOR
VCO
VOLTAGE STABILIZER
BANDPASS
6,25kHz (from TDA3701)
4,43MHz
4,43MHz
10kΩ
33nF
0,47μF
5,6V reference
7Z80272
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28

Fig. 1 Block diagram.

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | | |
|---|---|---|---|---|
| Supply voltage (pin 10) | $V_P = V_{10\text{-}16}$ | max. | 13,2 | V |
| Voltage range at pins 1, 2, 5, 7, 8, 9, 17, 19, 20, 21, 22, 25 to pin 16 (ground) | $V_{n\text{-}16}$ | | 0 to $V_P$ | V |
| Voltage ranges | | | | |
| at pins 3, 4* | $V_{3,\,4\text{-}16}$ | | 3 to 6 | V |
| at pin 6* | $V_{6\text{-}16}$ | | 0 to 5 | V |
| at pin 11* | $V_{11\text{-}16}$ | | 1,5 to 4 | V |
| at pin 14* | $V_{14\text{-}16}$ | | 0 to 3 | V |
| at pin 15* | $V_{15\text{-}16}$ | | 0 to 8 | V |
| at pin 24 | $V_{24\text{-}16}$ | | 5 to $V_P$ | V |
| Voltages | | | | |
| at pin 13 | $V_{13\text{-}16}$ | max. | 9 | V |
| at pin 23 | $V_{23\text{-}16}$ | max. | 7 | V |
| Currents | | | | |
| at pins 12, 18 | $-I_{12,18}$ | max. | 2 | mA |
| at pins 13, 26, 27 | $-I_{13,\,26,\,27}$ | max. | 5 | mA |
| at pin 23 | $-I_{23}$ | max. | 3 | mA |
| Total power dissipation | $P_{tot}$ | max. | 2 | W |
| Storage temperature range | $T_{stg}$ | | −55 to +150 | °C |
| Operating ambient temperature range | $T_{amb}$ | | 0 to +70 | °C |

DEVELOPMENT SAMPLE DATA

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* Measured with $V_{9\text{-}16} = 5{,}6$ V and applied supply voltage.

## CHARACTERISTICS

$V_P = V_{10\text{-}16} = 10$ V; $V_{9\text{-}16} = 5{,}6$ V; $T_{amb} = 25$ °C; unless otherwise specified

| parameter | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| **Supply** (pin 10) | | | | | |
| Supply voltage | $V_P = V_{10\text{-}16}$ | 9,6 | – | 13,2 | V |
| Supply current for playback and burst keying | | | | | |
| at $-I_{13, 18, 23, 26, 27} = 0$ | $I_P = I_{10}$ | – | 61 | – | mA |
| at $-I_{13, 18, 23, 26, 27} = 0$; $V_P = 12$ V | $I_P = I_{10}$ | – | 62 | – | mA |
| **A.G.C. preamplifier** (pins 1 and 2) | | | | | |
| Input voltage (f = 4,43 MHz) during record (peak-to-peak value) | $V_{2\text{-}16(p\text{-}p)}$ | 20 | – | 400 | mV |
| Input voltage (f = 6,25 kHz) during playback (peak-to-peak value) | $V_{1\text{-}16(p\text{-}p)}$ | 30 | – | 400 | mV |
| Input resistance | $R_{1,\ 2\text{-}16}$ | 6 | – | – | kΩ |
| Input capacitance | $C_{1,\ 2\text{-}16}$ | – | – | 5 | pF |
| **625 kHz chrominance signal** (pin 26)* **(transposed on to 625 kHz signal)** | | | | | |
| Output voltage (peak-to-peak value) | $V_{26\text{-}16(p\text{-}p)}$ | – | 2 | – | V |
| Burst pre-emphasis (gain) | $G_{26}$ | – | 6 | – | dB |
| Signal suppression at output for f = 1,25 MHz | $\alpha_{26}$ | – | 35 | – | dB |
| for f = 5,06 MHz (externally balanced via pins 3 and 4) | $\alpha_{26}$ | – | 40 | – | dB |
| during colour killing (pin 25) | $\alpha_{26}$ | 40 | – | – | dB |
| D.C. output voltage | $V_{26\text{-}16}$ | – | 6,7 | – | V |
| Colour killing voltage | $V_{25\text{-}16}$ | – | – | 2 | V |
| **4,43 MHz chrominance signal** (pin 27)* | | | | | |
| Output voltage during record (peak-to-peak value) | $V_{27\text{-}16(p\text{-}p)}$ | – | 1,15 | – | V |
| during playback after signal mixing subcarrier (peak-to-peak value) | $V_{27\text{-}16(p\text{-}p)}$ | – | – | 3,1 | V |
| Burst de-emphasis (gain) | $G_{27}$ | – | –5 | – | dB |
| Signal suppression at output for f = 5,06 MHz (externally balanced) | $\alpha_{27}$ | – | 40 | – | dB |
| for f = 8,86 MHz | $\alpha_{27}$ | – | 30 | – | dB |
| for f = 3,81 MHz | $\alpha_{27}$ | – | 38 | – | dB |
| for f = 3,18 MHz | $\alpha_{27}$ | – | 30 | – | dB |
| D.C. output voltage | $V_{27\text{-}16}$ | – | 7 | – | V |

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* The chrominance signal values hold for a 75% saturated colour bar signal.

DEVELOPMENT SAMPLE DATA

| parameter | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| **4,43 MHz chrominance signal amplifier*** | | | | | |
| Burst input signal | | | | | |
| at pin 21 (peak-to-peak value) | $V_{21\text{-}16(p\text{-}p)}$ | – | 190 | – | mV |
| at pin 22 (peak-to-peak value) | $V_{22\text{-}16(p\text{-}p)}$ | – | 190 | – | mV |
| Input resistance | | | | | |
| at pin 21 | $R_{21\text{-}16}$ | 3,3 | – | – | kΩ |
| at pin 22 | $R_{22\text{-}16}$ | 3,3 | – | – | kΩ |
| Output voltage of the chrominance signal | | | | | |
| at pin 23 (peak-to-peak value) | $V_{23\text{-}16(p\text{-}p)}$ | – | 470 | – | mV |
| at pin 24 (peak-to-peak value)** | $V_{24\text{-}16(p\text{-}p)}$ | – | – | 2 | V |
| Signal suppression at output (pin 23) | | | | | |
| during colour killing | $\alpha_{23}$ | 35 | – | – | dB |
| D.C. output voltage | | | | | |
| during colour-on | $V_{23\text{-}16}$ | – | 2,4 | – | V |
| during colour-off (killed) | $V_{23\text{-}16}$ | – | 0,7 | – | V |
| **Subcarrier-mixer** | | | | | |
| 625 kHz input voltage; sinewave | | | | | |
| (peak-to-peak value) | $V_{14\text{-}16(p\text{-}p)}$ | 220 | – | – | mV |
| Input resistance | $R_{14\text{-}16}$ | 1 | – | – | kΩ |
| D.C. output voltage | $V_{13\text{-}16}$ | – | 6,25 | – | V |
| 5,06 MHz output voltage▲ | | | | | |
| selective (peak-to-peak value) | $V_{13\text{-}16(p\text{-}p)}$ | – | 800 | – | V |
| Signal suppression at output▲ | | | | | |
| for f = 4,43 MHz | $\alpha_{13}$ | 20 | – | – | dB |
| for f = 5,68 MHz | $\alpha_{13}$ | 30 | – | – | dB |
| **Subcarrier amplifier and H/8 selector** | | | | | |
| 5,06 MHz input voltage (peak-to-peak value) | $V_{6\text{-}16(p\text{-}p)}$ | 250 | – | – | mV |
| Input resistance | $R_{6\text{-}16}$ | 1,9 | – | – | kΩ |
| Input capacitance | $C_{6\text{-}16}$ | – | – | 5 | pF |
| Input voltage (pin 5) | | | | | |
| for H/8 selector ON | $V_{5\text{-}16}$ | 1,6 | – | – | V |
| for H/8 selector OFF | $V_{5\text{-}16}$ | – | – | 0,8 | V |
| Input resistance with $V_{5\text{-}16} > 1,6$ V | $R_{5\text{-}16}$ | 3 | – | – | kΩ |

---

* Chrominance signal values hold for a 75% saturated colour bar signal.

** Output voltage externally adjusted.

▲ Measured with a 0,3 V (peak-to-peak), 625 kHz input signal on pin 14 ($-I_{13}$ = 1 mA).

CHARACTERISTICS (continued)

| parameter | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| **4,43 MHz voltage controlled oscillator** (VCO) | | | | | |
| Input resistance | $R_{11\text{-}16}$ | – | 430 | – | Ω |
| Input capacitance | $C_{11\text{-}16}$ | – | – | 10 | pF |
| Output resistance | $R_{12\text{-}16}$ | – | – | 220 | Ω |
| PLL-controlled oscillator catching range | $\Delta f$ | ± 500 | – | – | Hz |
| Phase difference between oscillator and burst signals for ± 400 Hz deviation of crystal frequency | $\varphi$ | ± 7 | – | – | deg |
| **4,43 MHz local oscillator** | | | | | |
| Oscillator temperature coefficient* | TC | – | – | 3 | Hz/K |
| **Record/playback selector** (pin 20) | | | | | |
| Input voltage for record** | $V_{20\text{-}16}$ | – | – | 4 | V |
| Input current with $V_{20\text{-}16}$ = 4 V | $I_{20}$ | – | – | 130 | μA |
| Input voltage for playback | $V_{20\text{-}16}$ | 8 | – | – | V |
| Input current with $V_{20\text{-}16}$ = 8 V | $I_{20}$ | – | – | 430 | μA |
| Input resistance | $R_{20\text{-}16}$ | 7 | – | – | kΩ |
| **Colour on/off and SECAM selector** | | | | | |
| Input voltage (pin 19) | | | | | |
| for forced colour ON | $V_{19\text{-}16}$ | – | $V_{9\text{-}16}$ | – | V |
| for forced colour OFF | $V_{19\text{-}16}$ | – | – | 0,5 | V |
| for SECAM operation | $V_{19\text{-}16}$ | 8,8 | – | – | V |
| for PAL operation (normal) | $V_{19\text{-}16}$ | | pin open | | |
| Output voltage (pin 18)▲ | | | | | |
| with colour ON | $V_{18\text{-}16}$ | 5,9 | – | – | V |
| with colour OFF | $V_{18\text{-}16}$ | – | – | 1 | V |

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* Not considering the effects of external components.

** Pin open: record.

▲ D.C. average heterodyned by 1,6 V (peak-to-peak) H/2 signal.

| parameter | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| **Voltage stabilizer** (pin 9) | | | | | |
| External reference voltage range | $V_{9\text{-}16}$ | 5,4 | – | 5,8 | V |
| Input current | $-I_9$ | – | – | 0,12 | mA |
| **Burst keying pulse** (pin 17) | | | | | |
| Threshold voltage for burst keying | $V_{17\text{-}16}$ | 7,5 | – | – | V |
| Input current | $I_{17}$ | – | – | 5 | μA |
| Delay time of BK2 | $t_d$ | – | 1,0 | – | μs |
| **SECAM operation** (with $V_{19\text{-}16} > 8{,}8$ V) | | | | | |
| 5,0 MHz subcarrier input signal (pin 6) with phase inversion internally switched OFF (peak-to-peak value) | $V_{6\text{-}16(p\text{-}p)}$ | 250 | – | – | mV |
| Chrominance signal output voltage* (peak-to-peak value) | $V_{23\text{-}1(p\text{-}p)}$ | – | 370 | – | mV |
| D.C. output voltage with subcarrier-mixer switched OFF | $V_{13\text{-}16}$ | – | 3,5 | – | V |

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* Chrominance signal values hold for a 75% saturated colour bar signal.

This information is derived from development samples made available for evaluation. It does not necessarily imply that the device will go into regular production.

# VIDEO PROCESSOR FOR VIDEO RECORDERS

## GENERAL DESCRIPTION

The TDA3771 is a monolithic integrated circuit for video signal processing in video recorders. It incorporates the following features:

### Features

- 3 channel input selector
- 4 dB preamplifier
- A.G.C. amplifier:
  during record: controlled to sync pulse level and peak white level
  during playback: controlled to sync pulse level
- Pulse triggered clamping control stage
- Regeneration of the sync pulse
- Adder stage for the luminance signal (with keyed-in burst pulse) and chrominance signal
- Emitter follower output stage for the luminance signal (composite video)
- Two emitter follower output stages for the composite colour video signal.

## QUICK REFERENCE DATA

| | | | |
|---|---|---|---|
| Supply voltage (pin 14) | $V_P = V_{14\text{-}11}$ | typ. | 12 V |
| Supply current (pin 14) | $I_P = I_{14}$ | typ. | 60 mA |
| **Preamplifier** | | | |
| Composite colour video input signals (peak-to-peak value) | $V_{2,3,4\text{-}11(p\text{-}p)}$ | typ. | 2 V |
| Gain | $G_{18\text{-}2,3,4}$ | typ. | 4 dB |
| **A.G.C. amplifier** | | | |
| Composite video signal (peak-to-peak value) | $V_{12\text{-}11(p\text{-}p)}$ | typ. | 0,4 ± 6 dB |
| **Sync level detector** | | | |
| Threshold voltage for active sync | $V_{9\text{-}11}$ | min. | 6 V |
| **Sync pulse regenerator** | | | |
| Composite video output signal (controlled) (peak-to-peak value) | $V_{6\text{-}11(p\text{-}p)}$ | typ. | 4 V |
| **Adder stage** | | | |
| Input voltage (peak-to-peak value) | $V_{16\text{-}11(p\text{-}p)}$ | typ. | 0,3 V |

## PACKAGE OUTLINE

18-lead DIL; plastic (SOT-102CS).

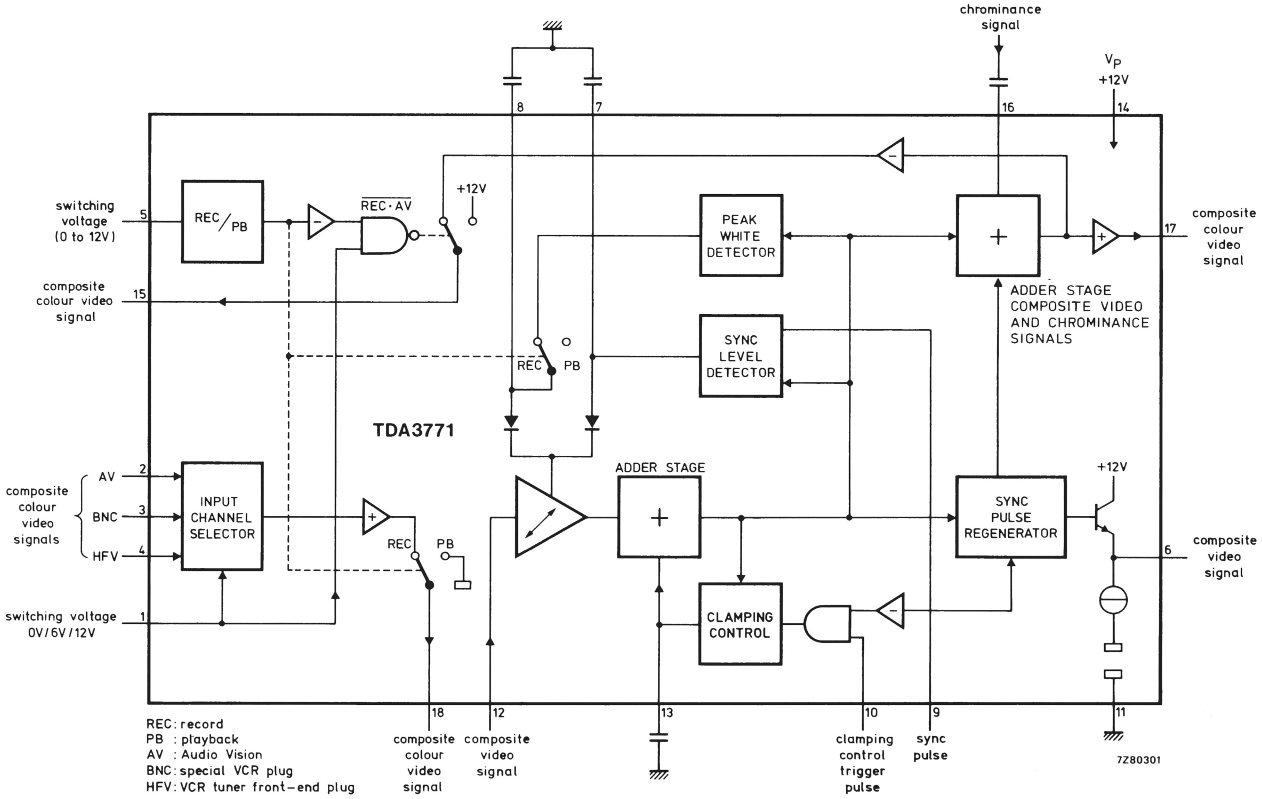

chrominance signal
VP +12V
composite colour video signal
composite video signal
switching voltage (0 to 12V)
composite colour video signal
composite colour video signals
AV
BNC
HFV
switching voltage 0V/6V/12V
REC/PB
REC·AV
+12V
PEAK WHITE DETECTOR
SYNC LEVEL DETECTOR
ADDER STAGE COMPOSITE VIDEO AND CHROMINANCE SIGNALS
INPUT CHANNEL SELECTOR
TDA3771
REC
PB
ADDER STAGE
SYNC PULSE REGENERATOR
CLAMPING CONTROL
+12V
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
composite colour video signal
composite video signal
clamping control trigger pulse
sync pulse
7Z80301
REC: record
PB : playback
AV : Audio Vision
BNC: special VCR plug
HFV: VCR tuner front-end plug

Fig. 1 Block diagram.

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | | |
|---|---|---|---|---|
| Supply voltage range (pin 14) | $V_P = V_{14\text{-}11}$ | | 0 to 13,2 | V |
| Voltage range at pins 1, 5, 9, 10, 12, 16 to pin 11 (ground) | $V_{n\text{-}11}$ | | 0 to $V_P$ | V |
| Voltage ranges | | | | |
| at pins 2, 3, 4 | $V_{2,3,4\text{-}11}$ | | 0 to $0{,}8V_P$ | V |
| at pins 7, 8 | $V_{7,8\text{-}11}$ | | $0{,}7V_P$ to $V_P$ | V |
| at pin 13 | $V_{13\text{-}11}$ | | $0{,}25V_P$ to $V_P$ | V |
| Currents | | | | |
| at pins 6, 15, 17 | $I_{6,15,17}$ | max. | 10 | mA |
| at pin 18 | $I_{18}$ | max. | 20 | mA |
| Total power dissipation | $P_{tot}$ | max. | 1 | W |
| Storage temperature range | $T_{stg}$ | | −25 to +150 | °C |
| Operating ambient temperature range | $T_{amb}$ | | −20 to +70 | °C |

## CHARACTERISTICS

$V_P = V_{14\text{-}11} = 12$ V; trigger pulse on pin 10 with a width of 4 $\mu$s; $T_{amb} = 25$ °C; measured in test circuit Fig. 2; unless otherwise specified

| parameter | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| **Supply** (pin 14) | | | | | |
| Supply voltage | $V_P = V_{14\text{-}11}$ | 9,6 | – | 13,2 | V |
| Supply current | $I_P = I_{14}$ | – | 60 | – | mA |
| **Input channel selector** | | | | | |
| Input resistance | $R_{1\text{-}11}$ | – | 7,5 | – | kΩ |
| Internal bias voltage | $V_{1\text{-}11}$ | – | 6 | – | V |
| Selector switching voltages on pin 1-11 | | | | | |
| to select input pin 4 | $V_{1\text{-}11}$ | – | – | 2 | V |
| to select input pin 3 | $V_{1\text{-}11}$ | 4 | – | 8 | V |
| to select input pin 2 | $V_{1\text{-}11}$ | 10 | – | – | V |
| **Preamplifier** | | | | | |
| Composite colour video input signals (peak-to-peak value) | $V_{2,3,4\text{-}11(p\text{-}p)}$ | – | 2 | – | V |
| Input resistance | $R_{2,3,4\text{-}11}$ | – | 10 | – | kΩ |
| Input capacitance | $C_{2,3,4\text{-}11}$ | – | 10 | – | pF |
| Gain | $G_{18\text{-}2,3,4}$ | – | 4 | – | dB |
| D.C. output voltage | | | | | |
| during record | $V_{18\text{-}11}$ | – | – | 5,8 | V |
| during playback | $V_{18\text{-}11}$ | – | 1 | – | V |
| Frequency response (0 to 3 MHz) | $\alpha_{18\text{-}2,3,4}$ | – | – | 1 | dB |
| Signal suppression at output (pin 18) | | | | | |
| with no input selected | $\alpha_{18}$ | 43 | – | – | dB |
| during playback | $\alpha_{18}$ | 50 | – | – | dB |
| **A.G.C. amplifier** | | | | | |
| Input voltage (composite video signal) (peak-to-peak value) | $V_{12\text{-}11(p\text{-}p)}$ | – | 0,4 ± 6 dB | – | V |
| Input resistance | $R_{12\text{-}11}$ | – | 10 | – | kΩ |
| Input capacitance | $C_{12\text{-}11}$ | – | 10 | – | pF |
| Frequency response (0 to 3 MHz) | $\alpha_{15,17\text{-}12}$ | – | 1 | – | dB |
| **Peak-white and sync-pulse level detectors** | | | | | |
| Capacitor currents | | | | | |
| charging current on pin 8 | $-I_8$ | – | 15 | – | mA |
| discharging current on pin 8 | $I_8$ | – | 0,8 | – | $\mu$A |
| charging current on pin 7 | $-I_7$ | – | 0,3 | – | mA |
| discharging current on pin 7 | $I_7$ | – | 0,3 | – | mA |

| parameter | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| **Clamping control triggering and sync pulse regeneration** | | | | | |
| Threshold voltage for clamping control ON $V_{9\text{-}11} = 0$ V | $V_{10\text{-}11}$ | 7 | – | – | V |
| Input current | $-I_{10}$ | – | – | 50 | μA |
| Threshold voltage for active sync pulse generation and clamping control OFF | $V_{9\text{-}11}$ | 6 | – | – | V |
| Input current | $-I_9$ | – | – | 50 | μA |
| Charging current | $-I_{13}$ | – | 0,3 | – | mA |
| Discharging current | $I_{13}$ | – | 0,3 | – | mA |
| Black level voltage | $V_{6\text{-}11}$ | – | 5,5 | – | V |
| Sync pulse slicing level | $V_{6\text{-}11}$ | – | 5,2 | – | V |
| Controlled output signal (peak-to-peak value) | $V_{6\text{-}11(p\text{-}p)}$ | – | 4,0 | – | V |
| **Record/playback selector** | | | | | |
| Input voltage | | | | | |
| for playback | $V_{5\text{-}11}$ | 7 | – | – | V |
| for record | $V_{5\text{-}11}$ | – | – | 5 | V |
| Input current | $-I_5$ | – | – | 50 | μA |
| **Chrominance signal adder and output stage** | | | | | |
| Input voltage (peak-to-peak value) | $V_{16\text{-}11(p\text{-}p)}$ | – | 0,3 | – | V |
| Gain | $G_{15,17\text{-}16}$ | – | 12 | – | dB |
| Input resistance | $R_{16\text{-}11}$ | – | 10 | – | kΩ |
| Input capacitance | $C_{16\text{-}11}$ | – | 10 | – | pF |
| Output signal (peak-to-peak values) | | | | | |
| composite colour video signal: negative | $V_{15\text{-}11(p\text{-}p)}$ | – | 2 | – | V |
| composite colour video signal: positive | $V_{17\text{-}11(p\text{-}p)}$ | – | 2 | – | V |
| 2nd harmonic suppression | $\alpha_{17}$ | 40 | – | – | dB |
| Black level | | | | | |
| composite colour video signal: negative | $V_{15\text{-}11}$ | – | 9,3 | – | V |
| composite colour video signal: positive | $V_{17\text{-}11}$ | – | 3,7 | – | V |
| Signal suppression during record and with input pin 2 selected | $\alpha_{15}$ | 40 | – | – | dB |
| D.C. voltage during record and with input pin 2 selected | $V_{15\text{-}11}$ | – | 12 | – | V |
| Output resistance during record and with input pin 2 selected | $R_{15\text{-}11}$ | – | 30 | – | kΩ |

DEVELOPMENT SAMPLE DATA

## APPLICATION INFORMATION

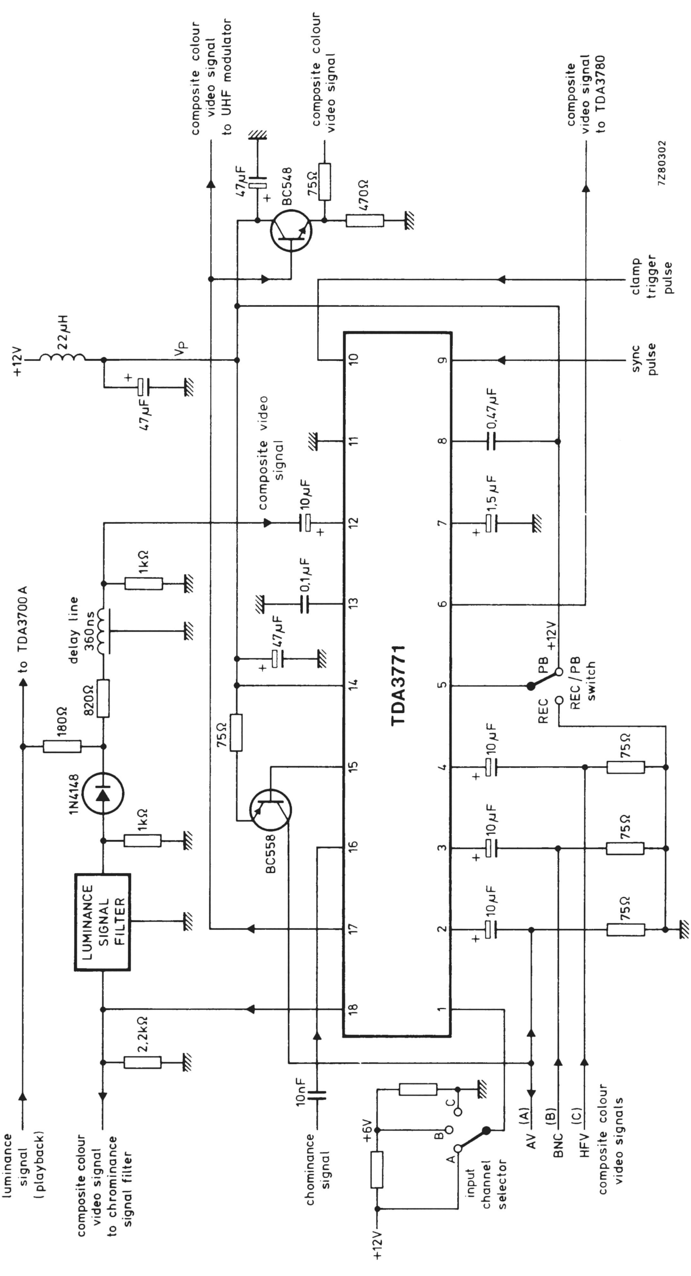

TDA3771
composite colour video signal to UHF modulator
composite colour video signal
composite video signal to TDA3780
7Z80302
BC548
47µF
75Ω
470Ω
clamp trigger pulse
sync pulse
+12V
22µH
VP
47µF
composite video signal
10µF
0,47µF
1,5µF
0,1µF
47µF
to TDA3700 A
delay line 360ns
1kΩ
180Ω
820Ω
PB
+12V
REC
REC / PB switch
75Ω
1N4148
BC558
10µF
LUMINANCE SIGNAL FILTER
2,2kΩ
10nF
luminance signal (playback)
composite colour video signal to chrominance signal filter
chominance signal
+6V
+12V
A
B
C
input channel selector
AV (A)
BNC (B)
HFV (C)
composite colour video signals
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18

Fig. 2 Application diagram; also used as test circuit.

DEVELOPMENT SAMPLE DATA
This information is derived from development samples made available for evaluation. It does not necessarily imply that the device will go into regular production.

# FREQUENCY MODULATOR FOR VIDEO RECORDERS

## GENERAL DESCRIPTION

The TDA3780 is a monolithic integrated circuit for frequency modulation in video recorders.

### Features

- Voltage clamping control stage
- Two-stage amplification for the luminance signal with linear and dynamic pre-emphasis (adjustable)
- Adjustable white limiter
- 3 MHz voltage controlled oscillator (VCO), with facility for switch-off
- Limiting stage with facility to disconnect from output stage
- Switch-off pulse for VCO and output stage

## QUICK REFERENCE DATA

| | | | |
|---|---|---|---|
| Supply voltage (pin 1) | $V_P = V_{1\text{-}18}$ | typ. | 12 V |
| Supply current (pin 1) | $I_P = I_1$ | typ. | 52 mA |
| **Pre-emphasis amplifier and clamping stage** (dynamic) | | | |
| Luminance input signal (pin 2)<br>(peak-to-peak value) | $V_{2\text{-}18(p\text{-}p)}$ | typ. | 2,0 V |
| Output voltage (pin 4) | $V_{4\text{-}18}$ | | 2,5 to 8,0 V |
| **Pre-emphasis amplifier stage** (linear) | | | |
| Output voltage (pin 7) | $V_{7\text{-}18}$ | | 2,5 to 8,0 V |
| **Output stage** | | | |
| D.C. output voltage | $V_{17\text{-}18}$ | typ. | 6,0 V |
| FM signal output voltage<br>(peak-to-peak value) | $V_{17\text{-}18(p\text{-}p)}$ | typ. | 4,2 V |

## PACKAGE OUTLINE

18-lead DIL; plastic (SOT-102CS).

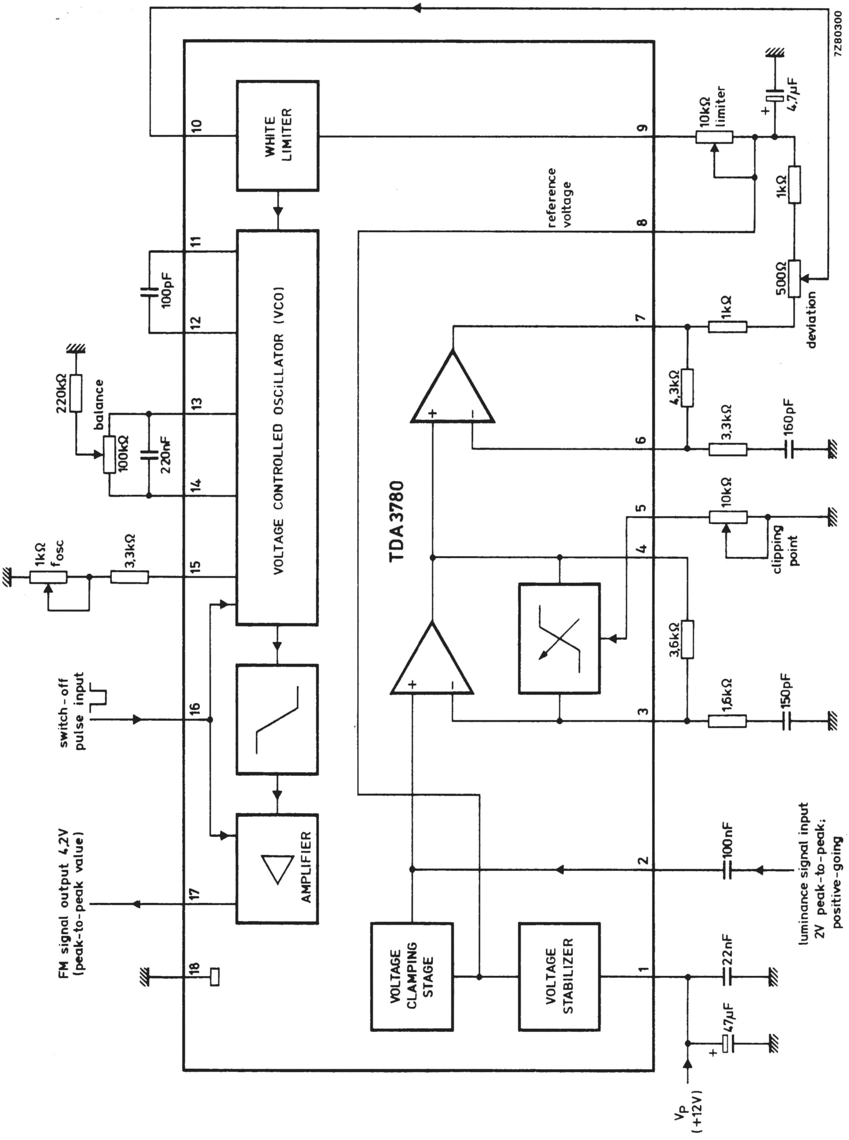

WHITE LIMITER
VOLTAGE CONTROLLED OSCILLATOR (VCO)
AMPLIFIER
VOLTAGE CLAMPING STAGE
VOLTAGE STABILIZER
TDA 3780
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
100pF
220kΩ
balance
100kΩ
220nF
1kΩ
f_osc
3,3kΩ
switch-off pulse input
FM signal output 4,2V (peak-to-peak value)
reference voltage
10kΩ
limiter
4,7μF
1kΩ
500Ω
deviation
1kΩ
4,3kΩ
3,3kΩ
160pF
10kΩ
clipping point
3,6kΩ
1,6kΩ
150pF
100nF
luminance signal input 2V peak-to-peak; positive-going
22nF
47μF
V_P (+12V)
7Z80300

Fig. 1 Block diagram.

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | |
|---|---|---|---|
| Supply voltage (pin 1) | $V_P = V_{1\text{-}18}$ | max. | 13,2 V |
| Voltage range at pins 2, 3, 4, 5, 6, 7, 9, 10, 13, 14, 15, 16, 17 to pin 18 (ground) | $V_{n\text{-}18}$ | | 0 to $V_P$ V |
| Voltage at pin 8 | $V_{8\text{-}18}$ | max. | 10 V |
| Currents at pins 11 and 12 | $\pm I_{11,\,12}$ | max. | 5 mA |
| Total power dissipation | $P_{tot}$ | max. | 920 mW |
| Storage temperature range | $T_{stg}$ | | −25 to + 125 °C |
| Operating ambient temperature range | $T_{amb}$ | | 0 to + 70 °C |

## CHARACTERISTICS

$V_P = V_{1\text{-}18} = 12$ V; balancing the 2nd harmonic to the minimum level; $T_{amb} = 25$ °C; measured in test circuit Fig. 1; unless otherwise specified

| parameter | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| **Supply** (pin 1) | | | | | |
| Supply voltage | $V_P = V_{1\text{-}18}$ | 9,6 | 12 | 13,2 | V |
| Supply current | $I_P = I_1$ | – | 52 | – | mA |
| Reference voltage | $V_{8\text{-}18}$ | – | 4 | – | V |
| **Pre-emphasis amplifier and clamping stage** (dynamic) | | | | | |
| Luminance input signal (pin 2) (peak-to-peak value) | $V_{2\text{-}18(p\text{-}p)}$ | – | 2 | – | V |
| Input impedance at $V_{2\text{-}18} < V_{8\text{-}18}$; $-I_2 = 1$ mA | $\lvert Z_{2\text{-}18}\rvert$ | – | 25 | – | Ω |
| Input current at $V_{2\text{-}18} > V_{8\text{-}18}$ | $I_2$ | – | 2 | – | µA |
| Input bias current | $I_3$ | – | 1 | – | µA |
| Clamping voltage for the input signal clamped at top sync | $V_{2\text{-}18}$ | – | 4 | – | V |
| Gain-bandwidth product | | 30 | – | – | MHz |
| Output voltage (pin 4) | $V_{4\text{-}18}$ | 2,5 | – | 8 | V |
| Start of gain reduction (adjustable at pin 5) | $V_{4\text{-}3}$ | 100 | – | – | mV |

DEVELOPMENT SAMPLE DATA

**CHARACTERISTICS** (continued)

| parameter | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| **Pre-emphasis amplifier stage** (linear) | | | | | |
| Input bias current | $I_6$ | – | – | 1 | μA |
| Gain-bandwidth product | | 30 | – | – | MHz |
| Output voltage (pin 7) | $V_{7-18}$ | 2,5 | – | 8 | V |
| **White limiter** (pin 10) | | | | | |
| Limiting | | | | | |
| at $I_9 = 0$ | $V_{10-18}$ | 7,5 | – | – | V |
| at $I_9 = 0,5$ mA | $V_{10-18}$ | – | 4 | – | V |
| **Voltage controlled oscillator** (VCO) | | | | | |
| Output frequency with $C_{osc} = 100$ pF (pin 11-12); $R_{osc} = 3,8$ kΩ (pin 15) | $f_{osc}$ | 3,04 | 3,30 | 3,56 | MHz |
| Oscillator steepness | $f_{osc}/\Delta V_{10-18}$ | – | 1,5 | – | MHz/V |
| **FM output signal switching stage** | | | | | |
| Input voltage to switch FM off | $V_{16-18}$ | – | – | 4 | V |
| Input voltage to switch FM on | $V_{16-18}$ | 6 | – | – | V |
| Output voltage suppression with FM switched off | $\alpha_o$ | 50 | – | – | dB |
| **Output stage** (pin 17) | | | | | |
| D.C. output voltage | $V_{17-18}$ | – | 6 | – | V |
| FM signal output voltage (peak-to-peak value) | $V_{17-18(p-p)}$ | – | 4,2 | – | V |
| Suppression of the 2nd harmonic $\frac{\text{V (1st harmonic)}}{\text{V (2nd harmonic)}}$ | $\alpha_{harm}$ | 40 | – | – | dB |
| AM suppression | $\alpha_{AM}$ | 40 | – | – | dB |
| Crosstalk between output and input | $\frac{V_{17-18}}{V_{2-18}}$ | 40 | – | – | dB |

# STEREO/DUAL TV SOUND PROCESSING CIRCUIT

The TDA3800 is a stereo/dual TV sound decoder circuit, including the second i.f. amplifier and f.m. demodulator.

The circuit includes the following functions:

- 2nd i.f. limiter/amplifier and demodulator (5,742 MHz) for second sound channel
- Level adjustment for the demodulated a.f. signal for channel matching
- Pilot carrier processing with digital identification, hysteresis and short switching times
- De-matrixing of the signals for the two audio channels
- De-emphasis
- Mode selection of stereo/mono or sound 1/sound 2 with storage of selected mode
- Two dual channel, independently controllable a.f. outputs
- Low-resistance a.f. outputs (short-circuit protected); can be used for headphone
- Switched output for controlling external audio/video equipment
- Signal path control by an identification bit (also in audio/video mode)
- LED indication of selected mode (also in audio/video mode)
- Possibility to apply a.f. signals from external equipment via the de-emphasis inputs (audio/video mode)

## QUICK REFERENCE DATA

| | | | | |
|---|---|---|---|---|
| Supply voltage (pin 20) | $V_P$ | typ. | 12 | V |
| 2nd sound i.f. input voltage for start of limiting (r.m.s. value) | $V_{i(rms)}$ | typ. | 50 | µV |
| Pilot carrier amplifier control range | $\Delta G_v$ | > | 20 | dB |
| A.F. input voltage (r.m.s. value) | $V_{i(rms)}$ | typ. | 1 | V |
| A.F. demodulator output voltage (r.m.s. value) | $V_{o(rms)}$ | typ. | 0,6 | V |
| LED output current | $I_{LED}$ | typ. | 15 | mA |
| Signal-to-noise ratio of the a.f. signal switches | S/N | typ. | 80 | dB |
| Crosstalk in stereo mode | $\alpha_S$ | > | 40 | dB |
| Crosstalk in dual sound mode | $\alpha_{DS}$ | > | 60 | dB |

## PACKAGE OUTLINES

28-lead DIL; plastic (SOT-117).

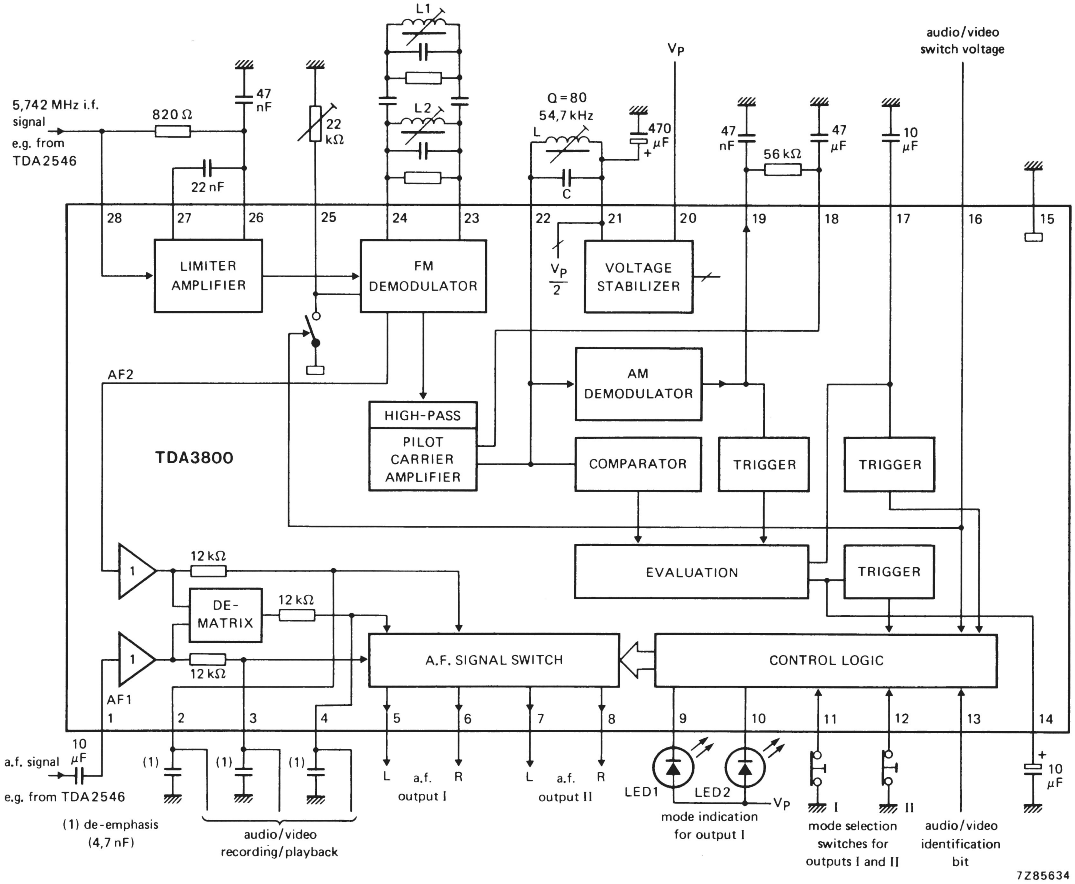

5,742 MHz i.f.
signal
e.g. from
TDA2546
820 Ω
47
nF
22 nF
22
kΩ
L1
L2
Q = 80
54,7 kHz
L
C
470
μF
+
V<sub>P</sub>
47
nF
56 kΩ
47
μF
10
μF
audio/video
switch voltage
28
27
26
25
24
23
22
21
20
19
18
17
16
15
LIMITER
AMPLIFIER
FM
DEMODULATOR
VP/2
VOLTAGE
STABILIZER
AM
DEMODULATOR
HIGH-PASS
PILOT
CARRIER
AMPLIFIER
COMPARATOR
TRIGGER
TRIGGER
EVALUATION
TRIGGER
TDA3800
AF2
AF1
1
1
12 kΩ
DE-
MATRIX
12 kΩ
12 kΩ
A.F. SIGNAL SWITCH
CONTROL LOGIC
1
2
3
4
5
6
7
8
9
10
11
12
13
14
10
μF
a.f. signal
e.g. from TDA2546
(1)
(1)
(1)
(1) de-emphasis
(4,7 nF)
audio/video
recording/playback
L
a.f.
R
output I
L
a.f.
R
output II
LED1
LED2
VP
mode indication
for output I
I
II
mode selection
switches for
outputs I and II
audio/video
identification
bit
+
10
μF
7Z85634

Fig. 1 Block diagram and test circuit.

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | | |
|---|---|---|---|---|
| Supply voltage (pin 20) | $V_P = V_{20\text{-}15}$ | max. | 14 | V |
| Voltage | | | | |
| at pin 1 | $V_{1\text{-}15}$ | max. | $V_P$ | |
| at pins 9 and 10 | $V_{9;\ 10\text{-}15}$ | max. | $V_P$ | |
| at pin 16 | $V_{16\text{-}15}$ | max. | $V_P$ | |
| Current | | | | |
| at pins 11 and 12 | $I_{11;\ 12}$ | max. | 1 | mA |
| at pin 13 | $I_{13}$ | max. | 1 | mA |
| at pin 21 | short-circuit protected | | | |
| Total power dissipation | $P_{tot}$ | max. | 1,5 | W |
| Storage temperature range | $T_{stg}$ | | −25 to + 125 | °C |
| Operating ambient temperature range | $T_{amb}$ | | −20 to + 70 | °C |

## CHARACTERISTICS

$V_P = 12$ V; $T_{amb} = 25$ °C; measured in Fig. 1 with a 1 kHz signal. $V_{1\text{-}15(rms)} = 0{,}5$ V, an i.f. signal $V_{28\text{-}15(rms)} = 5$ mV (VC/2SC = 20 dB, $\Delta f = \pm 50$ kHz, $f_m = 400$ Hz) and with adjusted de-matrix circuit; i.f. filter selection at input pin 28 as in Fig. 2.

| | | | | |
|---|---|---|---|---|
| Supply voltage range | $V_P = V_{20\text{-}15}$ | | 10,8 to 13,2 | V |
| Supply current | $I_P = I_{20}$ | typ. | 53 | mA |

**FM limiter/amplifier and demodulator**

| | | | | |
|---|---|---|---|---|
| Start of limiting at: | $V_{28\text{-}15(rms)}$ | typ. | 50 | μV |
| Input resistance | $R_{28\text{-}15}$ | typ. | 40 | kΩ |
| Input capacitance | $C_{28\text{-}15}$ | typ. | 4,5 | pF |
| AM suppression | $\alpha_{AM}$ | typ. | 60 | dB |

**Pilot carrier processing**

| | | | | |
|---|---|---|---|---|
| Input voltage | $V_{18\text{-}15}$ | typ. | 6,9 | V |
| AM demodulator output voltage | $V_{19\text{-}15}$ | typ. | 7,0 | V |
| AM demodulator output voltage for m = 50% (peak-to-peak value) | $V_{19\text{-}15(p\text{-}p)}$ | typ. | 2,0 | V |
| Controlled pilot carrier output voltage (peak-to-peak value) | $V_{22\text{-}21(p\text{-}p)}$ | typ. | 200 | mV |
| Output resistance | $R_{22\text{-}15}$ | > | 50 | kΩ |

**Identification frequency evaluation**

| | | | | |
|---|---|---|---|---|
| No identification signal (mono) | $V_{14\text{-}15}$ | < | 2 | V |
| Identification signal available (dual sound/stereo) | $V_{14\text{-}15}$ | typ. | 6 | V |
| Stereo transmission | $V_{17\text{-}15}$ | < | 2 | V |
| Dual sound transmission | $V_{17\text{-}15}$ | > | 7 | V |

## CHARACTERISTICS (continued)

### De-matrixing

| | | | | |
|---|---|---|---|---|
| Output voltages | $V_{2;\,3;\,4\text{-}15}$ | typ. | 5,3 | V |
| De-emphasis output resistances | $R_{2;\,3;\,4\text{-}15}$ | typ. | 12 | kΩ |
| A.F. output signal of 2nd i.f. (r.m.s. value; see Fig. 3) | $V_{2\text{-}15(rms)}$ | typ. | 0,6 | V |
| Attenuation of the demodulator output signal AF2 at audio/video mode | $\alpha_{AF2}$ | > | 75 | dB |

### AF1 input

| | | | | |
|---|---|---|---|---|
| Input voltage | $V_{1\text{-}15}$ | typ. | 6 | V |
| Input resistance | $R_{1\text{-}15}$ | typ. | 14 | kΩ |
| Maximum input signal (r.m.s. value) | $V_{1\text{-}15(rms)}$ | typ. | 2 | V |

### A.F. signal switches

| | | | | |
|---|---|---|---|---|
| Output voltages | $V_{5;\,6;\,7;\,8\text{-}15}$ | typ. | 5,3 | V |
| Output resistances | $R_{5;\,6;\,7;\,8\text{-}15}$ | typ. | 200 | Ω* |
| Maximum a.f. output signals (r.m.s. value) | | | | |
| for $V_{AF\ I(rms)}$ | $V_{5;\,6\text{-}15(rms)}$ | typ. | 2 | V |
| for $V_{AF\ II(rms)}$ | $V_{7;\,8\text{-}15(rms)}$ | typ. | 2 | V |
| Total distortion during applying a signal: $V_{2;\,3;\,4\text{-}15(rms)} = 0{,}5$ V | $d_{tot}$ | typ. | 0,1 | % |
| Signal plus noise-to-noise ratio | S + N/N | typ. | 80 | dB |
| Crosstalk attenuation | | | | |
| in stereo mode | $\alpha_S$ | > | 40 | dB |
| in dual sound mode (f = 20 Hz to 20 kHz) | $\alpha_{DS}$ | > | 60 | dB |

### Audio/video switch

| | | | | |
|---|---|---|---|---|
| Audio/video switch voltage | | | | |
| for playback (HIGH) | $V_{16\text{-}15}$ | | 7 to $V_P$ | V |
| for recording (LOW) | $V_{16\text{-}15}$ | | 0 to 2,5 | V |
| Audio/video identification bit | | | | |
| for stereo mode (LOW) | $V_{13\text{-}15}$ | | 0 to 0,2 | V |
| for dual sound mode (HIGH $V_{13\text{-}15} = 0{,}7$ V | $I_{13}$ | typ. | 0 | mA |

---

* Connection of high-impedance headphones is possible.

**Mode selection switches for output I and II** (see Fig. 1)

The pushbuttons at pins 11 and 12 are assigned to the a.f. outputs I and II respectively.

Serial commands can be applied to the mode selection switch inputs (pins 11 and 12) for choice of stereo/mono or AF1/AF2. The choice for stereo and dual sound transmission is stored internally.

When a television transmitter changes its identification from dual sound to stereo and then back to dual sound again, the last selected dual sound signal is available automatically because of the internal storage of the choice. This holds for mono/stereo selection too.

Power-on reset: when applying the supply voltage, the stereo or the AF1 signal appears at both the outputs I and II or depending on the type of transmission.

| | | | |
|---|---|---|---|
| Switching at LOW level (see Fig. 4) | $V_{11;\,12\text{-}15}$ | | 0 to 0,2 V |
| Situation at HIGH level (see Fig. 4)<br>$V_{11;\,12\text{-}15} = 0{,}7$ V | $I_{11;\,12}$ | typ. | 0 mA |
| Pulse duration | $t_p$ | $>$ | 1 μs |

**Mode indication** (pins 9 and 10)

Only the mode for output I is indicated.

| | | | |
|---|---|---|---|
| Maximum output current | $I_{9;\,10}$ | typ. | 15 mA |

**Indication possibilities**

| LED 1 | LED 2 | selected reception mode |
|---|---|---|
| OFF | OFF | mono at mono or stereo transmission |
| ON | ON | stereo at stereo transmission |
| ON | OFF | AF1 signal at dual sound transmission |
| OFF | ON | AF2 signal at dual sound transmission |

**Voltage stabilizer** (pin 21)

| | | | |
|---|---|---|---|
| Output voltage | $V_{21\text{-}15}$ | typ. | 6 V |
| Maximum d.c. output current short-circuit protected | $\pm I_{21}$ | typ. | 0,5 mA |

DEVELOPMENT SAMPLE DATA

CHARACTERISTICS (continued)

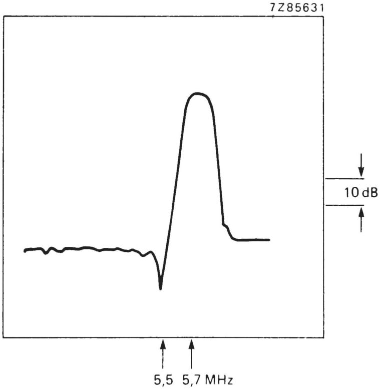


Fig. 2 IF2 filter selection.

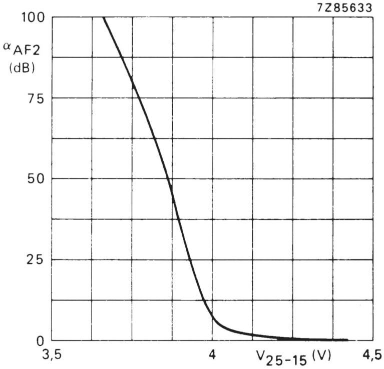


Fig. 3 Level adjustment in the demodulator part for matching of the AF2 signal to the AF1 signal; attenuation $\alpha_{AF2}$ as a function of $V_{25-15}$.

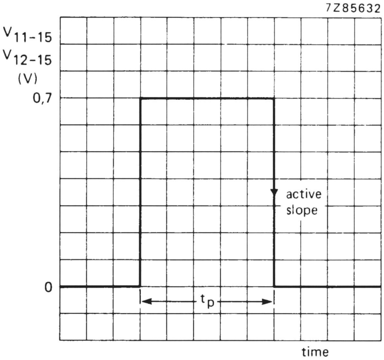


Fig. 4 Mode selection switching levels.

# SMALL SIGNAL COMBINATION IC FOR MONOCHROME TV

## GENERAL DESCRIPTION

The TDA4500 combines all small signal functions (except the tuner) which are required for a monochrome television receiver.

For a complete monochrome television receiver only output stages are required to be added for horizontal and vertical deflection, video and sound. The TDA4500 can also be used in simple colour television receivers. In this application an external sandcastle pulse generator is required.

It incorporates the following functions:

- vertical sync separator/oscillator
- vertical output
- coincidence detector (sound mute)
- phase detector/frequency control
- a.g.c. detector
- sync separator
- horizontal oscillator
- synchronous demodulator
- vision i.f. amplifier
- tuner a.g.c.
- d.c. volume control
- a.f.c. detector
- video output
- sound demodulator
- audio output
- gate pulse generator
- sound limiter/feedback
- 90° phase shift
- overload detector
- horizontal output

## QUICK REFERENCE DATA

| | | | | |
|---|---|---|---|---|
| Supply voltage | $V_{7-10}$, $V_{22-10}$ | typ. | 10,5 | V |
| Supply current | $I_7$ | typ. | 75 | mA |
| Supply current | $I_{22}$ | typ. | 4,5 | mA |
| Operating ambient temperature range | $T_{amb}$ | | −25 to +65 | °C |
| Storage temperature range | $T_{stg}$ | | −25 to +150 | °C |
| Power dissipation | $P_{tot}$ | max. | 1,7 | W |

## PACKAGE OUTLINE

28-lead DIL; plastic, with internal heat spreader (SOT-117).

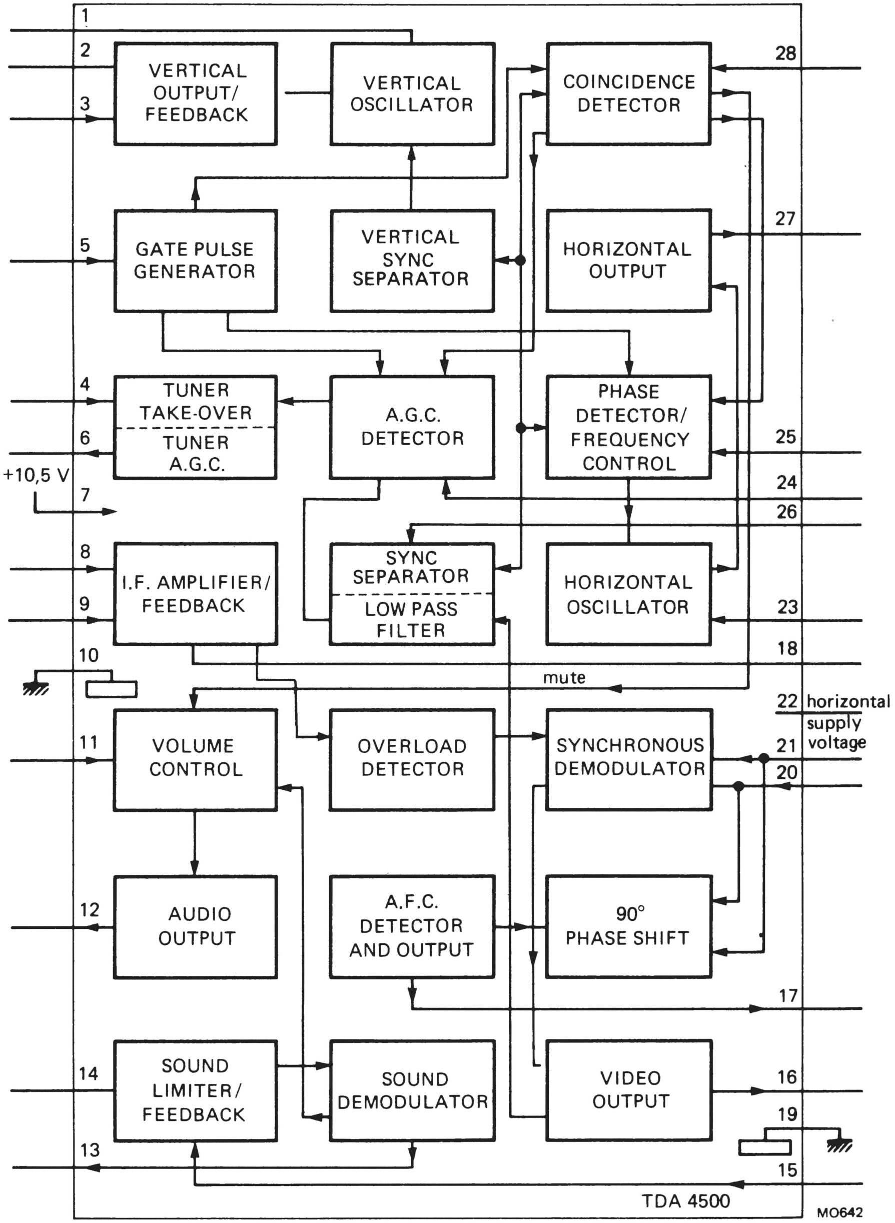

1
2
3
VERTICAL OUTPUT/ FEEDBACK
VERTICAL OSCILLATOR
COINCIDENCE DETECTOR
28
5
GATE PULSE GENERATOR
VERTICAL SYNC SEPARATOR
HORIZONTAL OUTPUT
27
4
TUNER TAKE-OVER
TUNER A.G.C.
6
A.G.C. DETECTOR
PHASE DETECTOR/ FREQUENCY CONTROL
25
+10,5 V
7
24
26
8
I.F. AMPLIFIER/ FEEDBACK
9
SYNC SEPARATOR
LOW PASS FILTER
HORIZONTAL OSCILLATOR
23
10
18
mute
22 horizontal supply voltage
VOLUME CONTROL
11
OVERLOAD DETECTOR
SYNCHRONOUS DEMODULATOR
21
20
12
AUDIO OUTPUT
A.F.C. DETECTOR AND OUTPUT
90° PHASE SHIFT
17
14
SOUND LIMITER/ FEEDBACK
SOUND DEMODULATOR
VIDEO OUTPUT
16
19
13
15
TDA 4500
MO642

Fig. 1 Block diagram.

## PINNING

| Pin number | function | Pin number | function |
|---|---|---|---|
| 1. | vertical oscillator | 15. | sound i.f. |
| 2. | vertical output | 16. | video output |
| 3. | vertical feedback | 17. | a.f.c. output |
| 4. | top linearity | 18. | decoupling capacitor |
| 5. | flyback pulse | 19. | ground |
| 6. | tuner a.g.c. | 20. | 38,5 MHz reference |
| 7. | +10,5 V supply | 21. | (38,9 MHz reference) |
| 8. | i.f. input | 22. | horizontal supply voltage |
| 9. | | 23. | horizontal oscillator |
| 10. | ground | 24. | top sync detector |
| 11. | volume control | 25. | phase detector |
| 12. | sound output | 26. | sync separator |
| 13. | 6 MHz tuning<br>(5,5 MHz tuning) | 27. | horizontal output |
| 14. | decoupling | 28. | mute/coincidence detector |

DEVELOPMENT SAMPLE DATA

## FUNCTIONAL DESCRIPTION (Fig. 1)

A complete black-and-white receiver can be built around this circuit by adding only the output stages for horizontal and vertical deflection with the video and sound output stages. The TDA4500 can also be used in simple colour television receivers using an external circuit to generate the sandcastle.

The block diagram (Fig. 1) depicts the various functions which are described briefly below.

The sensitivity of the i.f. amplifier is 70 $\mu$V for a peak-to-peak output voltage of 3 V (compare the TDA3541). This amplifier has a symmetrical input (pins 8 and 9) and is followed by a synchronous demodulator. The external tuned circuit is connected to pins 20 and 21. This circuit provides the information for the a.f.c. circuit, the 90° phase shift being supplied by internal RC-networks. An a.f.c. output with a voltage swing of about 9 V is obtained from pin 17 ($V_{7-10}$ = 10,5 V).

The a.g.c. detector is gated to reduce sensitivity to external electrical noise and the a.g.c. time constant network is connected to pin 24. Gain control range of the i.f. amplifier is greater than 60 dB. Adjustments of the tuner take-over point is made at pin 4. When the voltage at pin 4 is approximately 3,5 V the direction of the tuner control voltage is positive-going. When the voltage at pin 4 is approximately 8 V the direction of the tuner control voltage is negative-going.

An output signal of 3 V (p-p) is obtained from the video amplifier (top sync level 1,5 V) with negative-going sync. Since the sound signal is derived from pin 16 (see Fig. 4) the video output is not blanked during the flyback period. As shown in the application circuit (Fig. 4) the band-pass filter for the sound must be connected between video output (pin 16) and sound i.f. input (pin 15). Sound information passes through a sound limiter network and a sound demodulator circuit with an external tuned circuit for this stage connected to pin 13. The demodulator is followed by a volume control stage with a control range of 80 dB and an output amplifier with an audio output signal of 170 mV (r.m.s.) for a $\Delta$f of 7,5 kHz and at maximum volume setting.

The slicing level of the sync separator is referred to the top sync and is determined by the values of external resistors, the recommended slicing level being 30%. Noise protection is provided for the sync separator stage. Separated sync pulses are supplied to the gated phase detector which compare the sync pulses with the sawtooth voltage obtained from the horizontal flyback pulse (pin 5). During catching the gating of the phase detector is switched off and the phase detector output current is increased.

The in-sync or out-of-sync condition is detected with the coincidence detector which is also used for transmitter identification. Sound output is suppressed when no input signal is available. Clamping the voltage on pin 28 to a level of 3,5 V sets the phase detector to a high output current, short time constant mode. This is appropriate for the reception of VCR signals.

Phase detector output voltage levels maintain the horizontal oscillator at its correct operating frequency. The push-pull output (pin 27) has a typical duty cycle of 40%.

Vertical sync pulses are obtained from an internal integrating network with the vertical sawtooth being generated in the vertical oscillator. This sawtooth voltage is compared with the feedback voltage from the deflection coil via pin 3. The comparator generates the drive voltage for the vertical deflection output stage.

The TDA4500 has four supply pins. Pin 7 and pin 10 are for the main positive supply and circuit ground respectively.

Critical circuits are grounded by pin 19. Pin 22 is the supply for the horizontal oscillator. A low current supply (5 mA minimum) can be used to start the oscillator from an external high voltage supply rail.

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC134)

| | | | | |
|---|---|---|---|---|
| Supply voltage | $V_{7-10}$, $V_{22-10}$ | max. | 13,2 | V |
| Total power dissipation | $P_{tot}$ | max. | 1,7 | W |
| Storage temperature range | $T_{stg}$ | | −25 to +150 | °C |
| Operating ambient temperature range | $T_{amb}$ | | −25 to +65 | °C |

## CHARACTERISTICS

$V_{7-10}$ = 10,5 V, $V_{22-10}$ = 10,5 V and $T_{amb}$ = 25 °C unless otherwise specified

| parameter | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| Supply voltage | $V_{7-10}$ | 9,5 | 10,5 | 13,2 | V |
| Supply current | $I_7$ | – | 75 | – | mA |
| Supply voltage (horizontal oscillator) | $V_{22-10}$ | 9,5 | 10,5 | 13,2 | V |
| Supply current (horizontal oscillator, note 1) | $I_{22}$ | – | 4,5 | – | mA |
| Power dissipation | $P_{tot}$ | – | 850 | – | mW |
| **Vision i.f. amplifier** (pin 8) | | | | | |
| Input sensitivity (onset of a.g.c.) at 39,5 MHz (note 2) | $V_{i(rms)}$ | – | 70 | – | μV |
| Differential input resistance (note 3) | $R_i$ | – | 800 | – | Ω |
| Differential input capacitance (note 3) | $C_i$ | – | 6 | – | pF |
| Gain control range | ΔG | – | 56 | – | dB |
| Output signal expansion for 50 dB input signal variation (note 4) | $\Delta V_o$ | – | 1 | – | dB |
| Maximum input signal | $V_{i\,max}$ | – | 50 | – | mV |
| **Video amplifier (note 5)** | | | | | |
| Zero signal output level (note 6) | $V_{16-10}$ | – | 5 | – | V |
| Top sync output level (note 7) | $V_{16-10}$ | 1,2 | 1,4 | 1,6 | V |
| Video output signal amplitude (peak-to-peak value) | $V_{16-10(p-p)}$ | 2,75 | 3,0 | 3,25 | V |
| Internal bias current of n-p-n emitter follower output transistor | $I_B$ | 1,4 | 2,0 | – | mA |
| Bandwidth of demodulated output signal | B | 5 | 6 | – | MHz |
| Video non-linearity (note 8) | | – | – | 10 | % |

**CHARACTERISTICS** (continued)

| parameter | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| **Tuner a.g.c.** | | | | | |
| Take-over voltage (pin 4) for positive-going tuner a.g.c. (n-p-n tuner) | $V_{4-10}$ | – | 3,5 | – | V |
| Take-over voltage (pin 4) for negative-going tuner a.g.c. (p-n-p tuner) | $V_{4-10}$ | – | 8 | – | V |
| Maximum tuner a.g.c. output swing | $I_{6\,max}$ | 2 | 3 | – | mA |
| Output saturation voltage at $I_6$ = 2 mA | $V_{6-10(sat)}$ | – | – | 300 | mV |
| Leakage current | $I_6$ | – | – | 1 | μA |
| **A.F.C. circuit (note 9)** | | | | | |
| A.F.C. output voltage swing | $V_{17-19}$ | 9 | – | 10 | V |
| Available output current | $\pm I_{17}$ | – | 1 | – | mA |
| Output voltage at nominal tuning of the reference tuned circuit | $V_{17-19}$ | – | 5,25 | – | V |
| **Sound circuit** | | | | | |
| Input limiting voltage when $V_O = V_{Omax} - 3$ dB (note 10) | $V_{14\,lim}$ | – | 400 | – | μV |
| Input resistance at pin 15 (note 11) | $R_i$ | – | 3 | – | kΩ |
| A.F. output signal at pin 12 (note 12) (r.m.s. value) | $V_{12-10(rms)}$ | 170 | – | 240 | mV |
| **Volume control (pin 11) (Fig. 3)** | | | | | |
| Voltage with pin 11 disconnected | $V_{11-10}$ | – | 6,5 | – | V |
| Current pin 11 short-circuited to ground | $I_{11}$ | – | 1 | – | mA |
| Volume control characteristic (note 13) | | | See Fig. 3 | | |
| Value of external control resistor | $R_{11-10}$ | – | 5 | – | kΩ |

| parameter | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| **Horizontal synchronization circuit** | | | | | |
| Slicing level sync separator (note 14) | | – | 30 | – | % |
| Holding range PLL | | – | ±1000 | – | Hz |
| Catching range PLL | | – | ±600 | – | Hz |
| Control sensitivity video to flyback (note 15) | | – | 2 | – | kHz/μs |
| **Horizontal oscillator** | | | | | |
| Free running frequency | $f_{osc}$ | – | 15625 | – | Hz |
| Spread with fixed external components | $\Delta f_{osc}$ | – | – | 4 | % |
| Frequency variations due to supply voltage changes (note 16) | $\Delta f_{osc}/\Delta V$ | – | 0 | – | % |
| Frequency variation with temperature | $\Delta f_{osc}/\Delta T$ | – | – | $1 \times 10^{-4}$ | $K^{-1}$ |
| Maximum frequency shift | $\Delta f_{osc}$ | – | – | 10 | % |
| Maximum frequency deviation between starting point output and nominal condition | $\Delta f_{osc}$ | – | – | 10 | % |
| **Horizontal (push-pull) output** | | | | | |
| Output current | $I_{27}$ | 10 | – | – | mA |
| Output impedance | $R_{27-10}$ | – | 200 | – | Ω |
| Voltage when $I_{27}$ = 10 mA | $V_{27-10}$ | – | 2 | – | V |
| | $V_{27-22}$ | – | 3 | – | V |
| Duty cycle of output pulse (note 17) | δ | 0,35 | 0,40 | 0,45 | |
| **Flyback input (note 18)** | | | | | |
| Minimum required input amplitude (peak-to-peak value) | $V_{5-10(p-p)}$ | – | 4 | – | V |
| Phase detector switching voltage | | – | 0 | – | V |

CHARACTERISTICS (continued)

| parameter | symbol | min. | typ. | max. | unit |
|---|---|---|---|---|---|
| **Coincidence detector (mute) (note 19)** | | | | | |
| Voltage in synchronized condition | $V_{28-19}$ | – | 9,5 | – | V |
| Voltage in non-synchronized condition (no-signal) | $V_{28-19}$ | – | 1,0 | 1,5 | V |
| Switching level to switch phase detector from slow to fast | $V_{28-19}$ | 4,5 | 5,0 | 5,5 | V |
| Switching level to activate the 'mute' function (transmitter identification) | $V_{28-19}$ | 2,25 | 2,5 | 2,75 | V |
| Output current; in-sync (peak-to-peak value) | $I_{28(p-p)}$ | – | 1 | – | mA |
| **Vertical oscillator** | | | | | |
| Free running frequency | $f_{osc}$ | – | 47,5 | – | Hz |
| Spread with fixed external components | $\Delta f_{osc}$ | – | – | 4 | % |
| Holding range at nominal frequency | | 52,5 | – | – | Hz |
| Temperature coefficient | TC | – | $1 \times 10^{-4}$ | – | $K^{-1}$ |
| Frequency shift due to a supply voltage change from 9,5 to 12 V | $\Delta f_{osc}/\Delta V$ | – | 5 | – | % |
| **Vertical output (pin 2)** | | | | | |
| Output current | $I_2$ | 1 | 1,3 | – | mA |
| Output resistance | $R_{2-10}$ | – | 2 | – | kΩ |
| **Feedback input (pin 3)** | | | | | |
| D.C. input voltage | $V_{3-10}$ | 4,75 | 5 | 5,25 | V |
| A.C. input voltage (peak-to-peak value) | $V_{3-10(p-p)}$ | – | 1,2 | – | V |
| Input current | $I_3$ | – | – | 10 | μA |
| Non-linearity of deflection current at $V_P$ = 10,5 V | | – | – | 2,5 | % |

## Notes to characteristics

1. It is possible to start the horizontal oscillator by supplying a current of 5 mA which can be taken from the mains rectifier, to pin 22. The main supply (pin 7) can then be derived from the horizontal output stage.
2. I.F. input voltage (r.m.s.) — value at top sync level at which the video amplitude has dropped 0,5 dB compared with the amplitude at an input signal of 10 mV.
3. The input impedance has been chosen such that a SAW-filter can be applied. 800 Ω is an acceptable compromise between the requirements for triple transient suppression and power loss.
4. Measured with 0 dB = 150 μV.
5. Measured at 10 mV(r.m.s.) top sync input signal.
6. With switched demodulator.
7. Signal with negative-going sync with top white being 10% of the top sync amplitude (Fig. 2).
8. This figure is valid for the complete video signal amplitude (peak-white to top sync).
9. Measured with an input signal ($V_{8-9}$) of 10 mV(r.m.s.); the a.f.c. output (pin 7) loaded with 2 x 100 kΩ between the supply and ground. The Q factor of the reference tuned circuit is 50.
10. Voltage at pin 15 is the r.m.s. value. $Q_L$ of the demodulator tuned circuit is 20. Audio frequency is 1 kHz and the carrier frequency is 5,5 MHz.
11. Measured with an input signal of 1 mV(r.m.s.)
12. The tuned demodulator circuit must give an output level equal to that given in the "mute" condition.
13. Volume can be controlled using a variable resistor connected to ground (nominal 5 kΩ) or by means of a variable d.c. voltage. In this latter case the rather low impedance at pin 11 must be taken into account.

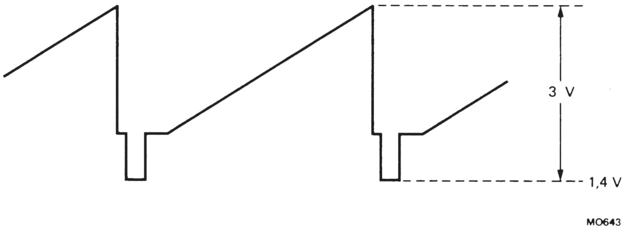


Fig. 2 Video output signal.

**Notes to characteristics (continued)**

14. The sync separator is noise gated. The slicing level is referred to top sync level and is independent of the video information. The value given is a percentage of the sync pulse amplitude. The slicing depends on the values of external resistors connected to pin 26.
15. Phase detector current increases by a factor of 7 during "catching" and when phase detector operates in the 'FAST' mode (pin 28). This ensures a high catching range and a higher dynamic loop gain.
16. Supply voltage variation in the range 8 to 12 V.
17. The negative-going edge of this pulse initiates the switch-off of the horizontal output transistor (simultaneous driver).
18. The circuit requires an integrated flyback pulse. The gate pulses for a.g.c. and the coincidence detector are obtained from the sawtooth.
19. The functions of in-sync/out-of-sync and transmitter identification have been combined on pin 28. For reception of VCR-signals the voltage on this pin must be fixed between 3 V and 4,5 V so that the time constant is fast and the sound is still available.

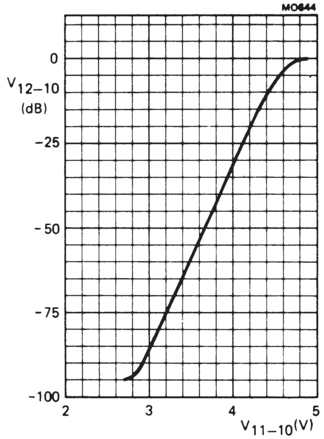


Fig. 3 Volume control characteristic at f = 1 kHz.

## APPLICATION INFORMATION

DEVELOPMENT SAMPLE DATA

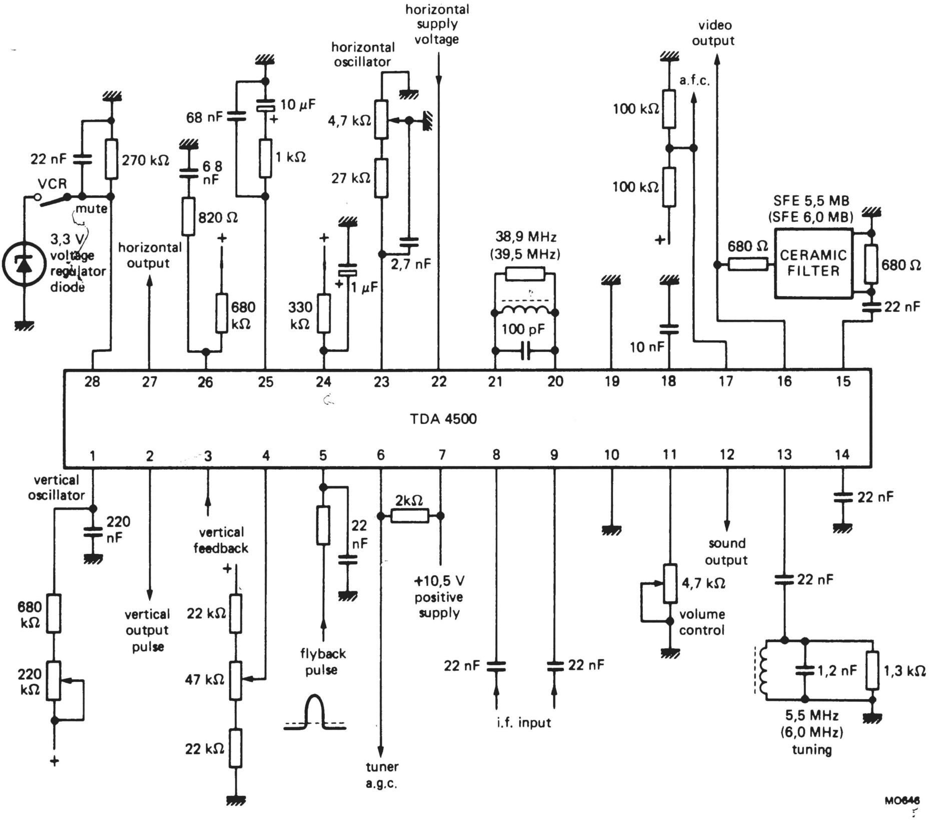

horizontal supply voltage
horizontal oscillator
video output
a.f.c.
22 nF
270 kΩ
VCR
mute
3,3 V voltage regulator diode
68 nF
10 μF
1 kΩ
6 8 nF
820 Ω
horizontal output
680 kΩ
4,7 kΩ
27 kΩ
2,7 nF
330 kΩ
1 μF
100 kΩ
100 kΩ
38,9 MHz
(39,5 MHz)
100 pF
10 nF
680 Ω
SFE 5,5 MB
(SFE 6,0 MB)
CERAMIC FILTER
680 Ω
22 nF
28
27
26
25
24
23
22
21
20
19
18
17
16
15
TDA 4500
1
2
3
4
5
6
7
8
9
10
11
12
13
14
vertical oscillator
220 nF
680 kΩ
220 kΩ
vertical output pulse
vertical feedback
22 kΩ
47 kΩ
22 kΩ
22 nF
flyback pulse
2kΩ
+10,5 V positive supply
tuner a.g.c.
22 nF
22 nF
i.f. input
4,7 kΩ
volume control
sound output
22 nF
22 nF
1,2 nF
1,3 kΩ
5,5 MHz
(6,0 MHz)
tuning
MO646

Fig. 4 Typical application circuit.

# PAL COLOUR ENCODER AND VIDEO SUMMER

The TEA1002 is mainly intended for video games, add-on teletext applications and colour bar generators for video test equipment. It is a bipolar integrated circuit which converts binary colour information into a PAL composite video output suitable for driving a v.h.f./u.h.f. modulator.

## QUICK REFERENCE DATA

| | | | | |
|---|---|---|---|---|
| Supply voltage (pin 10) | $V_P = V_{10\text{-}16}$ | nom. | 12 | V |
| Supply current at $V_P$ = 12 V | $I_P = I_{10}$ | typ. | 70 | mA |
| Input voltages (pins, 1, 2, 3, 4, 5, 12, 15, 18) | | | | |
| LOW | $V_{IL}$ | $\leqslant$ | 0,8 | V |
| HIGH | $V_{IH}$ | $\geqslant$ | 2,0 | V |
| Composite video output voltage (pin 8) | | | | |
| peak-to-peak value | $V_{8\text{-}16(p\text{-}p)}$ | typ. | 3 | V |
| Operating ambient temperature range | $T_{amb}$ | | −20 to +65 | °C |

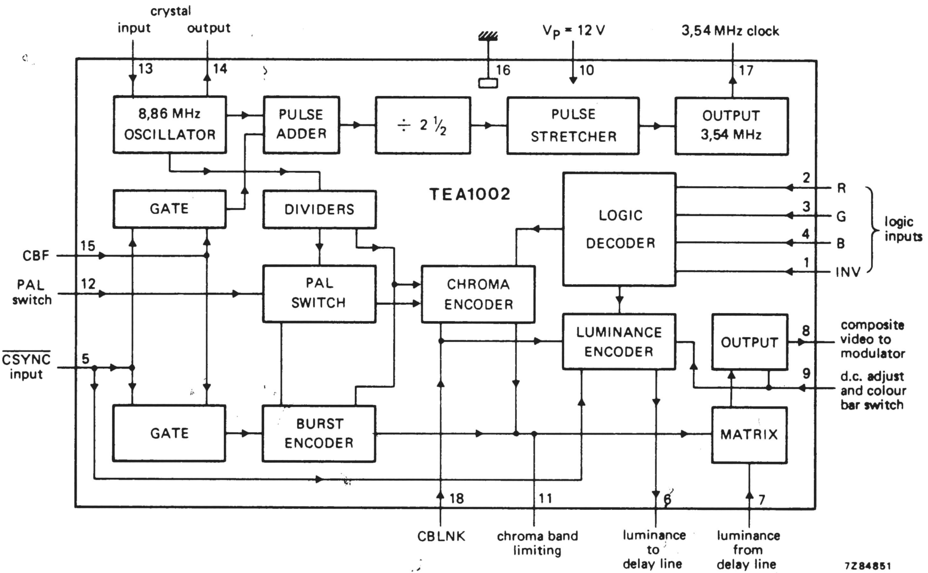

crystal
input
output
13
14
Vp = 12 V
3,54 MHz clock
16
10
17
8,86 MHz OSCILLATOR
PULSE ADDER
÷ 2 ½
PULSE STRETCHER
OUTPUT 3,54 MHz
GATE
DIVIDERS
TEA1002
LOGIC DECODER
2
R
3
G
4
B
1
INV
logic inputs
CBF
15
PAL switch
12
PAL SWITCH
CHROMA ENCODER
LUMINANCE ENCODER
OUTPUT
8
composite video to modulator
CSYNC input
5
9
d.c. adjust and colour bar switch
GATE
BURST ENCODER
MATRIX
18
11
6
7
CBLNK
chroma band limiting
luminance to delay line
luminance from delay line
7Z84851

Fig. 1 Block diagram.

## PACKAGE OUTLINE

18-lead DIL; plastic (SOT-102CS).

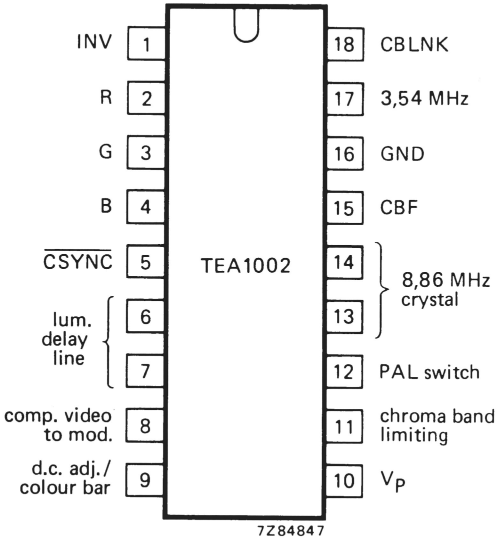

INV
R
G
B
$\overline{\text{CSYNC}}$
lum. delay line
comp. video to mod.
d.c. adj./ colour bar
1
2
3
4
5
6
7
8
9
TEA1002
18
17
16
15
14
13
12
11
10
CBLNK
3,54 MHz
GND
CBF
8,86 MHz crystal
PAL switch
chroma band limiting
$V_P$
7Z84847

Fig. 2 Pinning diagram.

**PINNING**

| | | | |
|---|---|---|---|
| 1 | INV | inverting logic input | |
| 2 | R | red logic input | |
| 3 | G | green logic input | |
| 4 | B | blue logic input | |
| 5 | $\overline{\text{CSYNC}}$ | composite sync input | |
| 6 | | luminance output to delay line | |
| 7 | | luminance input from delay line | |
| 8 | | composite video output to modulator | |
| 9 | | d.c. adjust and colour bar switch | |
| 10 | $V_P$ | supply voltage (+ 12 V) | |
| 11 | | chroma band limiting | |
| 12 | | PAL switch input | |
| 13 | | crystal input | 8,86 MHz |
| 14 | | crystal output | |
| 15 | CBF | colour burst flag input | |
| 16 | GND | ground | |
| 17 | 3,54 MHz | clock output | |
| 18 | CBLNK | composite blanking input | |

## GENERAL DESCRIPTION

The TEA1002 PAL colour encoder and video summer IC has an internal 8,86 MHz oscillator from which the 4,43 MHz (R-Y) and B-Y) waveforms are generated. For use in TV games systems, a 3,54 MHz clock output is provided which is buffered via the 2621 sync generator IC. The TEA1002 accepts timing signals (composite sync burst gate, PAL switch and composite blanking) from the 2621 and 4-bit binary coded logic inputs giving colour information from the 2636 programmable video interface IC. The resulting output, which has an adjustable d.c. level, is a 16 colour (including black and white) composite video signal, based on 75% colour bars. Alternatively, with one of the colour inputs connected to ground and the d.c. adjustment disabled, the TEA1002 can be used as a general purpose video encoder providing standard 95% colour bars from RGB logic inputs, suitable for applications such as add-on teletext.

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | | |
|---|---|---|---|---|
| Supply voltage (pin 10) | $V_P = V_{10\text{-}16}$ | max. | 13,2 | V |
| Input voltage (pins 1, 2, 3, 4, 5, 12, 15, 18) HIGH | $V_{IH}$ | max. | $V_P$ | V |
| Storage temperature range | $T_{stg}$ | | −25 to + 125 | °C |
| Operating ambient temperature range | $T_{amb}$ | | −20 to +65 | °C |

## CHARACTERISTICS

$T_{amb}$ = 25 °C; $V_P$ = 12 V; measured in Fig. 8; unless otherwise specified

| | | min. | typ. | max. | |
|---|---|---|---|---|---|
| Supply voltage | $V_P = V_{10\text{-}16}$ | 10,8 | 12 | 13,2 | V |
| Supply current | $I_P = I_{10}$ | – | 70 | – | mA |
| **Clock output** (pin 17) (notes 1 and 2, Fig. 6) | | | | | |
| Clock cycle time | T | – | 282 | – | ns |
| Output voltage (peak-to-peak value) measured into 30 pF load capacitance | $V_{17\text{-}16(p\text{-}p)}$ | 4 | – | 6 | V |
| Output rise time into 30 pF load | $t_r$ | – | 4 | 30 | ns |
| Output fall time into 30 pF load | $t_f$ | – | 10 | 30 | ns |
| Clock pulse width LOW measured at + 0,8 V after restoration | $t_L$ | 100 | 140 | – | ns |
| Clock pulse width HIGH measured at + 2,4 V after restoration | $t_H$ | 100 | 130 | – | ns |
| **Oscillator stability** (pins 13, 14) (notes 3 and 4) | | | | | |
| Variation in internal 4,43 MHz reference clock frequency | | | | | |
| temperature range: –20 to + 25 °C | $\Delta f_{osc}/\Delta T$ | – | –0,8 | – | Hz/K |
| + 25 to + 70 °C | $\Delta f_{osc}/\Delta T$ | – | –2,6 | – | Hz/K |
| supply voltage range: 10,8 to 13,2 V | $\Delta f_{osc}/\Delta V_P$ | – | –25 | – | Hz/V |
| **Timing inputs** (pins 5, 12, 15, 18) (Fig. 3) | | | | | |
| Input voltage LOW | $V_{IL}$ | – | – | 0,8 | V |
| Input voltage HIGH | $V_{IH}$ | 2 | – | $V_P$ | V |
| Input current LOW (d.c.); $V_I$ = 0 V | $I_{IL}$ | – | – | 100 | μA |
| Input current HIGH (d.c.); $V_I$ = 12 V | $I_{IH}$ | – | – | 100 | μA |
| Input capacitance | $C_I$ | – | – | 10 | pF |
| Input rise and fall times | $t_r$, $t_f$ | – | – | 200 | ns |
| **Colour code inputs** (pins 1, 2, 3, 4) (note 6) | | | | | |
| Input voltage LOW | $V_{IL}$ | – | – | 0,8 | V |
| Input voltage HIGH | $V_{IH}$ | 2 | – | $V_P$ | V |
| Input current LOW (d.c.); $V_I$ = 0 V | $I_{IL}$ | – | – | 100 | μA |
| Input current HIGH (d.c.); $V_I$ = 12 V | $I_{IH}$ | – | – | 100 | μA |
| Input capacitance | $C_I$ | – | – | 10 | pF |

DEVELOPMENT SAMPLE DATA

## CHARACTERISTICS (continued)

| | | min. | typ. | max. | |
|---|---|---|---|---|---|
| **Composite video output** (pin 8) (note 5, Table 1) | | | | | |
| Output voltage (peak-to-peak value)<br>sync tip to white | $V_{8\text{-}16(p\text{-}p)}$ | – | 3 | – | V |
| Residual chroma voltage on white<br>(r.m.s. value) (4,43 MHz) | $V_{8\text{-}16(rms)}$ | – | 30 | – | mV |
| Sync tip d.c. levels<br>for $V_{9\text{-}16}$ = 12 V | $V_{8\text{-}16}$ | – | 5,1 | – | V |
| for $V_{9\text{-}16} < 9$ V | $V_{8\text{-}16}$ | – | 2,6 | – | V |
| **D.C. output adjustment** (pin 9) | | | | | |
| D.C. adjustment voltage range<br>where $\Delta V_{8\text{-}16} = \Delta V_{9\text{-}16}$ | $V_{9\text{-}16}$ | 9,5 | – | 12 | V |
| Applied voltages to guarantee<br>75% colour bars | $V_{9\text{-}16}$ | 4 | – | – | V |
| 95% colour bars | $V_{9\text{-}16}$ | – | – | 3 | V |
| **Chroma band limiting** (pin 11) | | | | | |
| Internal impedance at pin 11 | $\lvert Z_i \rvert$ | – | 1,5 | – | kΩ |

**Notes**

1. This circuit assumes capacitive coupling to the N-MOS games IC (see Fig. 5).
2. The integrated circuit gates the CBF and CSYNC signals to provide a 'frame offset' which lengthens two clock periods by 56 ns every field. This provides a subcarrier/line frequency relationship of $f_{sc} = 283\frac{3}{4} f_l + 25$ Hz which gives an optimum picture response.
3. These figures hold for a typical quartz crystal as specified below:
   Crystal catalogue no. 4322 143 04051, used in series with 20 pF trimmer capacitance ($C_L$).
   motional resistance (R1): typ. 15 Ω; max. 60 Ω
   static capacitance (C0): typ. 5 pF; max. 6 pF.
4. These figures exclude the temperature dependence of the crystal and load capacitance ($C_L$).
5. The chroma/luminance phase inequality can be compensated by an external delay line connected between pins 6 and 7 (see Fig. 8).
   For measurements on the composite video output use the circuit as shown in Fig. 7.
6. To generate standard colour bar signals, pin 1 must be grounded externally.

## APPLICATION INFORMATION

**The function is described against the corresponding pin number**

1. **Inverting logic input**

   When this pin is connected to ground, the logic inputs on pins 2, 3 and 4 are decoded as R, G and B respectively and the chrominance signal at the output is at its full amplitude. If this pin is taken HIGH (> 2 V) the logic inputs are decoded as $\overline{R}$, $\overline{G}$ and $\overline{B}$ and the chrominance signal is reduced to half its full amplitude (see Table 1).

2, 3, 4. **Red, green and blue logic inputs**

5. **Composite sync input**

   This pin requires a negative logic composite sync signal ($\overline{\text{CSYNC}}$). The signal is also gated with CBF to control a frame offset phase adjustment for the 3,54 MHz clock (see pins 13 and 14).

6, 7. **Luminance delay line**

The combined luminance and sync signal appearing at pin 6 must be d.c. coupled to pin 7 via an appropriate luminance delay line or resistor network. The resistors must have a tolerance of ± 5% (see Fig. 7).

8. **Composite video output**

The output is internally buffered by an emitter follower stage giving a nominal output voltage of 3 V sync-white. The d.c. level is temperature compensated and can be continuously adjusted over a nominally 2,5 V range via an input on pin 9.

9. **D.C. adjustment and colour bar switch**

This pin provides the dual function of d.c. level adjustment for the composite video output stage and colour bar standard selection. An adjustment of $V_{9\text{-}16}$ from 9,5 V to 12 V will cause a corresponding change of output sync tip level from 3 V to 5,5 V (nominal values).

With $V_{9\text{-}16} \geqslant 4$ V the luminance levels are set to give 75% (E.B.U.) colour signals when using the RGB inputs with pin 1 grounded. With $V_{9\text{-}16} \leqslant 3$ V the output levels will be changed to give 95% (B.B.C.) colour signals (see Table 1). Thus d.c. adjustment can only be obtained with 75% colours.

10. **Supply voltage** (+ 12 V)

11. **Chroma band limiting**

This pin is connected internally to the chrominance summing junction and may be used to limit the bandwidth of the chroma signal by connecting it to a 4,43 MHz tuned filter via a blocking capacitor. The internal impedance is nominally 1,5 kΩ. If a filter is used at this point, then the delay of the chroma signals must be compensated by an appropriate luminance delay line between pins 6 and 7.

12. **PAL switch**

This pin requires a logic signal at half line frequency to control the phase of the (R-Y) modulator and the burst signal.

13, 14. **8,86 MHz crystal**

An 8,867238 MHz crystal in series with a trimmer capacitor is connected between these pins to form part of an oscillator. The output of the oscillator is divided to provide the four subcarrier phases required in the encoder.

The 8,86 MHz signal is also divided by 2½ to give a 3,54 MHz clock input to the 2621 sync generator IC. A phase correction is made after every field to ensure the correct subcarrier to line frequency relationship.

15. **Colour burst flag**

This pin requires a positive logic signal to enable the colour burst encoder.

16. **Ground** (0 V)

17. **Clock output**

The 3,54 MHz clock signal from this pin must be a.c. coupled to the 2621 sync generator IC.

18. **Composite blanking**

This pin requires a positive logic composite blanking signal. The colour logic inputs at pins 1 to 4 are gated to logic '0' when this input is HIGH.

**APPLICATION INFORMATION** (continued)

Table 1. Logic inputs and composite video output

| | inputs | | | | colour | nominal outputs | | | |
|---|---|---|---|---|---|---|---|---|---|
| | pin 2 R | pin 3 G | pin 4 B | pin 1 INV | | luminance $V_{9\text{-}16} \geqslant 4$ V (%) | luminance $V_{9\text{-}16} \leqslant 3$ V (%) | chroma phase (degrees) | chroma amplitude (% black-white) |
| 1 | 0 | 0 | 0 | 0 | black | 0<br>75% (E.B.U.) colour bars | 0<br>95% (B.B.C.) colour bars | – | – |
| 2 | 1 | 0 | 0 | 0 | red | 22,5 | 47,5 | 103 | ± 48 |
| 3 | 0 | 1 | 0 | 0 | green | 44 | 69 | 241 | ± 44 |
| 4 | 1 | 1 | 0 | 0 | yellow | 66,5 | 91,5 | 167 | ± 33 |
| 5 | 0 | 0 | 1 | 0 | blue | 8,5 | 33,5 | 347 | ± 33 |
| 6 | 1 | 0 | 1 | 0 | magenta | 31 | 56 | 61 | ± 44 |
| 7 | 0 | 1 | 1 | 0 | cyan | 52,5 | 77,5 | 283 | ± 48 |
| 8 | 1 | 1 | 1 | 0 | white | 100 | 100 | – | – |
| 9 | 0 | 0 | 0 | 1 | grey | 75 | 100 | – | – |
| 10 | 1 | 0 | 0 | 1 | cyan | 52,5 | 77,5 | 283 | ± 24 |
| 11 | 0 | 1 | 0 | 1 | magenta | 31 | 56 | 61 | ± 22 |
| 12 | 1 | 1 | 0 | 1 | blue | 8,5 | 33,5 | 347 | ± 17 |
| 13 | 0 | 0 | 1 | 1 | yellow | 66,5 | 91,5 | 167 | ± 17 |
| 14 | 1 | 0 | 1 | 1 | green | 44 | 69 | 241 | ± 22 |
| 15 | 0 | 1 | 1 | 1 | red | 22,5 | 47,5 | 103 | ± 24 |
| 16 | 1 | 1 | 1 | 1 | black | 0 | 0 | – | – |

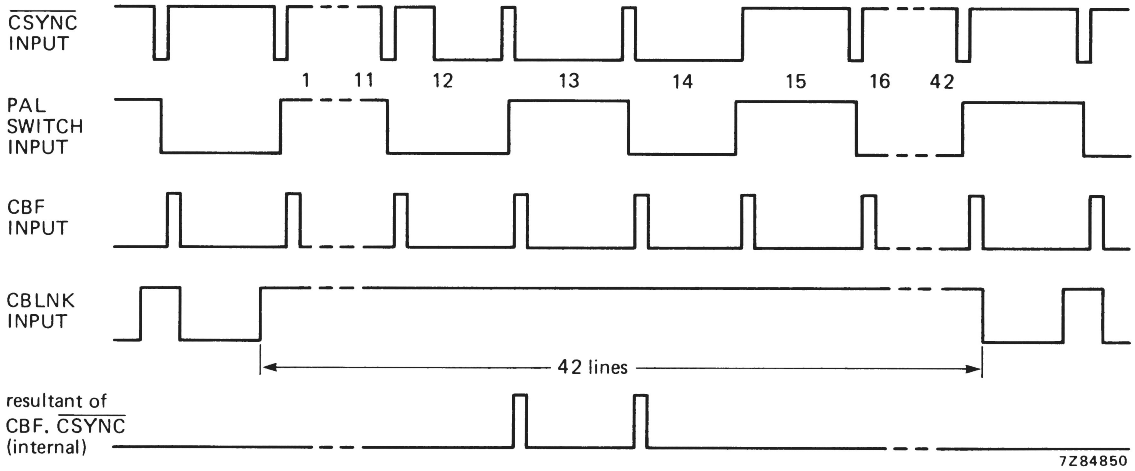

$\overline{\text{CSYNC}}$ INPUT
PAL SWITCH INPUT
CBF INPUT
CBLNK INPUT
resultant of CBF. $\overline{\text{CSYNC}}$ (internal)
1
11
12
13
14
15
16
42
42 lines
7Z84850

Fig. 3 Timing diagram (signals supplied from sync generator IC).

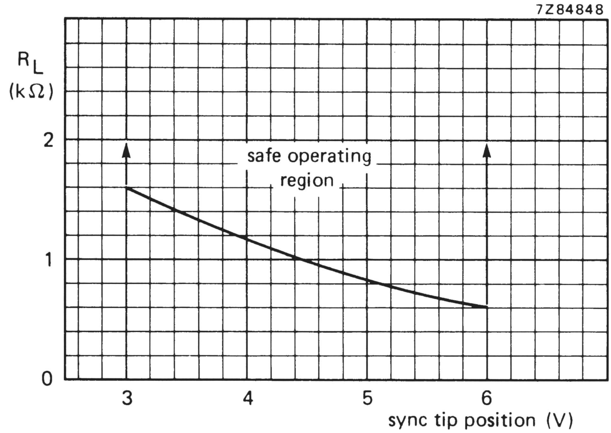


Fig. 4 Safe operating area for load resistor ($R_L$) at pin 8 as a function of sync tip d.c. position.

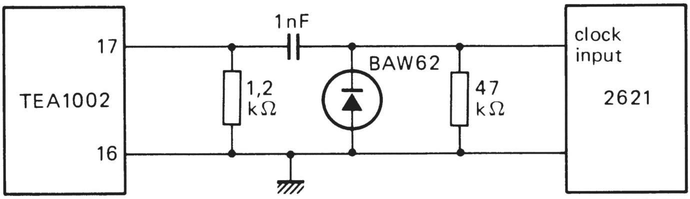

TEA1002
17
16
1 nF
1,2 kΩ
BAW62
47 kΩ
clock input
2621
7Z84853

Fig. 5 Clock coupling circuit.

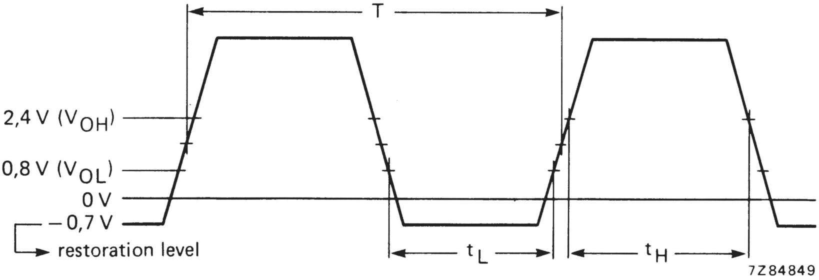

T
2,4 V ($V_{OH}$)
0,8 V ($V_{OL}$)
0 V
−0,7 V
restoration level
$t_L$
$t_H$
7Z84849

Fig. 6 Clock output waveform at pin 17 to the input of the 2621.

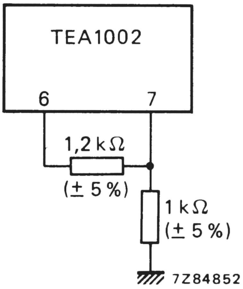
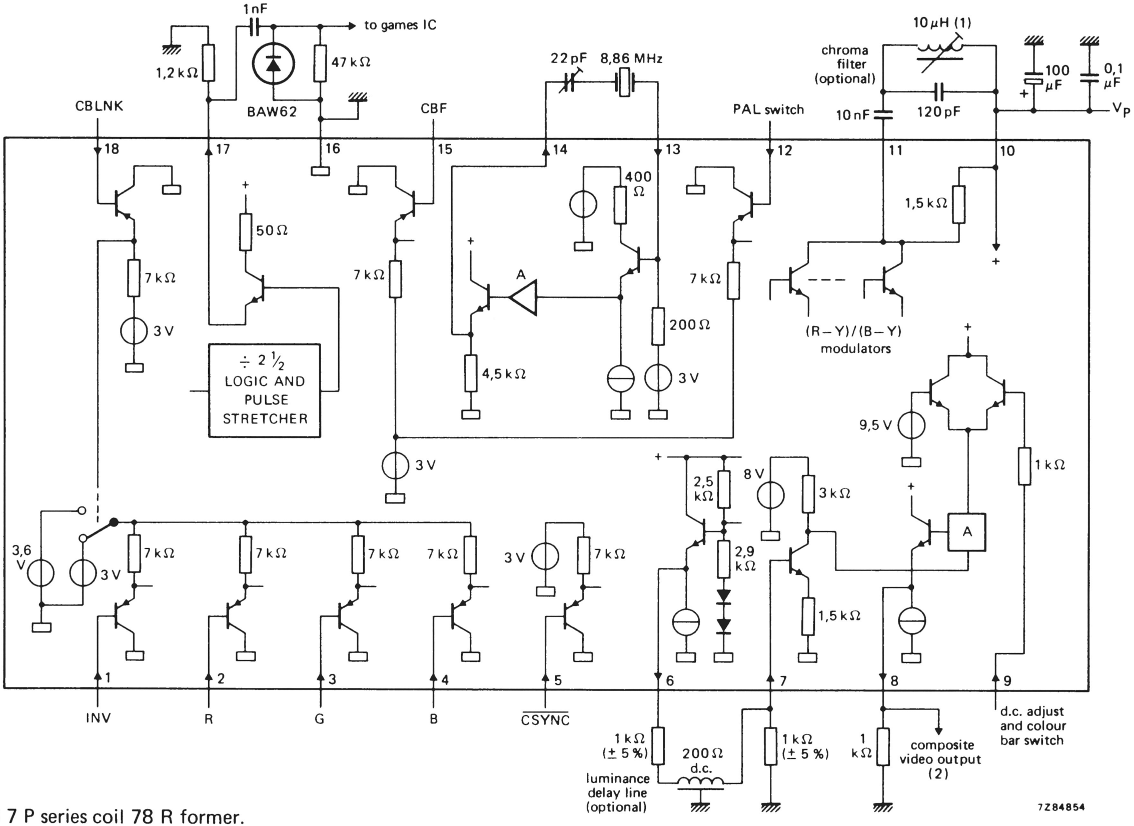

TEA1002
6
7
1,2 kΩ
(± 5 %)
1 kΩ
(± 5 %)
7Z84852

Fig. 7 Connections for pins 6 and 7 when no luminance delay line is used.

## DEVELOPMENT SAMPLE DATA


1nF
to games IC
1,2 kΩ
47 kΩ
BAW62
CBLNK
CBF
22pF
8,86 MHz
PAL switch
10 μH (1)
chroma
filter
(optional)
10nF
120pF
100 μF
0,1 μF
V_P
18
17
16
15
14
13
12
11
10
50 Ω
7 kΩ
3 V
÷ 2 ½
LOGIC AND
PULSE
STRETCHER
A
400 Ω
4,5 kΩ
200 Ω
1,5 kΩ
(R−Y)/(B−Y)
modulators
9,5 V
1 kΩ
2,5 kΩ
8 V
3 kΩ
2,9 kΩ
1,5 kΩ
3,6 V
1
2
3
4
5
6
7
8
9
INV
R
G
B
CSYNC
1 kΩ
(± 5 %)
200 Ω
d.c.
luminance
delay line
(optional)
1 kΩ
composite
video output
(2)
d.c. adjust
and colour
bar switch
7Z84854

(1) TOKO 7 P series coil 78 R former.
(2) See derating curve Fig. 4.

Fig. 8 Internal circuit details and typical external connections.

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